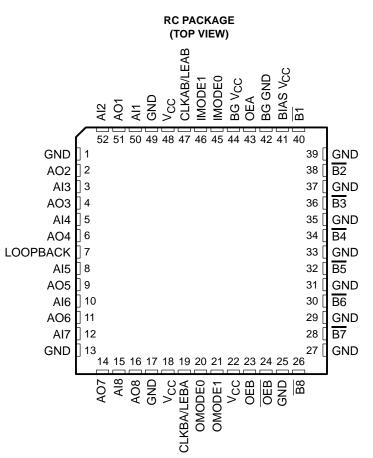
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- Compatible With IEEE Std 1194.1-1991 (BTL)
- TTL A Port, Backplane Transceiver Logic (BTL) B Port
- Open-Collector B-Port Outputs Sink 100 mA
- BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- High-Impedance State During Power Up and Power Down
- B-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination



description

The SN74FB2033K is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector \overline{B} port operates at backplane transceiver logic (BTL) signal levels. The SN74FB2033K is specifically designed to be compatible with IEEE Std 1194.1-1991.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock inputs serve as active-high transparent latch enables.



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description (continued)

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (before inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The \overline{B} port is controlled by OEB and \overline{OEB} . If OEB is low, or \overline{OEB} is high, or when V_{CC} is less than 2.5 V, the \overline{B} port is inactive. If OEB is high and \overline{OEB} is low, the \overline{B} port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive (B port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both of these clamps are active only during ac switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

TA	PACKAGE [†]		0	TOP-SIDE MARKING	
0°C to 70°C	QFP – RC Tube		SN74FB2033KRC	FB2033K	

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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					FUNCTIO	N		
				INPUTS				FUNCTION/MODE
OEA	OEB	OEB	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	FUNCTION/MODE
L	L	Х	Х	Х	Х	Х	х	Isolation
L	Х	Н	Х	Х	Х	Х	Х	1301411011
Х	Н	L	L	L	Х	Х	Х	AI to \overline{B} , buffer mode
Х	Н	L	L	Н	Х	Х	Х	AI to \overline{B} , flip-flop mode
Х	Н	L	Н	Х	Х	Х	Х	AI to B, latch mode
Н	L	Х	Х	Х	L	L	L	
Н	Х	Н	Х	Х	L	L	L	B to AO, buffer mode
Н	L	Х	Х	Х	L	Н	L	E to AQ film flom mode
Н	Х	Н	Х	Х	L	Н	L	B to AO, flip-flop mode
Н	L	Х	Х	Х	Н	Х	L	
Н	Х	Н	Х	Х	Н	Х	L	\overline{B} to AO, latch mode
Н	L	Х	Х	Х	L	L	Н	AI to AO, buffer mode
Н	Х	Н	Х	Х	L	L	Н	AI to AO, builer mode
Н	L	Х	Х	Х	L	Н	Н	Al to AQ flip flop mode
Н	Х	Н	Х	Х	L	Н	Н	AI to AO, flip-flop mode
Н	L	Х	Х	Х	Н	Х	Н	AI to AO, latch mode
Н	Х	Н	Х	Х	Н	Х	Н	
Н	Н	Ĺ	Х	Х	Х	Х	L	AI to B, B to AO

Function Tables

ENABLE/DISABLE

	INPUTS			ITPUTS		
OEA	OEB	OEB	AO B			
L	Х	Х	Hi Z			
н	Х	Х	Active			
X	L	L		Inactive (H)		
X	L	н		Inactive (H)		
X	Н	L		Active		
Х	Н	Н		Inactive (H)		

BUFFER

INPUT	OUTPUT
L	Н
Н	L

LATCH

INPU	OUTPUT					
CLK/LE	DATA	001901				
Н	H L					
н	Н	L				
L	Х	Q ₀				



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Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	B port
н	Point P [‡]

[†]Q is the input to the B-to-A logic element. [‡]P is the output of the A-to-B

P is the output of the A-to-B logic element (see functional block diagram).

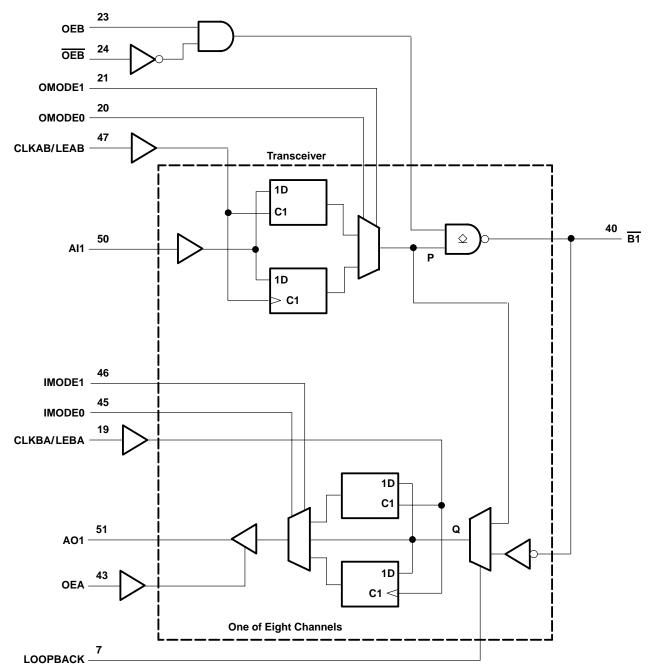
INPUTS		SELECTED-LOGIC		
MODE1	MODE0	ELEMENT		
L L		Buffer		
L	Н	Flip-flop		
н	Х	Latch		

FLIP-FLOP

INPU	OUTPUT			
CLK/LE DATA				
L	Х	Q ₀		
\uparrow	L	Н		
\uparrow	н	L		



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functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} Voltage range applied to any B output in the disabled or power-off state, V_O Voltage range applied to any output in the high state, V_O : A port Input voltage range, V_I : Except \overline{B} port Input clamp current, I_{IK} : Except \overline{B} port \overline{B} port	-0.5 V to 3.5 V -0.5 V to V _{CC} -1.2 V to 7 V -1.2 V to 3.5 V -40 mA -18 mA
Current applied to any single output in the low state, I _O : A port B port	
Package thermal impedance, θ _{JA} (see Note 1)	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT	
V _{CC} , BG V _{CC}	Supply voltage		4.75	5	5.25	V	
BIAS V _{CC}	Supply voltage		4.5	5	5.5	V	
	High lovel input veltage	B port	1.62		2.3	V	
VIH		Except B port	2				
M	Low-level input voltage	B port	0.75		1.47	V	
VIL	Low-level input voitage	Except B port			0.8	v	
IOH	High-level output current	AO port			-3	mA	
le.	Low-level output current	AO port			24	mA	
IOL		B port			100		
$\Delta t/\Delta v$	Input transition rise or fall rate	Except B port			10	ns/V	
Т _А	Operating free-air temperature		0		70	°C	

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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	PARAMETER	TEST C	ONDITIONS	MIN	түр†	MAX	UNIT	
M	B port	V _{CC} = 4.75 V,	lj = –18 mA			-1.2	V	
VIK	Except B port	V _{CC} = 4.75 V,	lj = -40 mA			-0.5	v	
		V _{CC} = 4.75 V to 5.25 V,	I _{OH} = −10 μA			V _{CC} -1.1		
Vон	AO port		I _{OH} = -3 mA	2.5	2.85	3.4	V	
		V _{CC} = 4.75 V	I _{OH} = -32 mA	2				
	40 nort	V	I _{OL} = 20 mA		0.33	0.5		
Mai	AO port	V _{CC} = 4.75 V	I _{OL} = 55 mA			0.8	v	
VOL	= .		I _{OL} = 100 mA	0.75		1.1	V	
	B port	V _{CC} = 4.75 V	$I_{OL} = 4 \text{ mA}$	0.5				
lj	Except B port	$V_{CC} = 0,$	Vj = 5.25 V			100	μΑ	
1	Except B port	V _{CC} = 5.25 V,	V _I = 2.7 V			50	μA	
	B port‡	$V_{CC} = 0$ to 5.25 V,	V _I = 2.1 V			100		
	Except B port	V _{CC} = 5.25 V,	V _I = 0.5 V			-50	۸	
ΙL	B port‡	V _{CC} = 5.25 V,	Vj = 0.75 V			-100	μA	
ЮН	B port	$V_{CC} = 0$ to 5.25 V,	V _O = 2.1 V			100	μΑ	
IOZH	AO port	V_{CC} = 2.1 V to 5.25 V,	V _O = 2.7 V			50	μΑ	
IOZL	AO port	V _{CC} = 2.1 V to 5.25 V,	V _O = 0.5 V			-50	μΑ	
IOZPU	A port	$V_{CC} = 0$ to 2.1 V,	V_{O} = 0.5 V to 2.7 V			50	μΑ	
IOZPD	A port	V _{CC} = 2.1 V to 0,	V_{O} = 0.5 V to 2.7 V			-50	μΑ	
los§	AO port	V _{CC} = 5.25 V,	$V_{O} = 0$	-40	-80	-150	mA	
ICC	All outputs on	V _{CC} = 5.25 V,	IO = 0		45	70	mA	
Ci	AI port and control inputs	V _I = 0.5 V or 2.5 V			5		pF	
Co	AO port	V _O = 0.5 V or 2.5 V			5		pF	
	B port	V _{CC} = 0 to 4.75 V				6	~	
Cio	per IEEE Std 1194.1-1991	V _{CC} = 4.75 V to 5.25 V				6	PF	

electrical characteristics over recommended operating free-air temperature range

[†] All typical values are at V_{CC} = 5 V, TA = 25° C [‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PAR	AMETER		MIN	MAX	UNIT		
ICC (BIAS VCC)		$V_{CC} = 0$ to 4.75 V,	$V_B = 0$ to 2 V,	BIAS V _{CC} = 4.5 V to 5.5 V		1.2	mA
СС (Ы		V _{CC} = 4.75 V to 5.25 V,	$V_{B} = 0$ to 2 V,	BIAS V _{CC} = 4.5 V to 5.5 V		10	μA
VO	B port	$V_{CC} = 0,$	BIAS $V_{CC} = 5 V$		1.62	2.1	V
		$V_{CC} = 0,$	V _B = 1 V,	V_{I} (BIAS V_{CC}) = 4.75 V to 5.25 V	-1		
IO	B port	$V_{CC} = 0$ to 5.25 V,	OEB = 0 to 0.8 V			100	μΑ
		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V			100	

NOTE 3: Power-up sequence is GND, BIAS V_{CC} , V_{CC} .



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V _{CC} =	= 5 V, 25°C	MIN	МАХ	UNIT
		MIN	MAX			
fclock	Clock frequency	0	150	0	150	MHz
tw	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t _{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	2.7		2.7		ns
t _h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA \uparrow	0.7		0.7		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V(V _{CC} = 5 V, T _A = 25°C			МАХ	UNIT	
		(001201)	MIN	TYP	MAX				
f _{max}			150			150		MHz	
^t PLH	AI (through mode)	-	2.8	5.1	6.8	2.8	8.1		
^t PHL	Al (infough mode)	B	2.5	4.2	5.7	2.5	6.1	ns	
^t PLH	\overline{B} (through mode)	AO	3.1	4.3	5.1	2.2	6.6	ns	
^t PHL	в (through mode)	AO	3.1	4.2	5.1	2.6	6	113	
^t PLH	AI (transparent)	B	2.8	5.1	6.8	2.8	8.1	ns	
^t PHL	Ai (iransparent)	В	2.6	4.2	5.7	2.6	6.1	113	
^t PLH	B (transparent)	AO	2.2	4.3	6	2.2	6.6	ns	
^t PHL	B (transparent)	AO	2.5	4.2	5.6	2.5	6	113	
^t PLH	OEB	B	2.7	5.1	6.8	2.7	8.3	ns	
^t PHL	OLB	D	2.4	4.2	5.7	2.4	6.1	113	
^t PLH	OEB	B	2.5	4.8	6.4	2.5	7.7	ns	
^t PHL	UEB	В	2.5	4.3	5.9	2.5	6.4	113	
^t PZH	OEA	AO	1.6	3.6	5.1	1.6	5.6	ns	
^t PZL	ULA		2.3	4.3	5.7	2.3	6		
^t PHZ	OEA	AO	1.7	4	5.5	1.7	5.9	ns	
^t PLZ		AO	1.2	2.9	4.4	1.2	4.7	113	
^t PLH	CLKAB/LEAB	B	5.2	6.5	7.8	3.7	9.9	9.9 ns	
^t PHL	GERRIBIEERB	В	3.8	5.4	7.1	3.4	7.7	110	
^t PLH	CLKBA/LEBA	AO	1.7	3.8	5.5	1.7	5.9	ns	
^t PHL	GERBITEBR		1.8	3.6	5.1	1.8	5.5	110	
^t PLH	OMODE	B	2.9	6.6	8.4	2.9	10	ns	
^t PHL	OMODE	В	3	5.7	7.5	3	8.3	110	
^t PLH	IMODE	AO	1.4	4.1	5.8	1.4	6.4	ns	
^t PHL	INICEL		1.9	4.2	5.7	1.9	5.9		
^t PLH	LOOPBACK	AO	2	5.2	7.3	2	8.2	ns	
^t PHL		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	2.6	4.8	6.3	2.6	6.4	110	
^t PLH	AI	AO	1.7	3.9	5.6	1.7	6.1	ns	
^t PHL			2.2	4.3	5.7	2.2	5.9	113	
t_r Rise time, 1.3 V to 1.8 V, \overline{B} port			1.8	2.5	3.8	1.7	4	ns	
t _f Fall time, 1.8 V to 1.3 V, B port			1.7	2.5	3.8	1.5	4	ns	
t _r Rise time, 10% to 90%, AO			2.5	3.4	4.8	2	5	ns	
t _f Fall time, 90% to 10%, AO			1.5	2.5	3.8	1	5	115	
B-port input pulse rejection						1		ns	

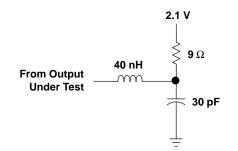
output-voltage characteristics

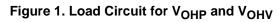
	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
VOHP	Peak output voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1		3	V
VOHV	Minimum output voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1	1.62		V
VOLV	Minimum output voltage during high-to-low switch	B port	I _{OL} = -50 mA	0.3		V



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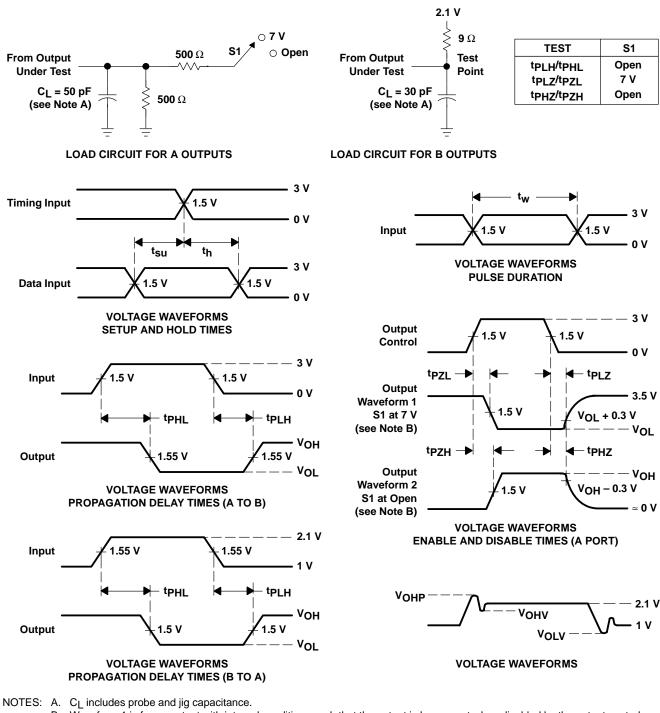
PARAMETER MEASUREMENT INFORMATION







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PARAMETER MEASUREMENT INFORMATION

- - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, tf \leq 2.5 ns; BTL inputs: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, tf \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	e Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74FB2033KRC	ACTIVE	QFP	RC	52	96	TBD	CU SNPB	Level-2-240C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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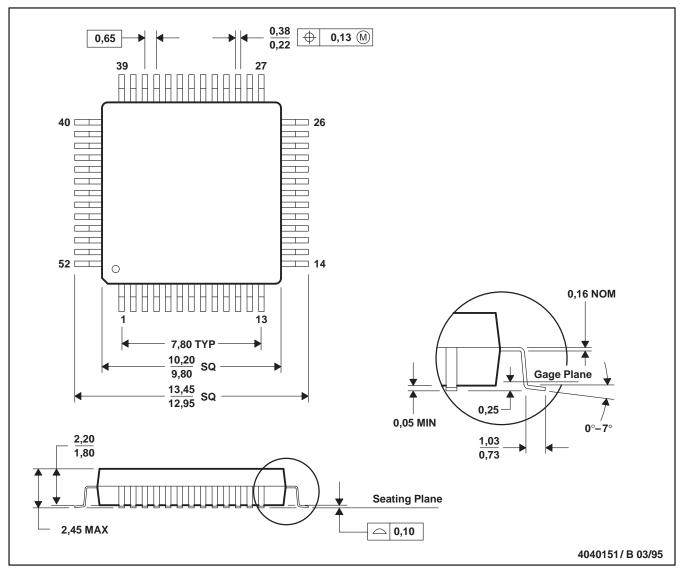
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MECHANICAL DATA

MQFP003 - OCTOBER 1994

RC (S-PQFP-G52)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-022



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