DATA SHEET

74LVC109
Dual $J\overline{K}$ flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 1998 Apr 28

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Philips
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Dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger

74LVC109

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC109A is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC109A is a dual positive edge triggered J$\overline{K}$ flip-flop featuring individual J and $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}$D) and reset ($\overline{R}$D) inputs and complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table. The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The J$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ and nCP to n$\overline{Q}$	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3.3 V	3.8	ns
	propagation delay n$\overline{S}$D to nQ and n$\overline{R}$D to n$\overline{Q}$	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3.3 V	3.2	ns
	propagation delay n$\overline{S}$D to n$\overline{Q}$ and n$\overline{R}$D to nQ	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3.3 V	3.5	ns
f_{max}	maximum clock frequency	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3.3 V	330	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	23	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT					OUTPUT	
	n$\overline{SD}$	n$\overline{RD}$	nCP	nJ	n$\overline{K}$	nQ	n$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load 0 (reset)	H	H	↑	l	l	L	H
Load 1 (set)	H	H	↑	h	h	H	L
Hold no change	H	H	↑	l	h	q	$\overline{q}$

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
   q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition;
   X = don't care;
   ↑ = LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC109D	–40 to +125 °C	16	SO16	plastic	SOT109-1
74LVC109DB	–40 to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC109PW	–40 to +125 °C	16	TSSOP16	plastic	SOT403-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{R}D$	asynchronous reset input (active LOW)
2	1J	synchronous input
3	$1\overline{K}$	synchronous input
4	1CP	clock input (LOW-to-HIGH; edge-triggered)
5	$1\overline{S}D$	asynchronous set input (active LOW)
6	1Q	true flip-flop output
7	$1\overline{Q}$	complement flip-flop output
8	GND	ground (0 V)
9	$2\overline{Q}$	complement flip-flop output
10	2Q	true flip-flop output
11	$2\overline{S}D$	asynchronous set input (active LOW)
12	2CP	clock input (LOW-to-HIGH; edge-triggered)
13	$2\overline{K}$	synchronous input
14	2J	synchronous input
15	$2\overline{R}D$	asynchronous reset input (active LOW)
16	V_{CC}	supply voltage

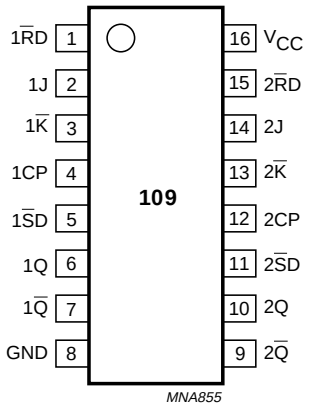


Fig.1 Pin configuration SO16 and (T)SSOP16.

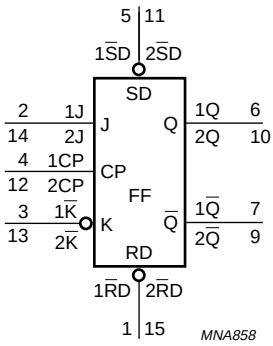


Fig.2 Logic symbol.

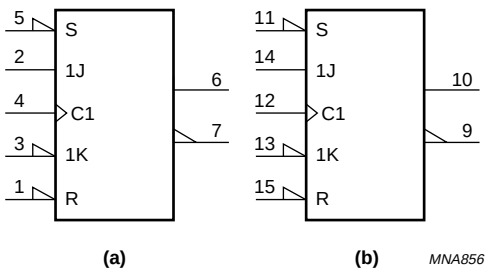


Fig.3 IEC logic symbol.

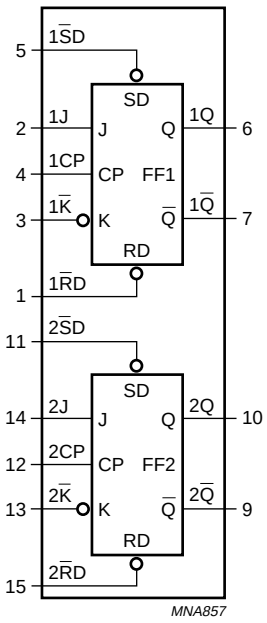


Fig.4 Functional diagram.

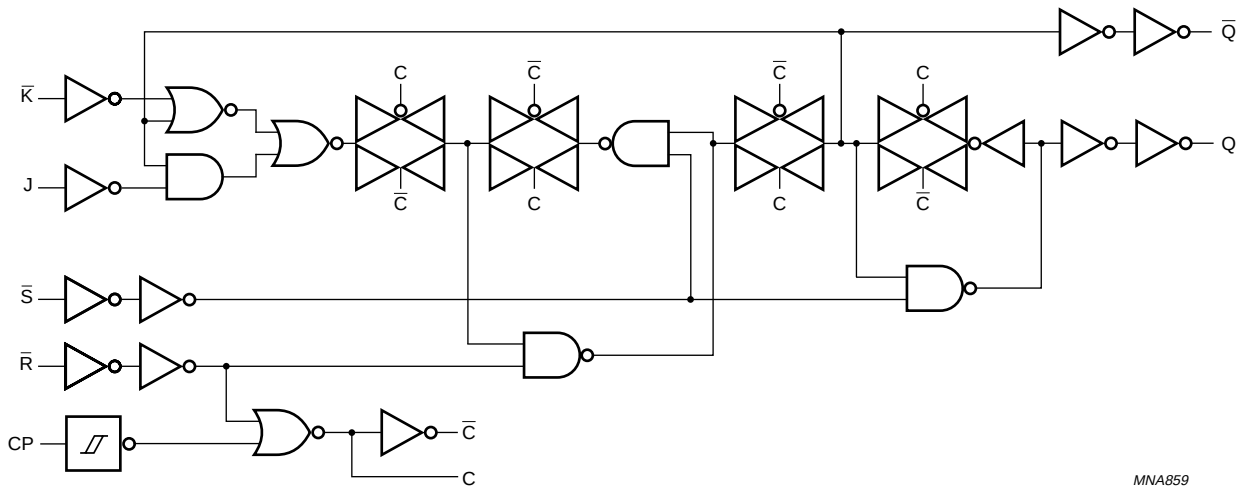


Fig.5 Logic diagram (one flip-flop).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	note 1	–0.5	V_{CC} + 0.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
   For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to 85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.2	V_{CC}	–	V
		I_O = –12 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.6	–	–	V
		I_O = –24 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	GND	0.2	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	±0.1	±5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0 A	2.7 to 3.6	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to 125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.3	–	–	V
		I_O = –12 mA	2.7	V_{CC} – 0.65	–	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.75	–	–	V
		I_O = –24 mA	3.0	V_{CC} – 1.0	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.6	V
		I_O = 24 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0 A	2.7 to 3.6	–	–	5000	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

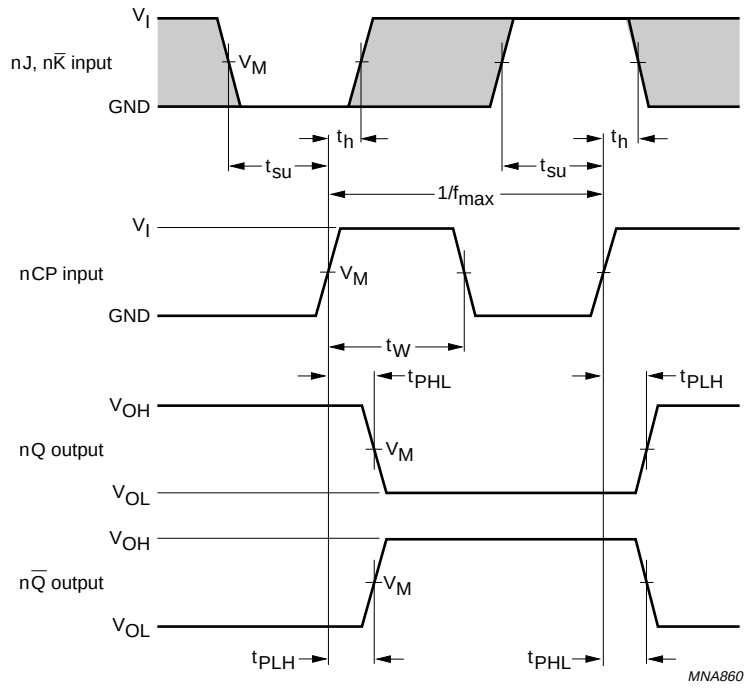
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to 85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ and nCP to n$\overline{Q}$	see Figs 6 and 8	1.2	–	15	–	ns
			2.7	1.5	2.8	7.3	ns
			3.0 to 3.6	1.0	3.8[2]	6.8	ns
t_{PLH}	propagation delay n$\overline{S}$D to nQ and n$\overline{R}$D to n$\overline{Q}$	see Figs 7 and 8	1.2	–	16	–	ns
			2.7	1.5	4.0	8.2	ns
			3.0 to 3.6	1.0	3.2[2]	7.0	ns
t_{PHL}	propagation delay n$\overline{S}$D to n$\overline{Q}$ and n$\overline{R}$D to nQ	see Figs 7 and 8	1.2	–	13	–	ns
			2.7	1.5	4.7	7.1	ns
			3.0 to 3.6	1.0	3.5[2]	6.5	ns
t_W	clock pulse width HIGH or LOW	see Fig. 6	3.0 to 3.6	3.3	2.0	–	ns
	set or reset pulse width HIGH or LOW	see Fig. 7	3.0 to 3.6	3.0	–	–	ns
t_{rem}	removal time n$\overline{S}$D, n$\overline{R}$D to nCP	see Fig. 7	3.0 to 3.6	3.0	–	–	ns
t_{su}	set-up time nJ and n$\overline{K}$ to CP	see Fig. 6	3.0 to 3.6	2.5	–	–	ns
t_h	hold time nJ and n$\overline{K}$ to nCP	see Fig. 6	3.0 to 3.6	2.0	–	–	ns
f_{max}	maximum clock pulse frequency	see Fig. 6	3.0 to 3.6	150	330	–	MHz
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to 125 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ and nCP to n$\overline{Q}$	see Figs 6 and 8	2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.0	–	8.5	ns
t_{PLH}	propagation delay n$\overline{SD}$ to nQ and n$\overline{RD}$ to n$\overline{Q}$	see Figs 7 and 8	2.7	1.5	–	10.5	ns
			3.0 to 3.6	1.0	–	9.0	ns
t_{PHL}	propagation delay n$\overline{SD}$ to n$\overline{Q}$ and n$\overline{RD}$ to nQ	see Figs 7 and 8	2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.0	–	8.5	ns
t_W	clock pulse width HIGH or LOW	see Fig. 6	3.0 to 3.6	3.3	–	–	ns
	set or reset pulse width HIGH or LOW	see Fig. 7	3.0 to 3.6	3.0	–	–	ns
t_{rem}	removal time n$\overline{SD}$, n$\overline{RD}$ to nCP	see Fig. 7	3.0 to 3.6	3.0	–	–	ns
t_{su}	set-up time nJ and n$\overline{K}$ to CP	see Fig. 6	3.0 to 3.6	2.5	–	–	ns
t_h	hold time nJ and n$\overline{K}$ to nCP	see Fig. 6	3.0 to 3.6	2.0	–	–	ns
f_{max}	maximum clock pulse frequency	see Fig. 6	3.0 to 3.6	150	–	–	MHz
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

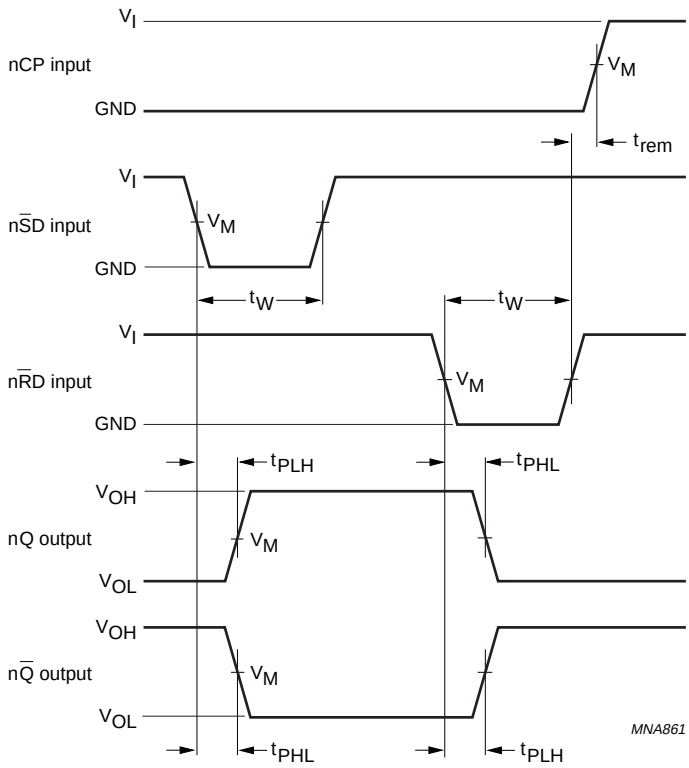
1. All typical values are measured at T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



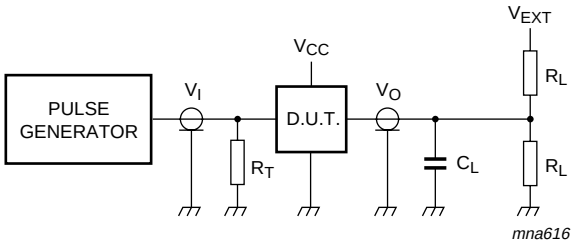
V_M = 1.5 V at $V_{CC} \geq 2.7$ V.
$V_M = 0.5V_{CC}$ at $V_{CC} < 2.7$ V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.6 Clock input (nCP) to output (nQ and n$\overline{Q}$) propagation delays, the clock pulse width, the nJ and n$\overline{K}$ to nCP set-up, the nCP to nJ and n$\overline{K}$ hold times and the maximum clock pulse frequency.



V_M = 1.5 V at $V_{CC} \geq 2.7$ V.
$V_M = 0.5V_{CC}$ at $V_{CC} < 2.7$ V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Set (n$\overline{S}$D) and reset (n$\overline{R}$D) input to output (nQ and n$\overline{Q}$) propagation delays, the set and reset pulse widths and the n$\overline{R}$D and n$\overline{S}$D to nCP removal time.



V_{CC}	V_I	C_L	R_L	V_{EXT}
				t_{PLH}/t_{PHL}
1.2 V	V_{CC}	50 pF	500 Ω[1]	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuit:

R_L = Load resistor.

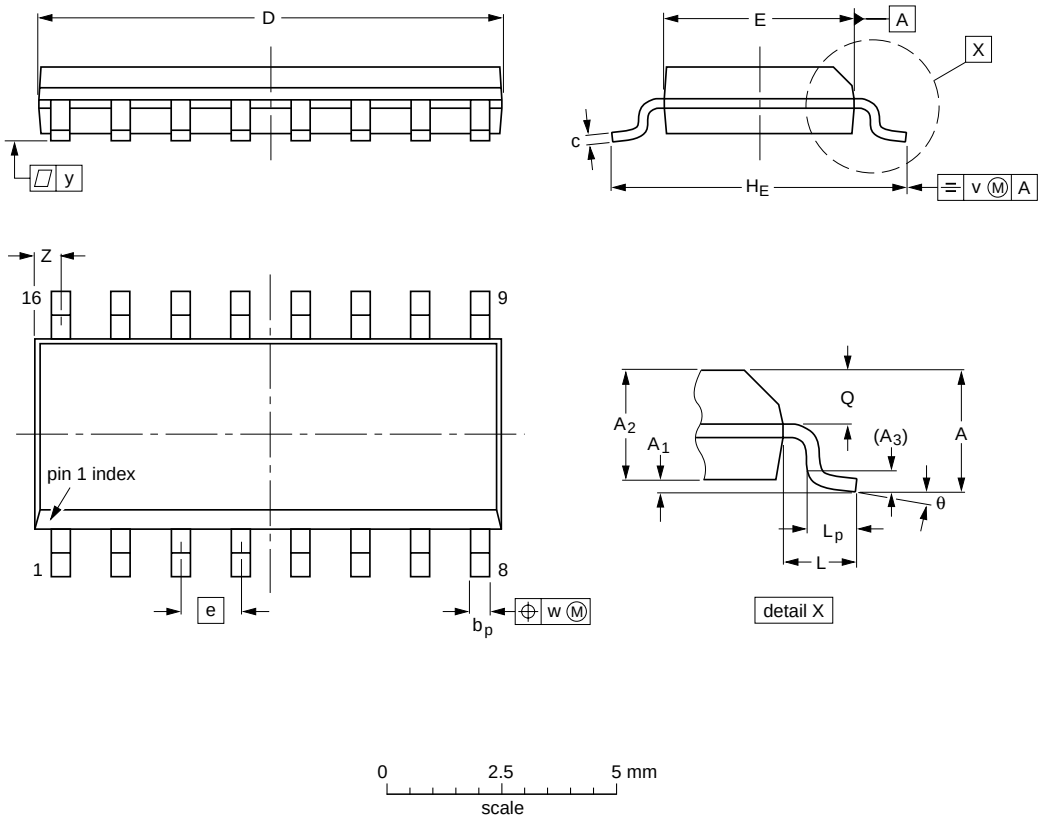
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

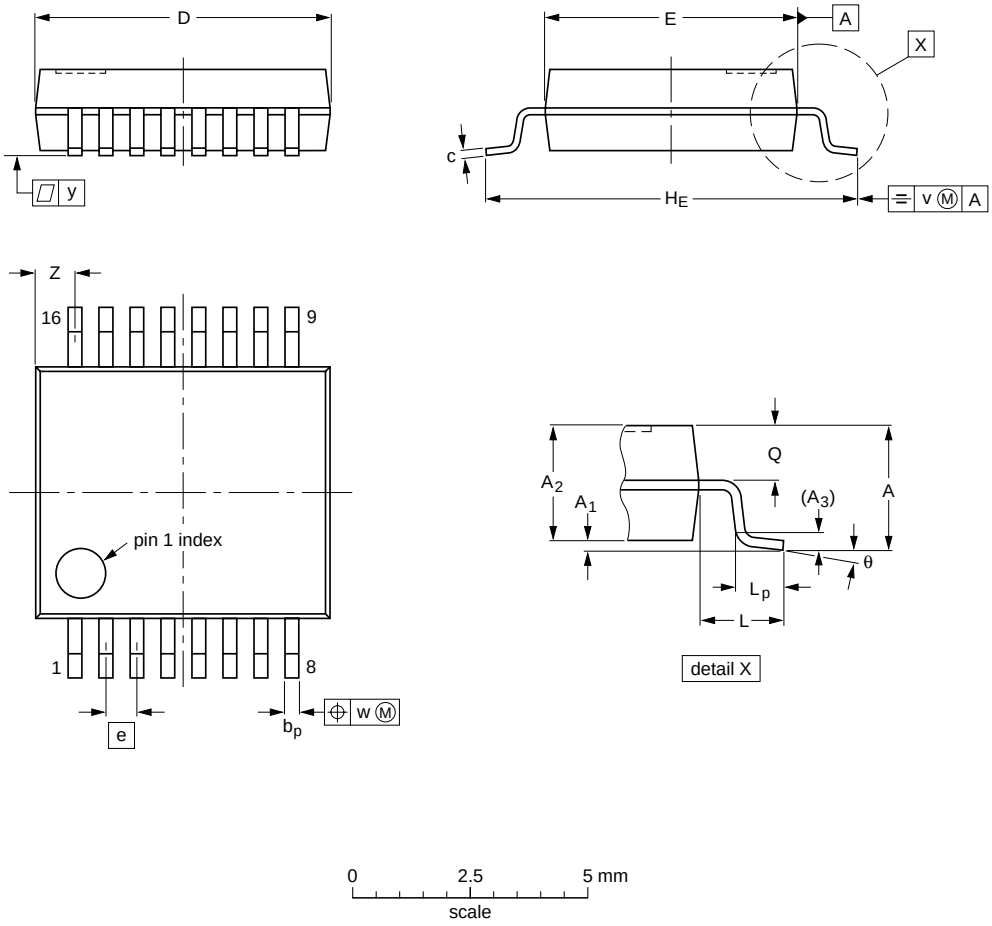
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

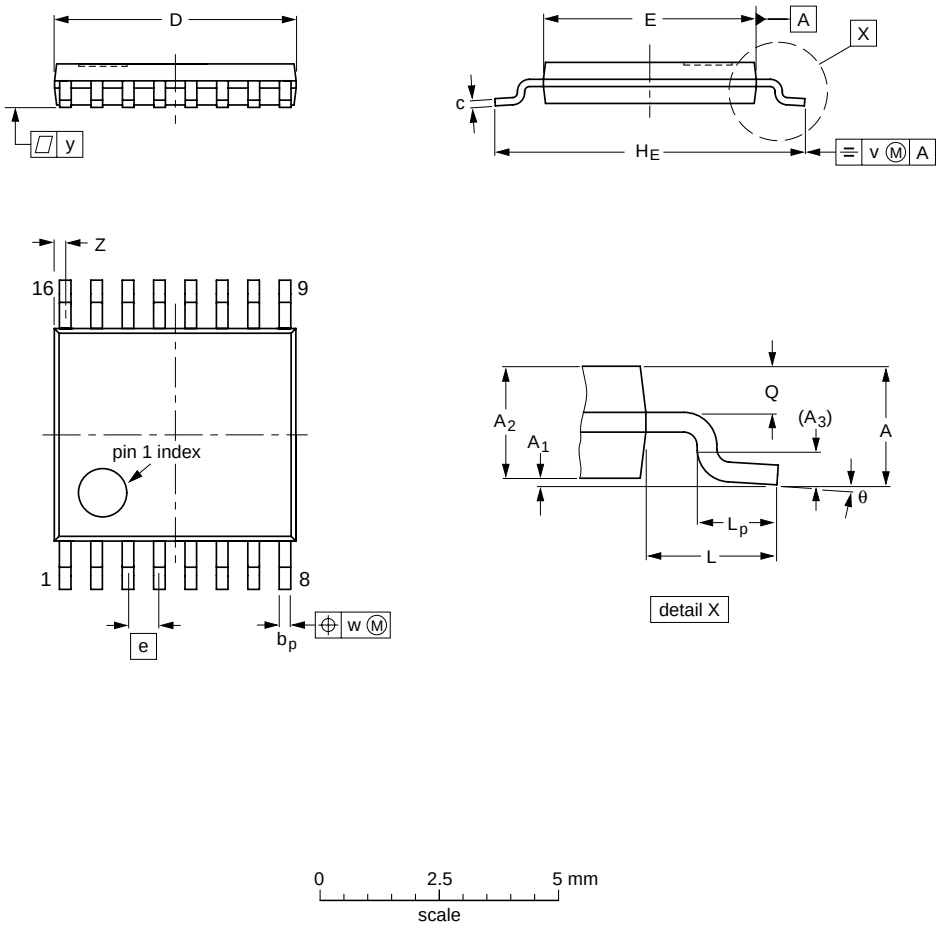
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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