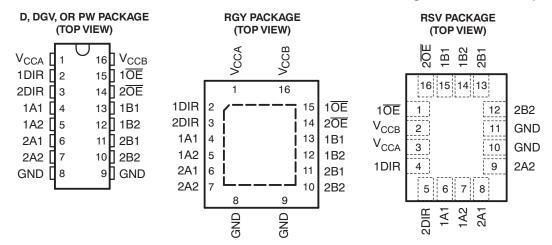
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#### **FEATURES**

- Control Inputs V<sub>IH</sub>/V<sub>IL</sub> Levels Are Referenced to V<sub>CCA</sub> Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- I<sub>off</sub> Supports Partial Power-Down-Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors

- Max Data Rates
  - 380 Mbps (1.8V to 3.3V Translation)
  - 200 Mbps (<1.8V to 3.3V Translation)</li>
  - 200 Mbps (Translate to 2.5V or 1.8V)
  - 150 Mbps (Translate to 1.5V)
  - 100 Mbps (Translate to 1.2V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### **DESCRIPTION/ORDERING INFORMATION**

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVCH4T245 is optimized to operate with  $V_{CCA}/V_{CCB}$  set at 1.4 V to 3.6 V. It is operational with  $V_{CCA}/V_{CCB}$  as low as 1.2 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCH4T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable  $(\overline{OE})$  input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74AVCH4T245 is designed so that the control pins (1DIR, 2DIR, 1OE, and 2OE) are supplied by V<sub>CCA</sub>.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then both ports are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PAC	KAGE <sup>(1)(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Tape and reel	SN74AVCH4T245RGYR	WS245
	QFN - RSV	Tape and reel	SN74AVCH4T245RSVR	ZWV
	SOIC - D	Tube	SN74AVCH4T245D	AVCH4T245
-40°C to 85°C	30IC - D	Tape and reel	SN74AVCH4T245DR	AVCH41245
	TSSOP – PW	Tube	SN74AVCH4T245PW	WS245
	1330F - PW	Tape and reel	SN74AVCH4T245PWR	W3243
	TVSOP - DGV	Tape and reel	SN74AVCH4T245DGVR	WS245

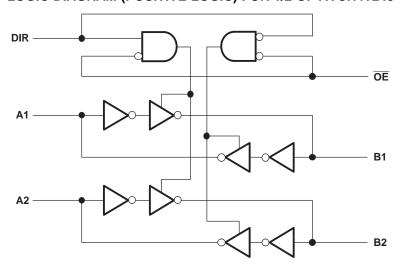
Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### FUNCTION TABLE<sup>(1)</sup> (EACH 2-BIT SECTION)

CONTRO	L INPUTS	OUTPUT (	CIRCUITS	OPERATION
ŌĒ	DIR	A PORT	B PORT	OPERATION
L	L	Enabled	Hi-Z	B data to A bus
L	Н	Hi-Z	Enabled	A data to B bus
Н	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

#### LOGIC DIAGRAM (POSITIVE LOGIC) FOR 1/2 OF AVCH4T245



<sup>(2)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CCA}$	Supply voltage range		-0.5	4.6	V
		I/O ports (A port)	-0.5	4.6	
$V_{I}$	Input voltage range <sup>(2)</sup>	I/O ports (B port)	-0.5	4.6	V
		Control inputs	-0.5	4.6	
V	Voltage range applied to any output	A port	-0.5	4.6	V
Vo	in the high-impedance or power-off state (2)	B port	-0.5	4.6	V
V	Voltage range applied to any output in the high or law state (2)(3)	A port	-0.5	V <sub>CCA</sub> + 0.5	V
Vo	Voltage range applied to any output in the high or low state (2)(3)	B port	-0.5	V <sub>CCB</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
		D package <sup>(4)</sup>		73	
		DGV package <sup>(4)</sup>		120	
$\theta_{JA}$	Package thermal impedance	PW package <sup>(4)</sup>		108	°C/W
		RGY package <sup>(5)</sup>		39	
		RSV package		184	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

The package thermal impedance is calculated in accordance with JESD 51-7.

The package thermal impedance is calculated in accordance with JESD 51-5.



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## Recommended Operating Conditions (1)(2)(3)(4)(5)

			V <sub>CCI</sub>	V <sub>cco</sub>	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage				1.2	3.6	V
$V_{CCB}$	Supply voltage				1.2	3.6	V
			1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65		
$V_{IH}$	High-level input voltage	Data inputs <sup>(4)</sup>	1.95 V to 2.7 V		1.6		V
	input voltage		2.7 V to 3.6 V		2		
			1.2 V to 1.95 V			$V_{CCI} \times 0.35$	
$V_{IL}$	Low-level input voltage	Data inputs <sup>(4)</sup>	1.95 V to 2.7 V			0.7	V
	input voltage		2.7 V to 3.6 V			0.8	
			1.2 V to 1.95 V		$V_{CCA} \times 0.65$		
$V_{IH}$	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.95 V to 2.7 V		1.6		V
	input voltago	(TOTOTOTIOGA TO VCCA)	2.7 V to 3.6 V		2		
			1.2 V to 1.95 V			$V_{CCA} \times 0.35$	
$V_{IL}$	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.95 V to 2.7 V			0.7	V
	input voltago	(TOTOTOTIOGA TO VCCA)	2.7 V to 3.6 V			0.8	
VI	Input voltage				0	3.6	V
Vo	Output voltage	Active state			0	$V_{CCO}$	V
VO	Output voltage	3-state			0	3.6	V
				1.2 V		-3	
				1.4 V to 1.6 V		-6	
I <sub>OH</sub>	High-level output cur	rrent		1.65 V to 1.95 V		-8	mA
				2.3 V to 2.7 V		-9	
				3 V to 3.6 V		-12	
				1.2 V		3	
				1.4 V to 1.6 V		6	
$I_{OL}$	Low-level output cur	rent		1.65 V to 1.95 V		8	mA
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δν	Input transition rise of	or fall rate				5	ns/V
T <sub>A</sub>	Operating free-air te	mperature			-40	85	°C

V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
 V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
 All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
 For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V.
 For V<sub>CCA</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V.

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## Electrical Characteristics (1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS	V	V	Т	<sub>A</sub> = 25°C		–40°C to 85	5°C	UNIT	
PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNII	
	I <sub>OH</sub> = -100 μA	1.2 V to 3.6 V	1.2 V to 3.6 V				V <sub>CCO</sub> - 0.2			
	$I_{OH} = -3 \text{ mA}$	1.2 V	1.2 V		0.95					
V	$I_{OH} = -6 \text{ mA}$ $V_I = V_{IH}$	1.4 V	1.4 V				1.05		V	
V <sub>OH</sub>	$I_{OH} = -8 \text{ mA}$ $V_I = V_{IH}$	1.65 V	1.65 V				1.2		V	
	$I_{OH} = -9 \text{ mA}$	2.3 V	2.3 V				1.75			
	$I_{OH} = -12 \text{ mA}$	3 V	3 V				2.3			
	I <sub>OL</sub> = 100 μA	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2		
	I <sub>OL</sub> = 3 mA	1.2 V	1.2 V		0.15					
V <sub>OL</sub>	$I_{OL} = 6 \text{ mA}$ $V_I = V_{IL}$	1.4 V	1.4 V					0.35	V	
OL	$I_{OL} = 8 \text{ mA}$	1.65 V	1.65 V					0.45	V	
	I <sub>OL</sub> = 9 mA	2.3 V	2.3 V					0.55		
	I <sub>OL</sub> = 12 mA	3 V	3 V					0.7		
I <sub>I</sub> DIR input	$V_I = V_{CCA}$ or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μΑ	
	V <sub>I</sub> = 0.42 V	1.2 V	1.2 V		25					
	$V_{I} = 0.49 V$	1.4 V	1.4 V				15			
I <sub>BHL</sub> <sup>(3)</sup>	V <sub>I</sub> = 0.58 V	1.65 V	1.65 V				25		μΑ	
	V <sub>I</sub> = 0.7 V	2.3 V	2.3 V				45			
	$V_{I} = 0.8 V$	3.3 V	3.3 V				100			
	$V_I = 0.78 \ V$	1.2 V	1.2 V		-25					
	$V_I = 0.91 \ V$	1.4 V	1.4 V				-15			
I <sub>BHH</sub> (4)	V <sub>I</sub> = 1.07 V	1.65 V	1.65 V				-25		μΑ	
	V <sub>I</sub> = 1.6 V	2.3 V	2.3 V				-45			
	V <sub>I</sub> = 2 V	3.3 V	3.3 V				-100			
		1.2 V	1.2 V		50					
		1.6 V	1.6 V				125			
I <sub>BHLO</sub> <sup>(5)</sup>	$V_I = 0$ to $V_{CCI}$	1.95 V	1.95 V				200		μΑ	
		2.7 V	2.7 V				300			
		3.6 V	3.6 V				500			
		1.2 V	1.2 V		-50					
		1.6 V	1.6 V				-125			
I <sub>BHHO</sub> <sup>(6)</sup>	$V_I = 0$ to $V_{CCI}$	1.95 V	1.95 V				-200		μΑ	
		2.7 V	2.7 V				-300			
		3.6 V	3.6 V				-500			

<sup>(1)</sup>  $V_{\text{CCO}}$  is the  $V_{\text{CC}}$  associated with the output port.

<sup>(2)</sup> V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

<sup>(3)</sup> The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

<sup>(4)</sup> The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

<sup>(5)</sup> An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

<sup>(6)</sup> An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

## SN74AVCH4T245 **4-BIT DUAL-SUPPLY BUS TRANSCEIVER**

# WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



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## **Electrical Characteristics**(1)(2)

over recommended operating free-air temperature range (unless otherwise noted) (continued)

DA	RAMETER	TEST CONDIT	ONC	V	V	Τ <sub>Δ</sub>	= 25°	С	–40°C to	85°C	UNIT
PA	KAWEIEK	TEST CONDIT	IONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNII
	A port	\\ or\\ \ 0 to 2.6\	,	0 V	0 V to 3.6 V		±0.1	±1		±5	
I <sub>off</sub>	B port	$V_I$ or $V_O = 0$ to 3.6 $V_I$	<b>,</b>	0 V to 3.6 V	0 V		±0.1	±1		±5	μA
I <sub>OZ</sub> <sup>(3)</sup>	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	OE = V <sub>IH</sub>	3.6 V	3.6 V		±0.5	±2.5		±5	
IOZ (°)	B port	$V_O = V_{CCO}$ or	OE =	0 V	3.6 V					±5	μA
	A port	GND, $V_I = V_{CCI}$ or GND	don't care	3.6 V	0 V					±5	
			,	1.2 V to 3.6 V	1.2 V to 3.6 V					8	
$I_{CCA}$		$V_I = V_{CCI}$ or GND,	$I_O = 0$	0 V	3.6 V					-2	μΑ
				3.6 V	0 V					8	
				1.2 V to 3.6 V	1.2 V to 3.6 V					8	
$I_{CCB}$		$V_I = V_{CCI}$ or GND,	$I_O = 0$	0 V	3.6 V					8	μΑ
				3.6 V	0 V					-2	
I <sub>CCA</sub> +	· I <sub>CCB</sub>	$V_I = V_{CCI}$ or GND,	I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					16	μΑ
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5	pF
C <sub>io</sub>	A or B port	$V_O = 3.3 \text{ V or GND}$		3.3 V	3.3 V		6			7	pF

#### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 1.2 \text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V ± 0.1 V	V <sub>CCB</sub> = 1.8 V ± 0.15 V	V <sub>CCB</sub> = 2.5 V ± 0.2 V	V <sub>CCB</sub> = 3.3 V ± 0.3 V	UNIT									
	(INFOI)	(001701)	TYP	TYP	TYP	TYP	TYP										
t <sub>PLH</sub>	А	В	3.4	2.9	2.7	2.6	2.8	9									
t <sub>PHL</sub>	А	В	3.4	2.9	2.7	2.6	2.8	ns									
t <sub>PLH</sub>	В	Α	3.6	3.1	2.8	2.6	2.6	5									
t <sub>PHL</sub>	ь	A	3.6	3.1	2.8	2.6	2.6	ns									
t <sub>PZH</sub>	ŌĒ	Α	5.6	4.7	4.3	3.9	3.7	5									
t <sub>PZL</sub>	OE	Α	5.6	4.7	4.3	3.9	3.7	ns									
t <sub>PZH</sub>	ŌĒ	В	5	4.3	3.9	3.6	3.6	20									
t <sub>PZL</sub>	OE	В	5	4.3	3.9	3.6	3.6	ns									
t <sub>PHZ</sub>	ŌĒ	^	6.2	5.2	5.2	4.3	4.8	5									
$t_{PLZ}$	OE	A	6.2	5.2	5.2	4.3	4.8	ns									
t <sub>PHZ</sub>	- OE	OE	В	5.9	5.1	5	4.7	5.5	20								
t <sub>PLZ</sub>			ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	В	5.9	5.1	5	4.7

 <sup>(1)</sup> V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
 (2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
 (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

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#### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA}$  = 1.5 V  $\pm$  0.1 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = ± 0.2		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT										
	(INPOT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX											
t <sub>PLH</sub>	Α	В	3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns										
t <sub>PHL</sub>	A	ь	3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	115										
t <sub>PLH</sub>	В	Α	3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns										
t <sub>PHL</sub>	ь	A	3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	115										
t <sub>PZH</sub>	ŌĒ	Α	4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	20										
t <sub>PZL</sub>	OE	A	4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns										
t <sub>PZH</sub>	ŌĒ	В	4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	2										
t <sub>PZL</sub>	OE	ь	4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns										
t <sub>PHZ</sub>	<del>oe</del>	^	5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	2										
t <sub>PLZ</sub>	ŌĒ	ŌĒ A	5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns										
t <sub>PHZ</sub>	ŌĒ	ŌĒ	ŌĒ	ŌĒ	<u> </u>	OE .	OE .	ŌĒ	OF	OE .	OE.	ŌE B	5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	20
t <sub>PLZ</sub>					D	5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns							

#### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{\text{CCA}}$  = 1.8 V  $\pm$  0.15 V (see Figure 1)

PARAMETER	FROM	TO	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1					V <sub>CCB</sub> = 2.5 V ± 0.2 V		$V_{CCB}$ = 3.3 V $\pm$ 0.3 V			
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>PLH</sub>	٨	В	2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9			
t <sub>PHL</sub>	Α	В	2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	ns		
t <sub>PLH</sub>	В	۸	3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5			
t <sub>PHL</sub>	В	Ь	ם	A	3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns
t <sub>PZH</sub>	<del>0</del> -	^	4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2			
t <sub>PZL</sub>	ŌĒ	ŌĒ A	4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	ns		
t <sub>PZH</sub>	<u> </u>	В	4.1	1.2	9.2	1	7.4	0.8	5.3	0.8	4.6			
t <sub>PZL</sub>	ŌĒ	В	4.1	1.2	9.2	1	7.4	0.8	5.3	0.8	4.6	ns		
touz	<u> </u>	ŌĒ A	5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7			
t <sub>PLZ</sub>	OĒ		5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	ns		
t <sub>PHZ</sub>	ŌĒ	В	5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9			
t <sub>PLZ</sub>		ŌĒ	ŌĒ	В	5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	ns

## SN74AVCH4T245 4-BIT DUAL-SUPPLY BUS TRANSCEIVER





#### **Switching Characteristics**

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over recommended operating free-air temperature range,  $V_{CCA}$  = 2.5 V  $\pm$  0.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO V <sub>CCB</sub> = 1.2 V			V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V						
	(INFUI)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX						
t <sub>PLH</sub>	А	В	2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	20					
t <sub>PHL</sub>	A	Ь	2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns					
t <sub>PLH</sub>	В	Α	2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	20					
t <sub>PHL</sub>	Б	A	2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns					
t <sub>PZH</sub>	ŌĒ	Α	4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8						
t <sub>PZL</sub>	OE	UE	OE	A	4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns			
t <sub>PZH</sub>	<u> </u>	В	3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	20					
t <sub>PZL</sub>	ŌĒ	В	3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns					
t <sub>PHZ</sub>	<del>∩E</del>	^	4.7	1	8.4	1	8.4	1	6.2	1	6.6	20					
t <sub>PLZ</sub>	ŌĒ	ŌĒ A —	4.7	1	8.4	1	8.4	1	6.2	1	6.6	ns					
t <sub>PHZ</sub>	<u> </u>	В	4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2						
t <sub>PLZ</sub>	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	В	4.5	1.5	8.8	1.3	8.2	1.1	6.2	0.9	5.2	ns

### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{\text{CCA}}$  = 3.3 V  $\pm$  0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = ± 0.2		V <sub>CCB</sub> = ± 0.3		UNIT												
	(INPOT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX													
t <sub>PLH</sub>	А	В	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	50												
t <sub>PHL</sub>	А	В	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns												
t <sub>PLH</sub>	В	Α	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	20												
t <sub>PHL</sub>	ь	A	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns												
t <sub>PZH</sub>	ŌĒ	^	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	50												
t <sub>PZL</sub>	OE	Α	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns												
t <sub>PZH</sub>	ŌĒ	В	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	20												
t <sub>PZL</sub>	OE	В	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns												
t <sub>PHZ</sub>	<del>oe</del>	^	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	20												
t <sub>PLZ</sub>	ŌĒ	OE A	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns												
t <sub>PHZ</sub>	<u> </u>	В	5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	20												
t <sub>PLZ</sub>	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	D	5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns

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## **Operating Characteristics**

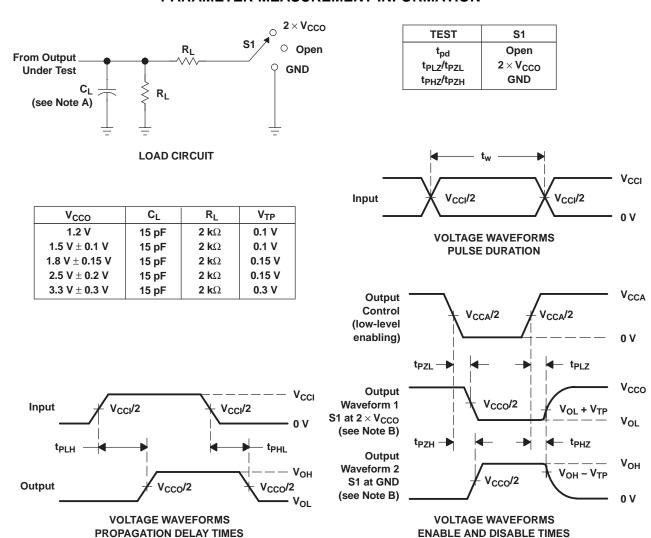
 $T_A = 25^{\circ}C$ 

F	PARAME	TER	TEST CONDITIONS	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	$V_{CCA} = V_{CCB} = 2.5 V$	$V_{CCA} = V_{CCB} = 3.3 V$	UNIT
	A to B	Outputs enabled		1	1	1	1.5	2	
C <sub>pdA</sub> <sup>(1)</sup>	AIOB	Outputs disabled	$C_L = 0,$ f = 10  MHz,	1	1	1	1	1	pF
O <sub>pd</sub> A ` /	B to A	Outputs enabled	$t_r = t_f = 1 \text{ ns}$	12	12.5	13	14	15	pΓ
	D IO A	Outputs disabled		1	1	1	1	1	
	A to B	Outputs enabled		12	12.5	13	14	15	
C (1)	АЮБ	Outputs disabled	$C_L = 0,$	1	1	1	1	1	~F
C <sub>pdB</sub> <sup>(1)</sup>	B to A	Outputs enabled	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	1	1	1	1	2	pF
	D IO A	Outputs disabled		1	1	1	1	1	

<sup>(1)</sup> Power dissipation capacitance per transceiver



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50~\Omega$ ,  $dv/dt \geq$  1 V/ns,  $dv/dt \geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

Figure 1. Load Circuit and Voltage Waveforms

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#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74AVCH4T245DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH4T245DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH4T245PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH4T245PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH4T245PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH4T245PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH4T245RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
74AVCH4T245RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74AVCH4T245DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH4T245RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74AVCH4T245RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## **PACKAGE OPTION ADDENDUM**

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#### OTHER QUALIFIED VERSIONS OF SN74AVCH4T245:

Enhanced Product: SN74AVCH4T245-EP

NOTE: Qualified Version Definitions:

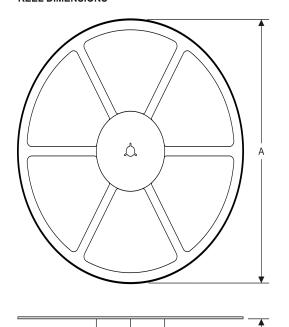
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

## PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

\*All dimensions are nominal

'All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH4T245DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AVCH4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVCH4T245PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVCH4T245RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVCH4T245RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

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\*All dimensions are nominal

All difficultions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH4T245DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AVCH4T245PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74AVCH4T245PWT	TSSOP	PW	16	250	346.0	346.0	29.0
SN74AVCH4T245RGYR	VQFN	RGY	16	3000	346.0	346.0	29.0
SN74AVCH4T245RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



## PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



## RGY (R-PVQFN-N16)

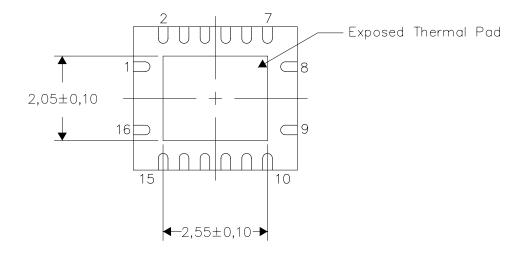
#### PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

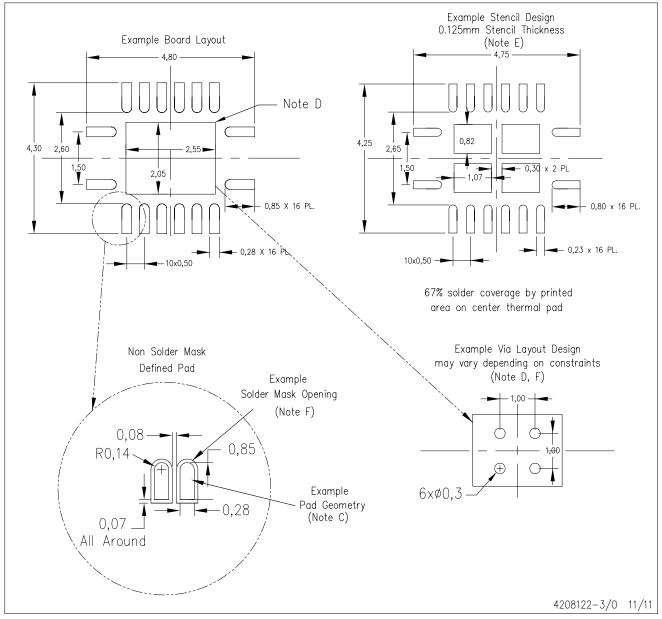
4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters



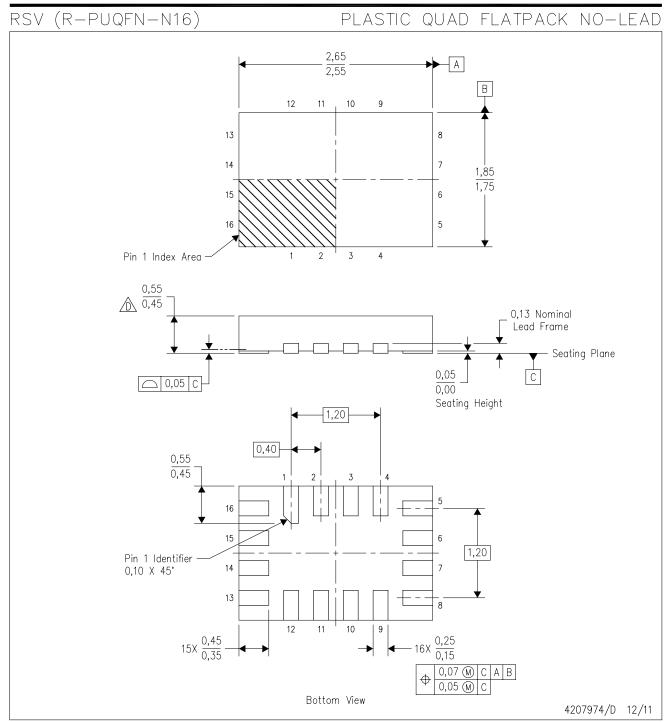
## RGY (R-PVQFN-N16)

## PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.





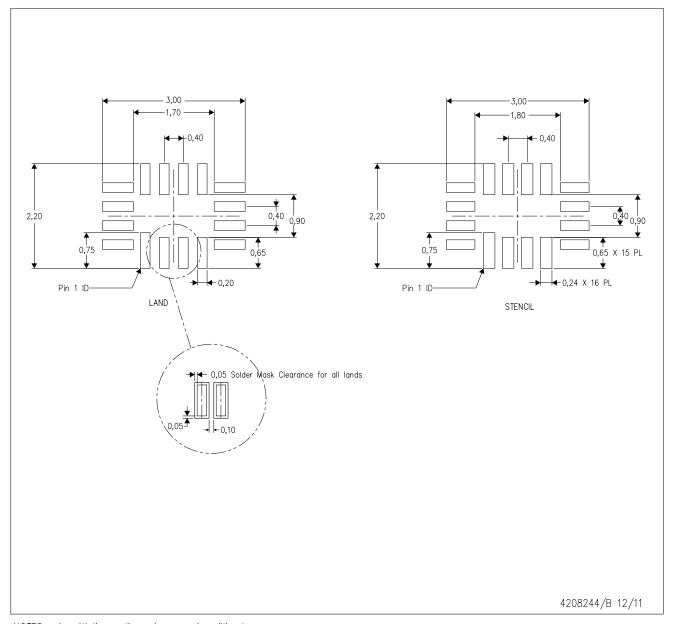
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.



## RSV (R-PUQFN-N16)

#### PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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