

MMC, SD CARD, Memory Stick™ VOLTAGE-TRANSLATION TRANSCEIVER AND LDO VOLTAGE REGULATOR WITH ESD PROTECTION AND EMI FILTERING

FEATURES

- Level Translator
 - V_{CCA} Range of 1.1 V to 3.6 V
 - Fast Propagation Delay (4 ns Max When Translating Between 1.8 V and 2.9 V)
- Low-Dropout (LDO) Regulator
 - 200-mA LDO Regulator With Enable
 - 2.9-V Output Voltage
 - 3.05-V to 5.5-V Input Voltage Range
 - Very Low Dropout: 200 mV at 200 mA

YFP PACKAGE (TOP VIEW)

	1	2	3	4
Α	()	()	()	()
В	(_)	$(\hat{\ })$	()	()
С	0	()	()	()
D	()	()	()	()
Е	\bigcirc	()	()	()

- ESD Protection Exceeds JESD 22 (A Port)
 - 2000-V Human-Body Model (A114-B)
 - 1000-V Charged-Device Model (C101)
- ±8-kV Contact Discharge IEC 61000-4-2 ESD (B Port)

TERMINAL ASSIGNMENTS

	1	2	3	4
Α	DAT2A	V _{CCA}	WP/CD	DAT2B
В	DAT3A	V_{BATT}	V _{CCB} O/P	DAT3B
С	CMDA	GND	GND	CMDB
D	DAT0A	CLKA	CLKB	DAT0B
E	DAT1A	CLK-f	EN	DAT1B

DESCRIPTION/ORDERING INFORMATION

The TXS0206-29 is a complete solution for interfacing microprocessors with MultiMediaCards (MMCs), secure digital (SD) cards, and Memory Stick™ cards. It is comprised of a high-speed level translator, a low-dropout (LDO) voltage regulator, IEC level ESD protection, and EMI filtering circuitry.

The voltage-level translator has two supply voltage pins. V_{CCA} can be operated over the full range of 1.1 V to 3.6 V. V_{CCB} is set at 2.9 V and is supplied by an internal LDO. The integrated LDO accepts input voltages from 3.05V to as high as 5.5 V and outputs 2.9 V, 200 mA to the B-side circuitry and to the external memory card. The TXS0206-29 enables system designers to easily interface low-voltage microprocessors to memory cards operating at 2.9 V.

Memory card standards recommend high-ESD protection for devices that connect directly to the external memory card. To meet this need, the TXS0206-29 incorporates ±8-kV Contact Discharge protection on the card side.

Since memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, set-top boxes, etc. Low static power consumption and small package size make the TXS0206-29 an ideal choice for these applications. The TXS0206-29 is offered in a 20-bump wafer chip scale package (WCSP). This package has dimensions of 1.96 mm \times 1.56 mm, with a 0.4-mm ball pitch for effective board-space savings

ORDERING INFORMATION(1)

T _A	PACKAG	E ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾	
-40°C to 85°C	WCSP - YFP (Pb-free)	Tape and reel	TXS0206-29YFPR	3 V 2	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) The actual top-side marking has three preceding characters to denote year, month, and sequence code.



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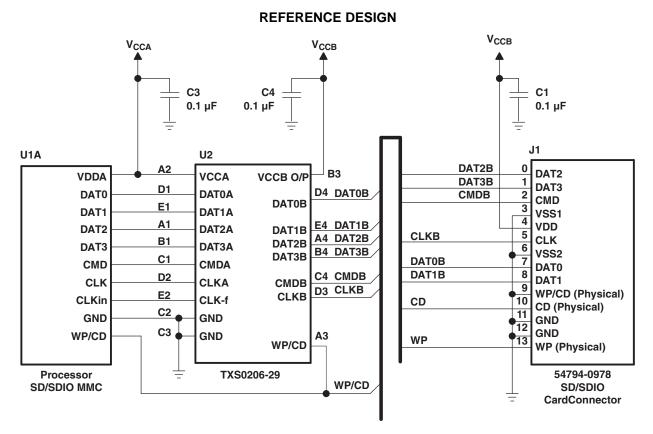


Figure 1. Interfacing With SD/SDIO Card

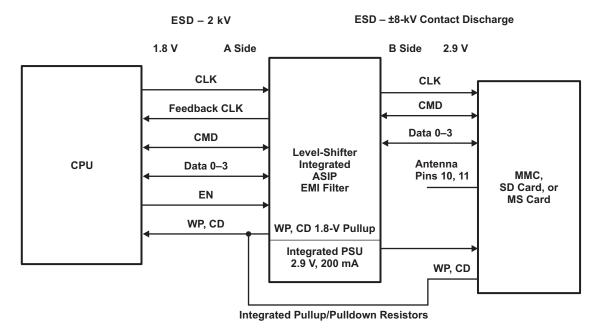


Figure 2. Typical Application Circuit



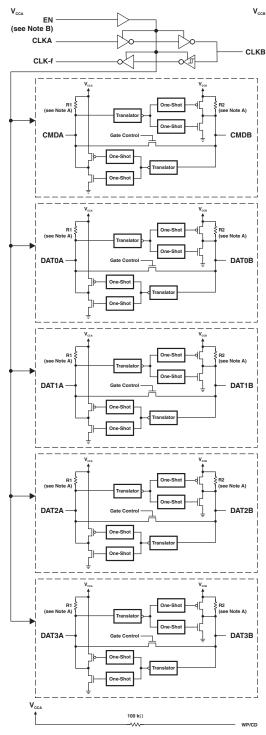
Table 1. LOGIC TABLE

EN	LDO	TRANSLATOR I/Os
L	Disabled	Disabled, pulled to V_{CCA} , V_{CCB} O/P through R_1 and R_2 at $70 k\Omega$ pullup resistors respectively
Н	Active	Active

TERMINAL FUNCTIONS

٦	ΓERMINAL		DECODIDETON
NO.	NAME	TYPE	DESCRIPTION
A1	DAT2A	I/O	Data bit 2 connected to host. Referenced to V _{CCA} . Includes R ₁ pullup resistor to V _{CCA} (see Note A).
A2	V _{CCA}	Power	A-port supply voltage. V _{CCA} powers all A-port I/Os and control inputs.
А3	WP/CD	Output	Connected to write protect on the mechanical connector. The WP pin has an internal 100-k Ω pullup resistor to V_{CCA} .
A4	DAT2B	I/O	Data bit 2 connected to memory card. Referenced to $V_{CCB}O/P$. Includes R_2 pullup resistor to $V_{CCB}O/P$ (see Note A).
B1	DAT3A	I/O	Data bit 3 connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
B2	V_{BATT}	Input	LDO input voltage from Battery-Supply
В3	V _{CCB} O/P	Output	LDO output voltage and B-port supply voltage. V _{CCB} O/P powers all B-port I/Os.
B4	DAT3B	I/O	Data bit 3 connected to memory card. Referenced to $V_{CCB}O/P$. Includes R_2 pullup resistor to $V_{CCB}O/P$ (see Note A).
C1	CMDA	I/O	Command bit connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
C2, C3	GND		Ground
C4	CMDB	I/O	Command bit connected to memory card. Referenced to $V_{CCB}O/P$. Includes R_2 pullup resistor to $V_{CCB}O/P$ (see Note A).
D1	DAT0A	I/O	Data bit 0 connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
D2	CLKA	Input	Clock signal connected to host. Referenced to V _{CCA} .
D3	CLKB	Output	Clock signal connected to memory card. Referenced to V _{CCB} O/P.
D4	DAT0B	I/O	Data bit 0 connected to memory card. Referenced to $V_{CCB}O/P$. Includes R_2 pullup resistor to $V_{CCB}O/P$ (see Note A).
E1	DAT1A	I/O	Data bit 1 connected to host. Referenced to V _{CCA} . Includes R ₁ pullup resistor to V _{CCA} (see Note A).
E2	CLK-f	Output	Clock feedback to host for resynchronizing data to a processor. Leave unconnected if not used.
E3	EN	Input	Enable/disable control. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to V _{CCA} .
E4	DAT1B	I/O	Data bit 1 connected to memory card. Referenced to $V_{CCB}O/P$. Includes R_2 pullup resistor to $V_{CCB}O/P$ (see Note A).





- A. R_1 and R_2 resistor values are determined based upon the logic level applied to the A port or B port as follows:
 - R_1 and R_2 = 40 k Ω when a logic level low is applied to the A port or B port.
 - R_1 and R_2 = 4 $k\Omega$ when a logic level high is applied to the A port or B port.
 - R_1 and R_2 = 70 k Ω when the port is deselected (or in High-Z or 3-state).
- B. EN controls all output buffers. When EN = low, all outputs are Hi-Z.

Figure 3. Logic Diagram

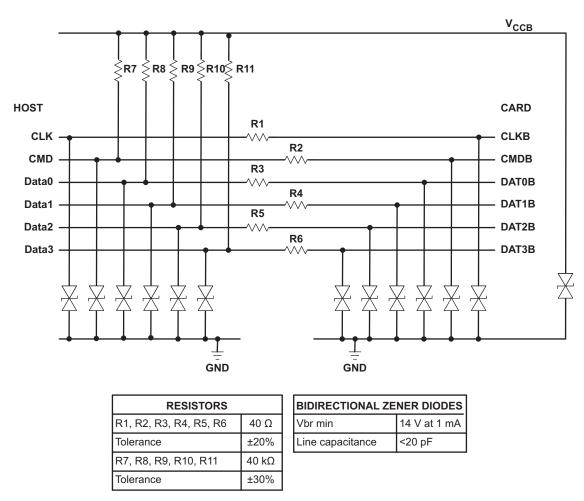


Figure 4. ASIP Block Diagram

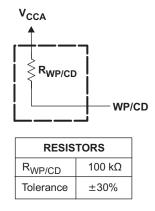


Figure 5. WP/CD Pullup Resistor



ABSOLUTE MAXIMUM RATINGS⁽¹⁾ Level Translator

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CCA}	Supply voltage range		-0.5	4.6	V	
		I/O ports (A port)	-0.5	4.6		
V_{I}	Input voltage range	I/O ports (B port)	-0.5	4.6	V	
		Control inputs	-0.5	4.6	ļ	
.,	Voltage range applied to any output in the high-impedance or	A port	-0.5	4.6 4.6 4.6 4.6 4.6 4.6 4.6 4.6 -50 -50 ±50 ±100	4.6	
v ₀	power-off state	B port	-0.5	4.6	V	
.,	Maltana and a see Paul to a see actual for the black on bounded.	A port	-0.5	4.6		
Vo	Voltage range applied to any output in the high or low state	B port	-0.5	4.6	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current	,		±50	mA	
	Continuous current through V _{CCA} or GND			±100	mA	
T _{stg}	Storage temperature range		-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

		TYP	UNIT
θ_{JA}	Package thermal impedance ⁽¹⁾	117	°C/W

⁽¹⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.3	6.5	V
V_{OUT}	Output voltage range	-0.3	4.6	V
	Peak output current		220	mA
	Continuous total power dissipation		TBD	mW
TJ	Junction temperature range	-55	150	°C
T _{stg}	Storage temperature range	- 55	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



RECOMMENDED OPERATING CONDITIONS⁽¹⁾ **Level Translator**

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT	
V _{CCA}	Supply voltage				1.1	3.6	V	
		A-Port CMD and	1.1 V to 1.95 V	201/	V _{CCI} - 0.2	V _{CCI}		
		DATA I/Os	1.95 V to 3.6 V	2.9 V	V _{CCI} - 0.4	V _{CCI}		
V_{IH}	High-level input voltage	B-Port and DATA	1.1 V to 1.95 V		V _{CCI} - 0.2	V _{CCI}	V	
		I/Os	1.95 V to 3.6 V	2.9 V	V _{CCI} - 0.4	3.6 V _{CCI} V _{CCI} V _{CCI} V _{CCI} V _{CCI} V _{CCI} O.15 0.15 0.15 0.15 V _{CCI} × 0.35 V _{CCO} -0.5 -1 -2 -4 -8 0.5 1 2 4 8 -8 8 8		
		OE and CLKA	1.1 V to 3.6 V		V _{CCI} × 0.65			
		A-Port CMD and	1.1 V to 1.95 V	0.014	0			
		DATA I/Os	1.95 V to 3.6 V	2.9 V	0	0.15		
V_{IL}	Low-level input voltage	B-Port CMD and	1.1 V to 1.95 V		0	0.15	V	
		DATA I/Os	1.95 V to 3.6 V	2.9 V	0	0.15		
		OE and CLKA	1.1 V to 3.6 V		0	$V_{CCI} \times 0.35$		
. ,	•	Active state					.,	
Vo	Output voltage	3-state			0	V _{CCO}	V	
		1	1.1 V to 1.3 V			-0.5		
			1.4 V to 1.6 V			-1		
I _{OH}	Output voltage 3-state 1.1 V to 1.3 V		-2	mA				
			2.3 V to 2.7 V			V _{CCI} 0.15 0.15 0.15 0.15 0.15 V _{CCO} -0.5 -1 -2 -4 -8 0.5 1 2 4 8 -8 8 5	-4	
			3 V to 3.6 V					
			1.1 V to 1.3 V			0.5		
			1.4 V to 1.6 V		1			
I _{OL}	Low-level output current	(CLK-f output)	1.65 V to 1.95 V	2.9 V		2	mA	
			2.3 V to 2.7 V			4		
			3 V to 3.6 V			8		
I _{OH}	High-level output current	(CLK output)		2.9 V		-8	mA	
I _{OL}	Low-level output current	(CLK output)		2.9 V		8	mA	
Δt/Δν	Input transition rise or fal	l rate				5	ns/V	
T _A	Operating free-air tempe	rature			-40	85	°C	

⁽¹⁾ All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

RECOMMENDED OPERATING CONDITIONS LDO

		MIN	MAX	UNIT
I _{OUT(PK)}	Peak output current	200		mA
C _{OUT}	Output capacitance	1	100	μF
T_{J}	Operating junction temperature	-40	125	°C

ELECTRICAL CHARACTERISTICS Level Translator

over recommended operating free-air temperature range (unless otherwise noted)

F	PARAMETER	TEST CONDITI	ONS	V _{CCA}	V _{CCB} O/P	MIN	TYP ⁽¹⁾	MAX	UNIT
		I _{OH} = -100 μA		1.1 V to 3.6 V		$V_{CCA} \times 0.8$			
		$I_{OH} = -0.5 \text{ mA}$		1.1 V		0.8			
	A port	$I_{OH} = -1 \text{ mA}$		1.4 V		1.05			
	(CLK-f output)	$I_{OH} = -2 \text{ mA}$		1.65 V		1.2			
V_{OH}		$I_{OH} = -4 \text{ mA}$		2.3 V	2.9 V	1.75			V
		$I_{OH} = -8 \text{ mA}$		3 V		2.3			
	A port (DAT and CMD outputs)	I _{OH} = -20 μA		1.1 V to 3.6 V		V _{CCA} × 0.8			
		I _{OL} = 100 μA		1.1 V to 3.6 V			\	/ _{CCA} × 0.8	
		$I_{OL} = 0.5 \text{ mA}$		1.1 V				0.35	
	A port	$I_{OL} = 1 \text{ mA}$		1.4 V	201/			0.35	V
	(CLK-f output)	I _{OL} = 2 mA		1.65 V	2.9 V			0.45	V
		I _{OL} = 4 mA		2.3 V				0.55	
V_{OL}		I _{OL} = 8 mA		3 V				0.7	
		I _{OL} = 135 μA						0.4	
	A port (DAT and CMD outputs)	I _{OL} = 180 μA						0.4	
		I _{OL} = 220 μA		1.1 V to 3.6 V	2.9 V			0.4	V
		I _{OL} = 300 μA						0.4	
		I _{OL} = 400 μA						0.55	
	B port	I _{OH} = -100 μA			2.9 V	V _{CCB} O/P × 0.8			
V_{OH}	(CLK output)	$I_{OH} = -8 \text{ mA}$		1.1 V to 3.6 V		2.3			V
	B port (DAT output)	I _{OH} = -20 μA			2.9 V	V _{CCB} O/P × 0.8			
	CLKB output	I _{OL} = 100 μA		1.1 V to 3.6 V	2.9 V		٧	/ _{CCB} O/P × 0.8	V
	port	$I_{OL} = 8 \text{ mA}$						0.7	
.,		I _{OL} = 135 μA						0.4	
V_{OL}	B port	I _{OL} = 180 μA		_				0.4	
	(DAT and CMD	I _{OL} = 220 μA		1.1 V to 3.6 V	2.9 V			0.4	V
	outputs)	I _{OL} = 300 μA						0.4	
		I _{OL} = 400 μA						0.55	
I _I	Control inputs	$V_I = V_{CCA}$ or GND		1.1 V to 3.6 V	2.9 V			±1	μΑ
I_{CCA}		$V_I = V_{CCI}$ or GND, I	$I_0 = 0$	1.1 V to 3.6 V	2.9 V			6	μΑ
I_{CCB}	-	$V_I = V_{CCI}$ or GND,	I _O = 0	1.1 V to 3.6 V	2.9 V			5	μΑ
C _{io}	A port						5.5	6.5	pF
010	B port						15	17.5	P'
C _i	Control inputs	$V_I = V_{CCA}$ or GND					3.5	4.5	pF
٦	Clock input	TI - TOUR OF STREET					3	4	۲,

⁽¹⁾ All typical values are at $T_A = 25$ °C.



ELECTRICAL CHARACTERISTICS LDO

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITION:	S	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{BATT}	Input voltage			V _{OUT} + V _{DO}		5.5	V	
V	Output valtage	Nominal T _A = 25°C			2.9		V	
V _{OUT}	Output voltage	All conditions		2.75		3.05	V	
ΔV_{OUT}	Output voltage tolerance	Nominal T _A = 25°C			±3		%	
V_{DO}	Dropout voltage	I _{OUT} = 200 mA			200	250	mV	
		I _{OUT} = 0				40		
I _{GND}	Ground-pin current	I _{OUT} < 100 mA	2	200	μΑ			
		100 mA ≤ I _{OUT} ≤ 200 mA				400		
I _{OUT(SC)}	Short-circuit current	$R_L = 0 \Omega$			300		mA	
DCDD	Davis aventural ation watin	V _{IN} = 3.05 V, V _{OUT} = 2.9 V,	f = 1 kHz		50		dB	
PSRR	Power-supply rejection ratio	$C_{NR} = 0.01 \ \mu F, I_{OUT} = 200 \ mA$	f = 10 kHz		40] ub	
t _{STR}	Start-up time	V _{OUT} = 2.9 V, I _{OUT} = 200 mA, C ₀	_{DUT} = 2.2 μF			200	μs	

⁽¹⁾ All typical values are at $T_A = 25$ °C.

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCB} = 2.9 V ± 5% (unless otherwise noted)

	·		V _{CCA} = 1.2 V ± 0.1 V		V _{CCA} = 1.5 V ± 0.1 V		V _{CCA} = 1.8 V ± 0.15 V		V _{CCA} = 2.5 V ± 0.2 V		V _{CCA} = 3.3 V ± 0.3 V		Ī <u> </u>		
			MIN			MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT		
	Push-pull driving		40		60		60		60		60	Mhna			
Data rate	Command Ope	Open-drain driving		1		1		1		1		1	Mbps		
Data fate	Clock	Push-pull driving		60		60		60		60		60	MHz		
	Data			40		60		60		60		60	Mbps		
	Command	Push-pull driving	25		17		17		17		17		ns		
t _W Pulse duration	Command	Command	Command	Open-drain driving	1		1		1		1		1		μs
	Clock	Duch pull driving	8.3		8.3		8.3		8.3		8.3		ns		
	Data	Push-pull driving	25		17		17		17		17		ns		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCB} = 2.9 \text{ V} \pm 5\%$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _C = 1. ± 0.	2 V	V _{CCA} = 1.5 V ± 0.1 V		V _{CCA} = 1.8 V ± 0.15 V		V _{CCA} = 2.5 V ± 0.2 V		V _{CCA} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			Push-pull driving		10.8		6.1		4.6		3.7		3.8	
	CMDA	CMDB	Open-drain driving (H-to-L)	3.2	10.6	2.7	6.6	2.4	5.5	2.1	4.4	2	4.1	
			Open-drain driving (L-to-H)	71	175	83	180	89	201	98	249	101	233	
			Push-pull driving		12		6.8		5.2		4.1		3.4	
t _{pd}	CMDB	CMDA	Open-drain driving (H-to-L)	2.9	9.4	2.1	7.3	2	6.4	2	5.7	2.2	4.6	ns
			Open-drain driving (L-to-H)	77	243	87	214	93	215	99	261	105	248	
	CLKA	CLKB	Push-pull driving		11.7		6.2		4.7		3.7		3.5	
	DATxA	DATxB	Push-pull driving		11.1		6.2		4.7		3.7		3.7	
	DATxB	DATxA	i dan-pun unving		11.5		6.2		5		3.9		6.2	
	CLKA CLK-f	CLK-f	Push-pull driving		24.7		13		8.9		6.8		4.8	
t	ten EN B-port EN A-port	B-port	Push-pull driving		1		1		1		1		1	μs
ten		A-port	Push-pull driving		1		1		1		1		1	μο
t	EN	B-port	Push-pull driving		40		39		35		38		34	ns
t _{dis}	EN	A-port	Push-pull driving		40		38		38		38		36	113
	CMDA rise time		Push-pull driving	1.6	12.2	0.4	8.3	1.1	5.9	1.9	3.3	8.0	4.2	
4	CIVIDA	rise time	Open-drain driving	32	120	44	127	52	150	62	201	74	194	ns
t _{rA}	CLK-f	rise time	Push-pull driving	0.6	12.7	0.5	7.2	0.4	4.5	0.7	1.5	0.7	1.4	113
	DATxA	rise time	1 dan pan anving	1.6	11.6	0.6	8.4	1	6.3	1.8	4.2	1.1	3.3	
	CMDB	rise time	Push-pull driving	1.7	6.7	0.5	5.6	1	5.2	1.5	5.2	1.9	5	
t _{rB}	OWIDD	noc unic	Open-drain driving	66	214	71	196	73	184	76	214	79	185	ns
чВ	CLKB rise time		Push-pull driving	1.7	4.8	1.5	4.9	1.5	4.9	1.6	5	1.6	5.1	110
	DATxB	rise time	1 don pair driving	0.4	6.8	0.6	5	0.2	5.2	0.9	5.3	1	14	
	CMDA	fall time	Push-pull driving	0.8	4	8.0	2.3	0.2	3.1	0.3	1.5	1	2.3	
t _{fA}	ONDA	Tall time	Open-drain driving	1.6	3.9	1.6	3.7	1.6	3.7	1.6	3.7	1.6	3.9	ns
ча	CLK-f	fall time	Push-pull driving	1	4	0.4	6.8	0.1	1.5	0.3	2.8	0.6	1.3	113
	DATxA	fall time	T don pair arring	1	3.9	0.1	3.8	0.2	2.7	0.3	2.9	0.4	1.8	
	CMDR	fall time	Push-pull driving	1.5	4.5	1.4	5.4	1.6	5	1.6	5.6	0.8	6.3	
t _{fB}	CINDO		Open-drain driving	1	4.3	1	2.3	0.8	1.9	0.8	1.6	0.9	1.3	ns
чь	CLKB	fall time	Push-pull driving	1.6	4	1.6	4.1	1.7	4.2	1.7	4.5	0.9	5.1	ns
	DATxB	fall time	pan animig	1	4.8	2.3	4.3	0.8	4.9	0.2	4.9	0.8	6.9	
t _{SK(O)}		to-channel kew	Push-pull driving		1		1		1		1		1	ns
	Com	nmand	Push-pull driving		40		60		60		60		60	Mbps
Max data rate	Con	iuiiu	Open-drain driving		1		1		1		1		1	IVIDPS
ivian udia iale	C	lock	Push-pull driving		60		60		60		60		60	MHz
	D	ata	. son pan anving		40		60		60		60		60	Mbps



OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C, V_{CCB} = 2.9 \text{ V}$

	PARAMETI	-D	TEST							UNIT
	IANAMETEN		CONDITIONS	1.2 V	1.2 V 1.5 V 1.8 V		2.5 V	3 V	3.3 V	UNII
	A-port input, B-port output	CLK Enabled		15	15	15	15.7	17.1	17.1	
		DATA Enabled		6.3	6.4	6.5	6.5	6.5	6.5	
C _{pdA} ⁽¹⁾	B-port input, A-port output	DATA Enabled	$C_L = 0,$ f = 10 MHz,	12.5	12.3	12.3	12.5	14	14	pF
OpdA \	A-port input, B-port	CLK Disabled	$t_r = t_f = 1 \text{ ns}$	0.2	0.2	0.2	0.3	0.3	0.3	PΕ
	output	DATA Disabled		1.2	1.2	1.2	1.2	1.2	1.2	
	B-port input, A-port output	DATA Disabled		0.2	0.2	0.2	0.3	0.3	0.3	
	A-port input, B-port output	DATA Enabled		31.2	30.6	30.3	29.5	28.5	28.5	
	B-port input, A-port	CLK Enabled		28.1	27.2	27	26.9	27	27	
C (1)	output	DATA Enabled	$C_L = 0,$ f = 10 MHz.	12.9	12.8	12.9	13.2	13.2	13.2	pF
C _{pdB} ⁽¹⁾ A-port inpu B-port output	B-port	DATA Disabled	$t_r = t_f = 1 \text{ ns}$	0.6	0.5	0.5	0.5	0.5	0.6	pr
	B-port input,	CLK Disabled		0.6	0.5	0.5	0.5	0.5	0.6	
	A-port output	DATA Disabled		1.2	1.2	1.2	1	1	1	

⁽¹⁾ Power dissipation capacitance per transceiver

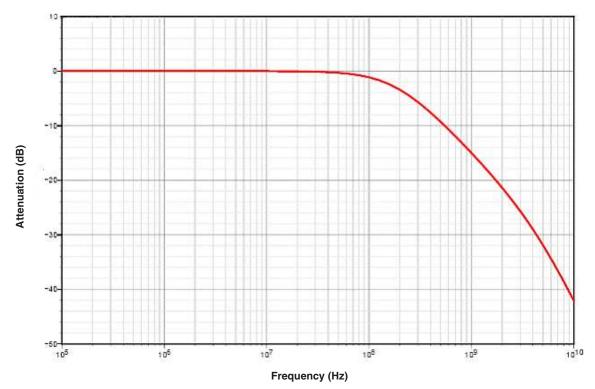


Figure 6. Typical ASIP EMI Filter Frequency Response

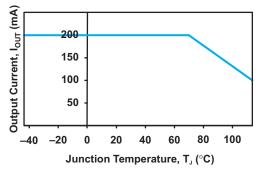
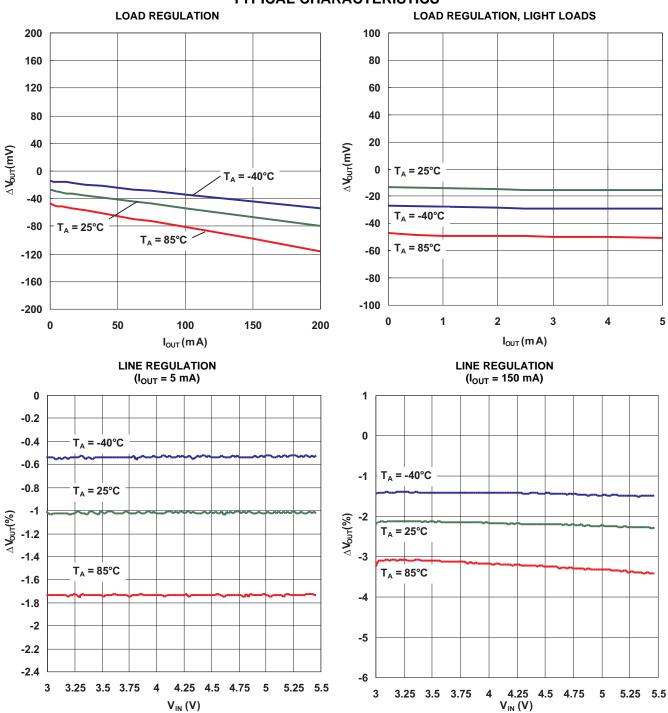


Figure 7. LDO Output Current Derating

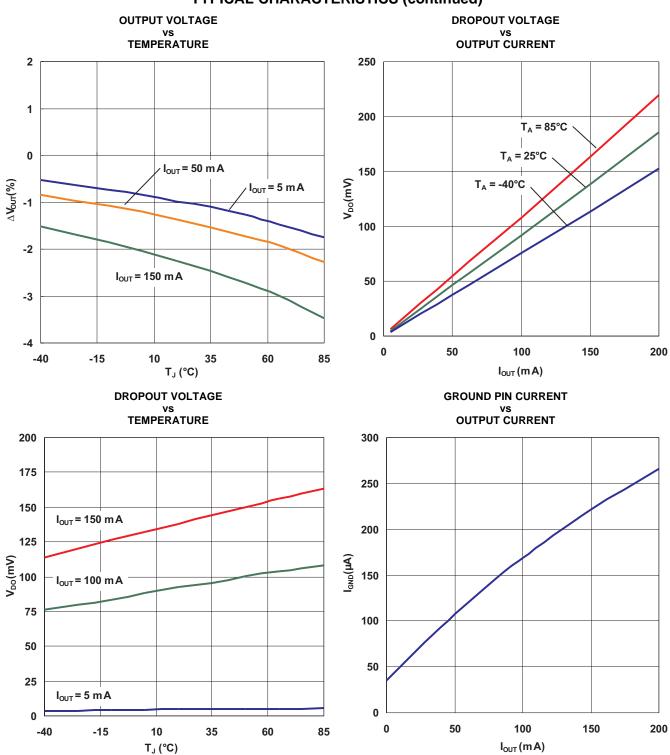








TYPICAL CHARACTERISTICS (continued)

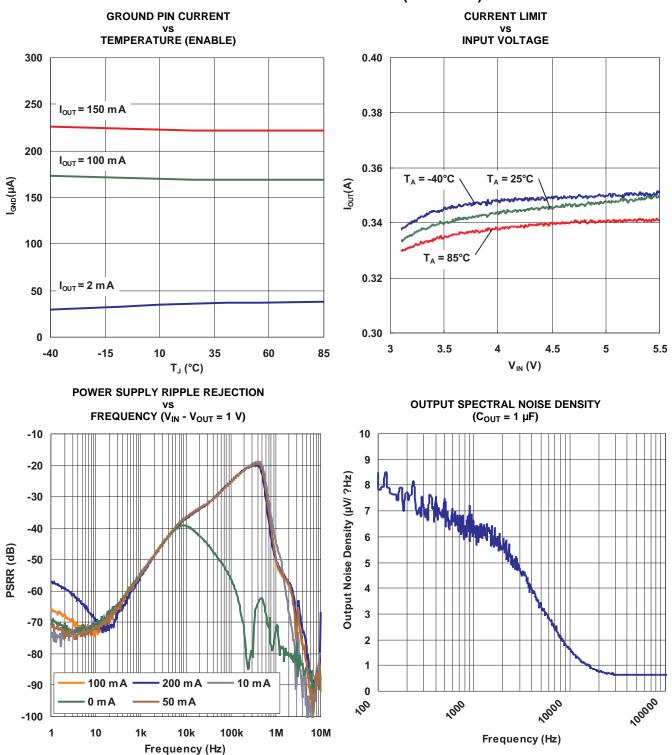




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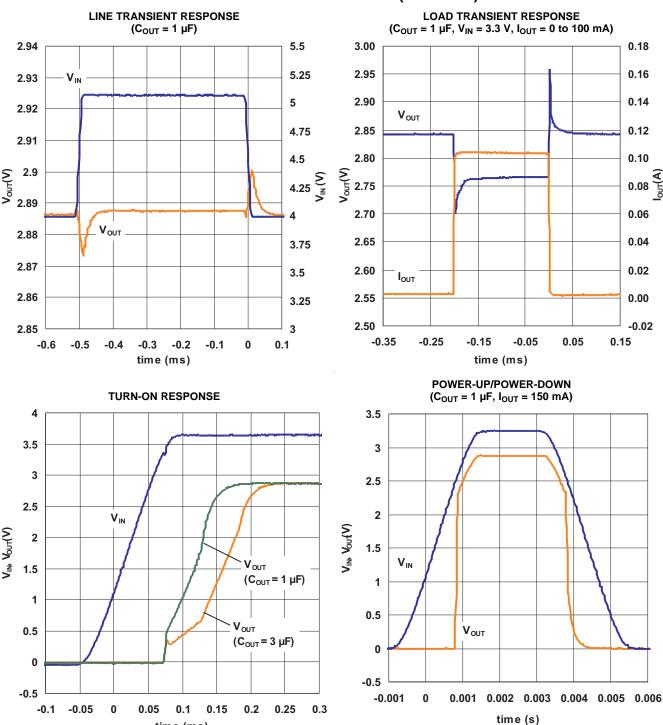
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TYPICAL CHARACTERISTICS (continued)





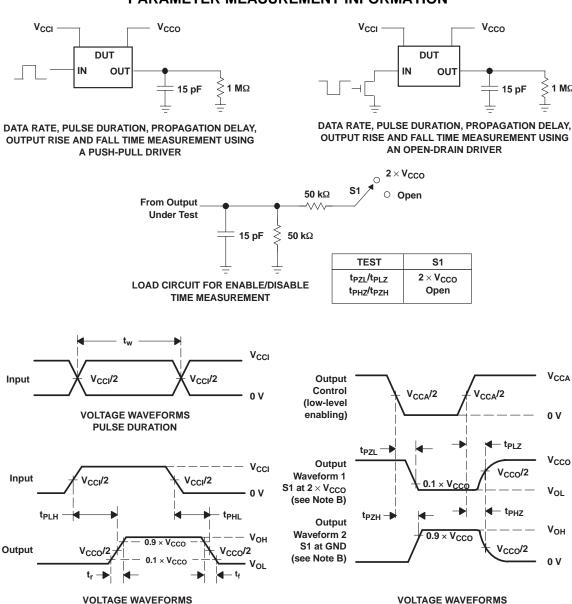
TYPICAL CHARACTERISTICS (continued)



time (ms)



PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

PROPAGATION DELAY TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $dv/dt \geq$ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 8. Load Circuit and Voltage WaveformsN

ENABLE AND DISABLE TIMES



PRINCIPLES OF OPERATION

Applications

The TXS0206-29 device is a complete application-specific voltage-translator designed to bridge the digital-switching compatibility gap and interface logic threshold levels between a micrprocessor with MMC, SD, and Memory Stick™ cards. It is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

Architecture

The CLKA, CLKB, and CLK-f subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength.

The SDIO lines comprise a semi-buffered auto-direction-sensing based translator architecture (see Figure 9) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

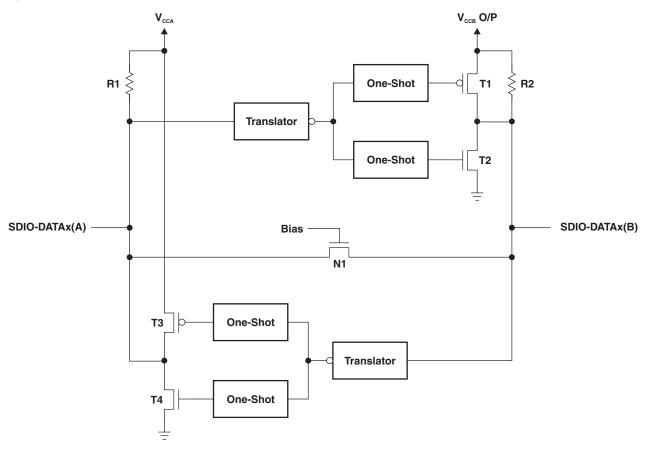


Figure 9. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the "switch-type" voltage translation function:

- 1. Integrated pullup resistors to provide dc-bias and drive capabilities
- 2. An N-channel pass-gate transistor topology (with a high R_{ON} of ~300 Ω) that ties the A-port to the B-port
- 3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports



For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high signal rising-edge, the O.S. circuits turn on the PMOS transistors (T_1 , T_3) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors (T_2 , T_4) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both High or both Low) for the one-shot to trigger again. In a DC state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the "smart pullup resistors" that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R_{PIJ1} and R_{PIJ2} values are a nominal 40 k Ω when the output is driving a low
- R_{PU1} and R_{PU2} values are a nominal 4 $k\Omega$ when the output is driving a high
- R_{PU1} and R_{PU2} values are a nominal 70 k Ω when the device is disabled via the EN pin or by pulling the either V_{CCA} or $V_{CCB}O/P$ to 0 V.

The reason for using these "smart" pullup resistors is to allow the TXS0206-29 to realize a lower static power consumption (when the I/Os are low), support lower V_{OL} values for the same size pass-gate transistor, and improved simultaneous switching performance.

Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level driver interfaced to the SDIO pins. Since the high bandwidth of these bidirectional SDIO circuits necessitates the need for a port to quickly change from an input to an output (and vice-vera), they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the smart pullup resistor values.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge rate and output impedance of the external device driving the SDIO I/Os, as well as the capacitive loading on these lines.

Similarly, the t_{pd} and max data rates also depend on the output impedance of the external driver. The values for t_{fA} , t_{fB} , t_{pd} , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω .

Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0206-29 SDIO output sees, so it is recommended that this lumped-load capacitance be considered and kept below 50 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.



When using the TXS0206-29 device with MMCs, SD, and Memory StickTM to ensure that a valid receiver input voltage high (V_{IH}) is achieved, the value of any pulldown resistors (external or internal to a memory card) must not be >10-k Ω value. The impact of adding too heavy a pulldown resistor (i.e. <10-k Ω value) to the data and command lines of the TXS0206-29 device and the resulting 4-k Ω pullup & 10-k Ω pulldown voltage divider network has a direct impact on the V_{IH} of the signal being sent into the memory card and its associated logic.

The resulting V_{IH} voltage for the 10-k Ω pulldown resistor value would be:

$$V_{CC} \times 10 \text{ k}\Omega / (10 \text{ k}\Omega + 4 \text{ k}\Omega) = 0.714 \times V_{CC}$$

This is marginally above a valid input high voltage for a 1.8-V signal (i.e., $0.65 \times V_{CC}$).

The resulting V_{IH} voltage for 20-k Ω pulldown resistor value would be:

$$V_{CC} \times 20 \text{ k}\Omega / (20 \text{ k}\Omega + 4 \text{ k}\Omega) = 0.833 \times V_{CC}$$

Which is above the valid input high voltage for a 1.8-V signal of 0.65 \times V_{CC}.

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PACKAGE OPTION ADDENDUM

4-Feb-2012

PACKAGING INFORMATION

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TXS0206-29YFPR	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TXS0206-29YFPRB	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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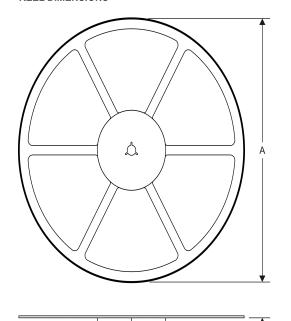
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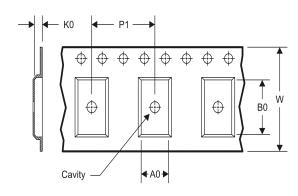
www.ti.com 3-Feb-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0206-29YFPR	DSBGA	YFP	20	3000	180.0	8.4	1.65	2.05	0.6	4.0	8.0	Q1
TXS0206-29YFPRB	DSBGA	YFP	20	3000	180.0	8.4	1.65	2.05	0.6	4.0	8.0	Q1

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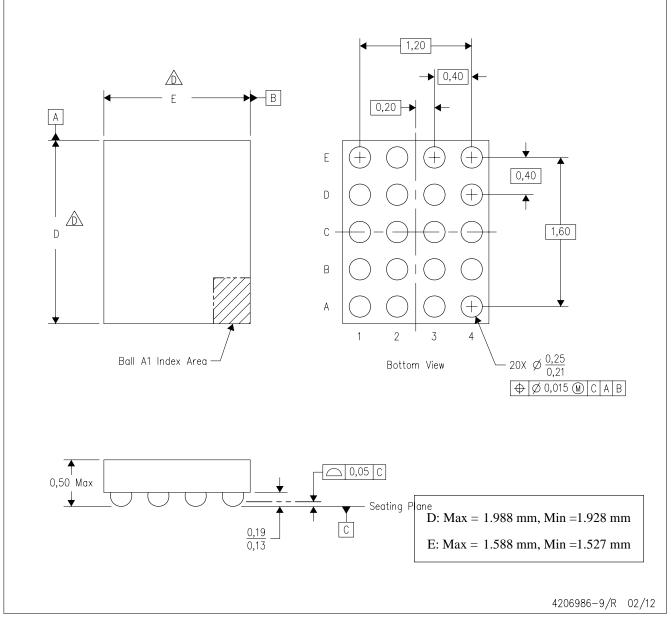


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0206-29YFPR	DSBGA	YFP	20	3000	220.0	220.0	34.0
TXS0206-29YFPRB	DSBGA	YFP	20	3000	220.0	220.0	34.0

YFP (R-XBGA-N20)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

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