D2661, APRIL 1982-REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of ~55°C to 125°C. The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

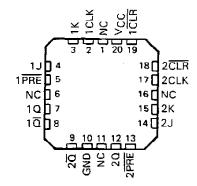
	INI	PUTS			ουπ	PUTS
PRE	CLR	CLK	J	K	a	Q
L	Н	X	Х	Х	Н	L
н	L	×	Х	X	L	Н
L	L	×	х	Х	Н [†]	H [†]
н	н	1	L	L	ΩO	₫₀
H	Н	1	Н	L	Н	L
Н	H	1	L	н	L	н
Н	Н	1	Н	н	TOG	GLE
Н	<u> H</u>	Н	_ X	х	αo	₫o

[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN54LS112A, SN54S112 . . . J OR W PACKAGE SN74LS112A, SN74S112A . . . D OR N PACKAGE (TOP VIEW)

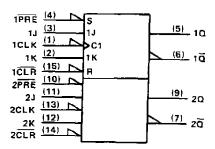
_	_		
1CLK[]1	\cup_{16}	□vcc
1K []2	15	1 CLR
1J[]3	14	2CLR
1PRE]4	13	2CLK
10[]5	12	<u></u> 2κ
10[]6	11	2J
20 [7	10	2PRE
GND [8	9	20

SN54LS112A, SN54S112...FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol‡

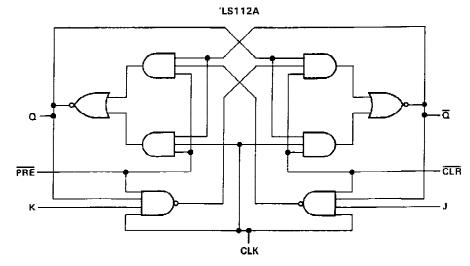


[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

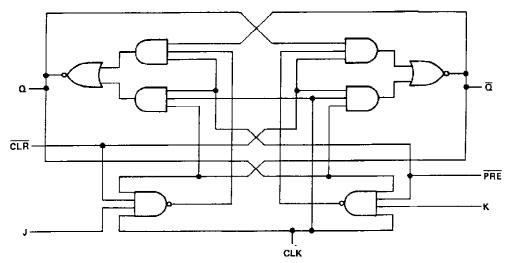
Pin numbers shown are for D, J, N, and W packages.

SN54LS112A, SN54S112, SN74LS112A, SN74S112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

logic diagrams (positive logic)

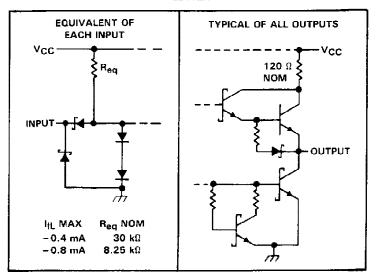


SN54S112, SN74LS112A

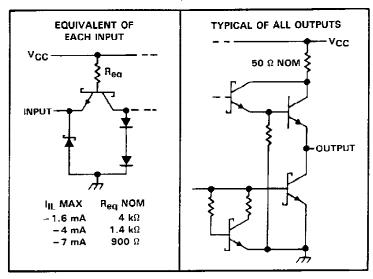


schematics of inputs and outputs

'LS112A



SN54S112, SN74S112A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V	
Input voltage: 'LS112A	7 V	
SN54LS112, SN74LS112A	5 V	
Operating free-air temperature range: SN54'	٥°C	
SN74') °C	
Storage temperature range65 °C to 150	°C	

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS112A, SN74LS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			SN	154LS11	2A	SN	74LS11	2A	LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	٧
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	٧
ЮН	High-level output current				-0.4			-0.4	mΑ
OL	Low-level output current				4			8	mA
fclock	Clock frequency		0		30	0		30	MHz
	Pulse duration	CLK high	20			20			
t _W	ruise duration	PRE or CLR low	25	-		25	<u></u>		ns
		Data high or low	20		**	20			
t _{su}	Set up time-before CLK↓	CLR inactive	25			25			ns
		PRE inactive	20			20			
th	Hold time-data after CLK1		0			0			Π\$
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	BANETER	TEST	CONDITIONS†		SN	154LS11	I2A	SI	174LS11	2A	LINIT
Ρ,	ARAMETER	IEST	CONDITIONS		MIN	TYP!	MAX	MIN	TYP‡	MAX	UNIT
v_{lK}		V _{CC} = MIN,	I _I = -18 mA				-1.5			1.5	V
Vон		V _{CC} = MIN, I _{OH} = -0.4 mA	$V_{IH} = 2 V$,	V _{IL} = MAX,	2.5	3.4		2.7	3.4		٧
.,		V _{CC} = MIN, I _{OL} = 4 mA	V _{IL} = MAX,	V _{IH} = 2 V,		0.25	0.4		0.25	0.4	· ·
VOL		V _{CC} = MIN, I _{OL} = 8 mA	$V_{IL} = MAX,$	V _{IH} = 2 V,					0.35	0.5	V
	J or K						0.1			0.1	
f _l	CLR or PRE	VCC = MAX,	$V_I = 7 V$				0.3			0.3	mA
	CLK						0.4			0.4	
	J or K						20			20	
ΉΗ	CLR or PRE	V _{CC} = MAX,	V_{\parallel} = 2.7 \vee		-		60			60	μА
	CLK						80			80	<u> </u>
1	J or K	Vcc = MAX,	Vi = 0 4 V				-0.4			-0.4	mA
ll .	All other	*CC = 1810011,	· · · · · · · · · · · · · · · · · · ·				-0.8			-0.8	
los §		VCC = MAX.	see Note 2		20		- 100	- 20		- 100	mΑ
ICC (T	otal)	V _{CC} = MAX,	see Note 3			4	6		4	6	mΑ

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_0 = 2.25 \text{ V}$ and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

^{3.} With all outputs open, ICC is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25 °C (see Note 4)

PARAMETER	FROM (INPUT)	TQ {OUTPUT)	TEST CO	TEST CONDITIONS				UNIT
fmax					30	45		MHz
t P LH	CLR. PRE or CLK	Q or Q	$R_L = 2 k\Omega$,	C _L = 15 pF		15	20	กร
†PHL	CLM, PRE OF CLK	2012				15	20	пs

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

SN54S112, SN74S112A DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			S	N54S1	12	SI	174611	2A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	DINIT
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
ViH	High-level input voltage	-	2			2			V
VIL	Low-level input voltage				0.8			0.8	٧
ЮН	High-level output current				- 1			– 1	mA
loL	Low-level output current				20			20	mA
		CLK high	6			6		.,,	
tw	Pulse duration	CLK low	6.5		- -	6.5			пѕ
		PRE or CLR low	8			8			
t _{su}	Set up time-before CLK↓	Data high or low	7			7			กร
th	Hold time-data after CLK↓		0			0			ns
TA	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETED	TECT	CONDITIONS		5	N54S1	2	SI	N74S11	2 A	UNIT
PA	RAMETER	IESI	CONDITIONS		MIN	TYP [‡]	MAX	MIN	TYP‡	MAX	UNIS
VIK		V _{CC} = MIN,	lj = -18 mA				-1.2			-1.2	٧
VoH		V _{CC} = MIN, I _{OH} = -1 mA	V _{IH} = 2 V,	VIL = MAX,	2.5	3.4		2.7	3.4		٧
VOL		V _{CC} = MIN, I _{OL} = 20 mA	V _{IH} = 2 V,	V _{IL} - 0.8 V,			0.5			0.5	V
I _I			V ₁ = 5.5 V				1			1	mA
1.	J or K	VCC = MAX.	V 27V				50			50	μА
ΉН	All other	T ACC = MINY	V = 2.7 V				100			100	μπ
	Jor K						-1.6			-1.6	
	CLR [§]],,	V 05V				-7			-7	mΑ
ΙΙΓ	PRE §	V _{CC} = MAX,	VI = 0.5 V			•	-7	1		-7	MA
	CLK	1					-4			- 4	
los¶		V _{CC} = MAX			-40	•	- 100	-40		~ 100	mA
ICC#		V _{CC} = MAX,	see Note 3			15	25		15	25	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§]Clear is tested with preset high and preset is tested with clear high.

Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

[#]Values are average per flip-flop.

NOTE 3: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, VCC = 5 V, TA = 25 °C (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				80	125		MHz
tPLH	PRE or CLR	Q or Q			4	7	ns
4	PRE or CLR (CLK high)	Ō or O	D. 200.0 0. 15 -5		5	7	
†PHL	PRE or CLR (CLK low)	a or a	$R_L = 280 \Omega$, $C_L = 15 pF$		5	7	ns
^t PLH	CLK	Q or $\overline{\mathbf{Q}}$			4	7	nŝ
tPHL .	CER	Q 01 Q			5	7	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
JM38510/07102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/07102BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30103B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30103BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30103BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/07102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/07102BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/30103B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30103BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/30103BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SN54LS112AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54S112J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74LS112AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS112AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS112ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS112ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS112ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS112ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S112AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74S112AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S112AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74S112ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54LS112AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS112AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS112AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54S112FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54S112J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54S112W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

25-Jan-2012

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS112A, SN74LS112A:

● Catalog: SN74LS112A

• Military: SN54LS112A

NOTE: Qualified Version Definitions:

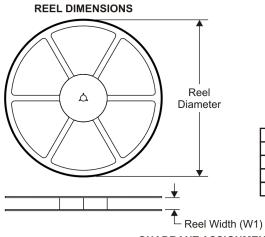
Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

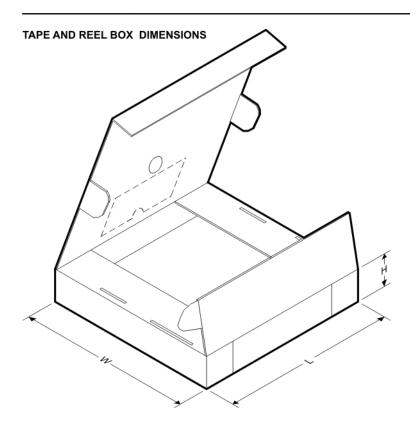


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS112ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS112ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS112ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS112ANSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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Applications

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