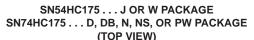
SN54HC175, SN74HC175 QUADRUPLE D-TYPE FLIP-FLOPS

WITH CLEAR

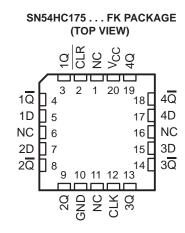
SCLS299D – JANUARY 1996 – REVISED SEPTEMBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Contain Four Flip-Flops With Double-Rail Outputs
- Typical t_{pd} = 13 ns



 \pm 4-mA Output Drive at 5 V

- Low Input Current of 1 μA Max
- Applications Include:
 Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators



NC - No internal connection

description/ordering information

These positive-edge-triggered D-type flip-flops have a direct clear (CLR) input. The 'HC175 devices feature complementary outputs from each flip-flop.

| TA | PACKA | GEŤ | ORDERABLE PART NUMBER | TOP-SIDE MARKING | | | | | | | | |
|----------------|------------|--------------|--------------------------|---------------------|--|--|--|--|--|--|--|--|
| | PDIP – N | Tube of 25 | SN74HC175N | SN74HC175N | | | | | | | | |
| | | Tube of 40 | SN74HC175D | | | | | | | | | |
| | SOIC – D | Reel of 2500 | SN74HC175DR | HC175 | | | | | | | | |
| | | Reel of 250 | SN74HC175DT | | | | | | | | | |
| –40°C to 85°C | SOP – NS | Reel of 2000 | SN74HC175NSR | HC175 | | | | | | | | |
| | SSOP – DB | Reel of 2000 | SN74HC175DBR | HC175 | | | | | | | | |
| | | Tube of 90 | SN74HC175PW | | | | | | | | | |
| | TSSOP – PW | Reel of 2000 | SN74HC175PWR | HC175 | | | | | | | | |
| | | Reel of 250 | SN74HC175PWT | | | | | | | | | |
| | CDIP – J | Tube of 25 | SNJ54HC175J | SNJ54HC175J | | | | | | | | |
| –55°C to 125°C | CFP – W | Tube of 150 | SNJ54HC175W | SNJ54HC175W | | | | | | | | |
| | LCCC – FK | Tube of 55 | SNJ54HC175FK | SNJ54HC175FK | | | | | | | | |

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



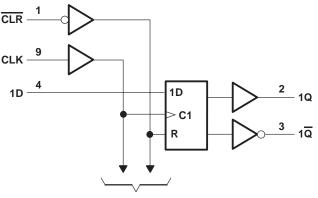
 $Copyright @ 2003, Texas Instruments Incorporated \\ On products compliant to MIL-PRF-38535, all parameters are tested \\ unless otherwise noted. On all other products, production \\ processing does not necessarily include testing of all parameters. \\ \label{eq:construction}$

description/ordering information (continued)

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

| | FUNCTION TABLE (each flip-flop) | | | | | | | | | | | |
|----------------|------------------------------------|---|----------------|------------------|--|--|--|--|--|--|--|--|
| INPUTS OUTPUTS | | | | | | | | | | | | |
| CLR | CLK | D | Q | Q | | | | | | | | |
| L | Х | Х | L | Н | | | | | | | | |
| н | \uparrow | Н | н | L | | | | | | | | |
| н | \uparrow | L | L | Н | | | | | | | | |
| н | L | Х | Q ₀ | \overline{Q}_0 | | | | | | | | |

logic diagram (positive logic)



To Three Other Channels

Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | -0.5 V to 7 V ote 1) |
|---|-------------------------|
| | ee Note 1) |
| | |
| Continuous current through V _{CC} or GND | ±50 mA |
| | backage |
| DE | package 67°C/W |
| N | backage 82°C/W |
| NS | package 64°C/W |
| PV | / package 108°C/W |
| Storage temperature range, T _{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



SN54HC175, SN74HC175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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recommended operating conditions (see Note 3)

| | | | SN | N54HC17 | ′ 5 | SN | 174HC17 | '5 | |
|-----------------------|---------------------------------|----------------------------|------|---------|------------|------|---------|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| VCC | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| | | $V_{CC} = 2 V$ | 1.5 | | | 1.5 | | | |
| VIH | High-level input voltage | $V_{CC} = 4.5 V$ | 3.15 | | | 3.15 | | | V |
| | | $V_{CC} = 6 V$ | 4.2 | | | 4.2 | | | |
| | | $V_{CC} = 2 V$ | | | 0.5 | | | 0.5 | |
| VIL | /II Low-level input voltage | $V_{CC} = 4.5 V$ | | | 1.35 | | | 1.35 | V |
| | | Λ CC = 6 Λ | | | 1.8 | | | 1.8 | |
| VI | Input voltage | | 0 | | VCC | 0 | | VCC | V |
| VO | Output voltage | | 0 | | VCC | 0 | | VCC | V |
| | | $V_{CC} = 2 V$ | | | 1000 | | | 1000 | |
| $\Delta t / \Delta v$ | Input transition rise/fall time | V _{CC} = 4.5 V | | | 500 | | | 500 | ns |
| | | V _{CC} = 6 V | | | 400 | | | 400 | |
| TA | Operating free-air temperature | ÷ | -55 | | 125 | -40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | 7507.00 | | | Т | A = 25°C | ; | SN54H | IC175 | SN74H | C175 | |
|-----------|-------------------------------------|---------------------------|------------|------|----------|------|-------|-------|-------|-------|------|
| PARAMETER | TEST CO | ONDITIONS | Vcc | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT |
| | | | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | |
| | | l _{OH} = -20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| VOH | $V_I = V_{IH} \text{ or } V_{IL}$ | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | V |
| | | $I_{OH} = -4 \text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| VOL | $V_{I} = V_{IH} \text{ or } V_{IL}$ | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL} = 4 \text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| lı | $V_I = V_{CC} \text{ or } 0$ | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| ICC | $V_I = V_{CC} \text{ or } 0,$ | IO = 0 | 6 V | | | 8 | | 160 | | 80 | μΑ |
| Ci | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |



SN54HC175, SN74HC175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | | T _A = | 25°C | SN54H | IC175 | SN74H | IC175 | |
|-----------------|---|-----------------|-------|------------------|------|-------|-------|-------|-------|------|
| | | | VCC | MIN | MAX | MIN | MAX | MIN | MAX | UNIT |
| | | | | | 6 | | 4.2 | | 5 | |
| fclock | Clock frequency | | 4.5 V | | 31 | | 21 | | 25 | MHz |
| | | | 6 V | | 36 | | 25 | | 29 | |
| | | | 2 V | 80 | | 120 | | 100 | | |
| | | CLR low | 4.5 V | 16 | | 24 | | 20 | | |
| | Pulse duration | | 6 V | 14 | | 20 | | 17 | | |
| tw | | | 2 V | 80 | | 120 | | 100 | | ns |
| | | CLK high or low | 4.5 V | 16 | | 24 | | 20 | | |
| | | | 6 V | 14 | | 20 | | 17 | | |
| | | | 2 V | 100 | | 150 | | 125 | | |
| | | Data | 4.5 V | 20 | | 30 | | 25 | | |
| | Catur time hafara CLIA | | 6 V | 17 | | 25 | | 21 | | |
| ^t su | Setup time before CLK↑ | | 2 V | 100 | | 150 | | 125 | | ns |
| | | CLR inactive | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | | 2 V | 0 | | 0 | | 0 | | |
| th | t _h Hold time, data after CLK↑ | | 4.5 V | 0 | | 0 | | 0 | | ns |
| | | | 6 V | 0 | | 0 | | 0 | | |

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| | FROM | то | | Т | _Δ = 25°C | ; | SN54H | IC175 | SN74H | IC175 | | | | | | | | | |
|------------------|---------|----------|-------|-----|---------------------|-----|-------|-------|-------|-------|-------|----|---|----|--|----|--|----|----|
| PARAMETER | (INPUT) | (OUTPUT) | VCC | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT | | | | | | | | |
| | | | 2 V | 6 | 12 | | 4.2 | | 5 | | | | | | | | | | |
| ^f max | | | 4.5 V | 31 | 50 | | 21 | | 25 | | MHz | | | | | | | | |
| | | | 6 V | 36 | 60 | | 25 | | 29 | | | | | | | | | | |
| | CLR | | 2 V | | 52 | 150 | | 255 | | 190 | | | | | | | | | |
| | | Any | 4.5 V | | 15 | 30 | | 45 | | 38 | | | | | | | | | |
| 4 | | | 6 V | | 13 | 26 | | 38 | | 32 | | | | | | | | | |
| ^t pd | | | 2 V | | 58 | 150 | | 255 | | 190 | ns | | | | | | | | |
| | CLK | Any | Any | Any | Any | Any | 4.5 V | | 16 | 30 | | 45 | | 38 | | | | | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | | | | | | | | | |
| | | | 2 V | | 38 | 75 | | 110 | | 90 | | | | | | | | | |
| tt | | Any | Any | Any | Any | Any | Any | Any | Any | Any | 4.5 V | | 8 | 15 | | 22 | | 19 | ns |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | | | | | | | | | |

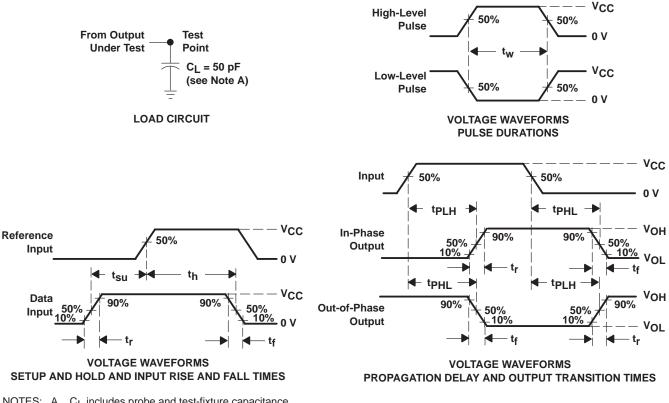
operating characteristics, $T_A = 25^{\circ}C$

| | PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----|---|-----------------|-----|------|
| Cpd | Power dissipation capacitance per flip-flop | No load | 30 | рF |



SN54HC175, SN74HC175 **QUADRUPLE D-TYPE FLIP-FLOPS** WITH CLEAR

SCLS299D - JANUARY 1996 - REVISED SEPTEMBER 2003



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CI includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns, t_f = 6 ns.
- C. For clock inputs, fmax is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 84089012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 8408901EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| 8408901FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Call TI | |
| JM38510/65308BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/65308BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/65308BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/65308BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54HC175J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74HC175D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |



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| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| SN74HC175NE4 | ACTIVE | PDIP | Ν | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC175NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWLE | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | |
| SN74HC175PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC175PWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54HC175FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54HC175J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54HC175W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



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⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54HC175, SN74HC175 :

• Catalog: SN74HC175

• Military: SN54HC175

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

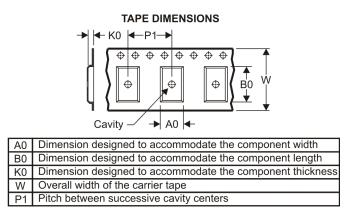
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74HC175DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC175NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC175PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC175PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

6-Aug-2010



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC175DBR | SSOP | DB | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74HC175DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC175NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74HC175PWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |
| SN74HC175PWT | TSSOP | PW | 16 | 250 | 346.0 | 346.0 | 29.0 |

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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