

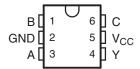
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

Check for Samples: SN74AUP1T97

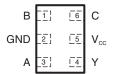
FEATURES

- Available in the Texas Instruments NanoStar™ Packages
- Single-Supply Voltage Translator
- 1.8 V to 3.3 V (at V_{CC} = 3.3 V)
- 2.5 V to 3.3 V (at $V_{CC} = 3.3 \text{ V}$)
- 1.8 V to 2.5 V (at V_{CC} = 2.5 V)
- 3.3 V to 2.5 V (at V_{CC} = 2.5 V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial-Power-Down Mode With Low Leakage Current (0.5 μA)
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SON (DRY or DSF), SOT-23 (DBV), SC-70 (DCK), and NanoStar WCSP
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Related Devices: SN74AUP1T98, SN74AUP1T57, and SN74AUP1T58

DBV OR DCK PACKAGE (TOP VIEW)



DRY OR DSF PACKAGE (TOP VIEW)



YFP OR YZP PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T97 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply.

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ($\Delta V_T = 210$ mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T97 can be easily configured to perform a required gate function by connecting A, B, and C inputs to V_{CC} or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.



 I_{off} is a feature that allows for powered-down conditions ($V_{CC} = 0$ V) and is important in portable and mobile applications. When $V_{CC} = 0$ V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T97 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
	NanoStar™ - WCSP (DSBGA) 0.23-mm Large Bump - YZP (Pb-free)	Reel of 3000	SN74AUP1T97YZPR	TH_
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP Reel of 3000 SN74/		SN74AUP1T97YFPR	TH_
-40°C to 85°C	QFN – DRY	Reel of 5000	SN74AUP1T97DRYR	TH
	uQFN – DSF	Reel of 5000	SN74AUP1T97DSFR	TH
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1T97DBVR	HT4_
	SOT (SC-70) - DCK	Reel of 3000	SN74AUP1T97DCKR	TH_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	5
2-input AND gate	6
2-input OR gate with one inverted input	7
2-input NAND gate with one inverted input	7
2-input AND gate with one inverted input	8
2-input NOR gate with one inverted input	8
2-input OR gate	9
Inverter	10
Noninverted buffer	11

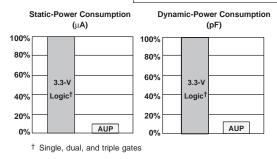


Figure 1. AUP - The Lowest-Power Family

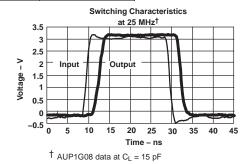


Figure 2. Excellent Signal Integrity



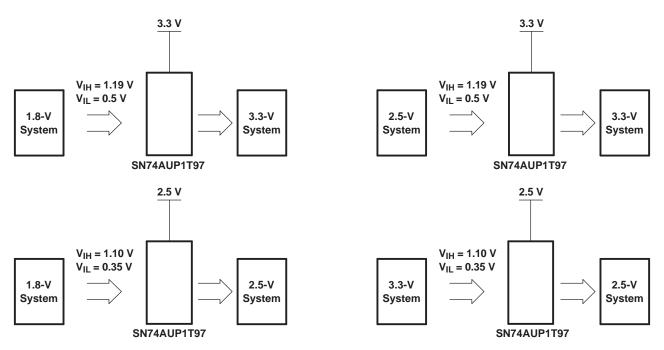


Figure 3. Possible Voltage-Translation Combinations

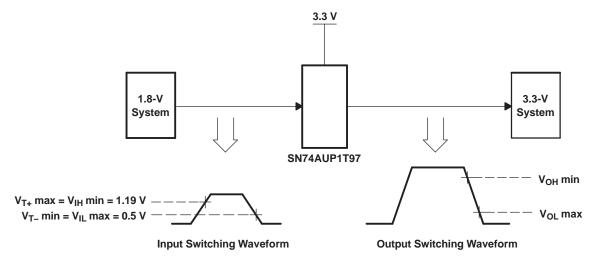


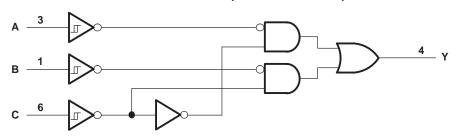
Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation



FUNCTION TABLE

	INPUTS		OUTPUT
С	В	Α	Υ
L	L	L	L
L	L	Н	L
L	Н	L	Н
L	Н	Н	Н
Н	L	L	L
Н	L	Н	Н
Н	Н	L	L
Н	Н	Н	Н

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC CONFIGURATIONS

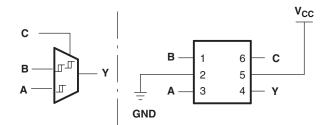


Figure 5. 157: 2-to-1 Data Selector/MUX When C is L, Y = B When C is H, Y = A

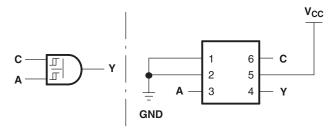


Figure 6. 08: 2-Input AND Gate



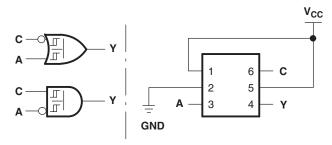


Figure 7. 14+32/14+00: 2-Input OR/NAND Gate With One Inverted Input

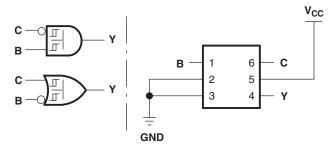


Figure 8. 14+08/14+02: 2-Input AND/NOR Gate With One Inverted Input

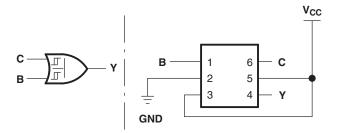


Figure 9. 32: 2-Input OR Gate

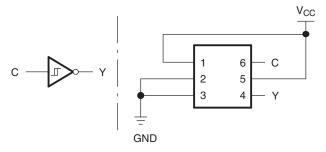


Figure 10. 04/14: Inverter



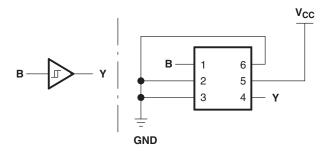


Figure 11. 17/34: Noninverted Buffer



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_{I}	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the hi	gh-impedance or power-off state ⁽²⁾	-0.5	4.6	V
Vo	Output voltage range in the high or low state	g(2)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current		±20	mA	
	Continuous current through V _{CC} or GND			±50	mA
		DBV package		165	
		DCK package		259	
0	Dealers theread is a dealer (3)	DRY package		340	00/14/
$\theta_{\sf JA}$	Package thermal impedance (3)	DSF package		300	°C/W
		YFP package		123	
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	V_{CC}	٧
	High level output ourrent	V _{CC} = 2.3 V		-3.1	۸ ۵۵
Іон	High-level output current	V _{CC} = 3 V		-4	mA
	Low level output ourrent	V _{CC} = 2.3 V		3.1	۸ ۵۵
I _{OL}	Low-level output current	V _{CC} = 3 V		4	mA
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Product Folder Link(s): SN74AUP1T97

²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{CC}	T _A =	= 25°C	T _A = -40 to 85°0		UNIT
				MIN	TYP MAX	MIN	MAX	
V_{T+}			2.3 V to 2.7 V	0.6	1.1	0.6	1.1	
	ve-going threshold e		3 V to 3.6 V	0.75	1.16	0.75	1.19	V
V_{T-}			2.3 V to 2.7 V	0.35	0.6	0.35	0.6	
Negative-going input threshold voltage			3 V to 3.6 V	0.5	0.85	0.5	0.85	V
ΔV_{T}			2.3 V to 2.7 V	0.23	0.6	0.1	0.6	
Hyste (V _{T+} -			3 V to 3.6 V	0.25	0.56	0.15	0.56	V
		I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1		
		$I_{OH} = -2.3 \text{ mA}$	2.3 V	2.05		1.97		
V_{OH}	V _{OH}	$I_{OH} = -3.1 \text{ mA}$	2.3 V	1.9		1.85		V
		$I_{OH} = -2.7 \text{ mA}$	3 V	2.72		2.67		
		$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55		
		I _{OL} = 20 μA	2.3 V to 3.6 V		0.1		0.1	
		I _{OL} = 2.3 mA	2.3 V		0.31		0.33	
V_{OL}		I _{OL} = 3.1 mA	2.5 V		0.44		0.45	V
		I _{OL} = 2.7 mA	3 V		0.31		0.33	
		I _{OL} = 4 mA	3 V		0.44		0.45	
I	All inputs	$V_I = 3.6 \text{ V or GND}$	0 V to 3.6 V		0.1		0.5	μΑ
$I_{\rm off}$		V_I or $V_O = 0$ V to 3.6 V	0 V		0.1		0.5	μΑ
ΔI_{off}		V_I or $V_O = 3.6 \text{ V}$	0 V to 0.2 V		0.2		0.5	μΑ
I_{CC}		$V_I = 3.6 \text{ V or GND}, I_O = 0$	2.3 V to 3.6 V		0.5		0.9	μΑ
ΔI_{CC}		One input at 0.3 V or 1.1 V, Other inputs at 0 or V_{CC} , $I_{O} = 0$	2.3 V to 2.7 V				4	μA
<u> </u>		One input at 0.45 V or 1.2 V, Other inputs at 0 or V_{CC} , $I_{O} = 0$	3 V to 3.6 V				12	μΛ
C_{i}		$V_I = V_{CC}$ or GND	3.3 V		1.5			pF
Co		$V_O = V_{CC}$ or GND	3.3 V		3			pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL	T _A = 25°C			T _A = -	UNIT	
			_	MIN	TYP	MAX	MIN	MAX	
		Υ	5 pF	1.8	2.3	2.9	0.5	6.8	
	A D C		10 pF	2.3	2.8	3.4	1	7.9	
t _{pd}	A, B, or C		15 pF	2.6	3.1	3.8	1	8.7	ns
				30 pF	3.8	4.4	5.1	1.5	10.8

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -	UNIT	
			_	MIN	TYP	MAX	MIN	MAX	
	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	
			10 pF	2.2	2.8	3.5	1	7.1	
t _{pd}			15 pF	2.6	3.2	5.2	1	7.9	ns
				30 pF	3.7	4.4	5.2	1.5	10

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -	UNIT	
			_	MIN	TYP	MAX	MIN	MAX	
		Υ	5 pF	2	2.7	3.5	0.5	5.5	
	A D == C		10 pF	2.4	3.1	3.9	1	6.5	
t _{pd}	A, B, or C		15 pF	2.8	3.5	4.3	1	7.4	ns
			30 pF	4	4.7	5.5	1.5	9.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL	Т,	T _A = 25°C			T _A = -40°C to 85°C		
			_	MIN	TYP	MAX	MIN	MAX		
		Y	5 pF	1.6	2	2.5	0.5	8	5	
	A D or C		10 pF	2	2.4	2.9	1	8.5		
t _{pd}	A, B, or C		15 pF	2.3	2.8	3.3	1	9.1	ns	
			30 pF	3.4	3.9	4.4	1.5	9.8		

SWITCHING CHARACTERISTICS

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over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	
			10 pF	2	2.3	2.7	1	6.1	
^t pd			15 pF	2.3	2.7	3.1	1	6.8	ns
			30 pF	3.4	3.8	4.2	1.5	8.5	

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{I} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			_	MIN	TYP	MAX	MIN	MAX	
	A, B, or C	Υ	5 pF	1.6	2.1	2.7	0.5	4.7	
			10 pF	2	2.4	3	1	5.7	
t _{pd}			15 pF	2.3	2.7	3.3	1	6.2	ns
			30 pF	3.4	3.8	4.4	1.5	7.8	

OPERATING CHARACTERISTICS

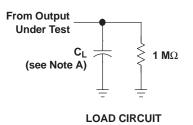
 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	4	5	pF

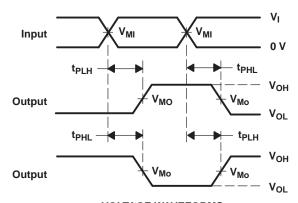
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PARAMETER MEASUREMENT INFORMATION



	V _{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V \pm 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _{MI}	V _I /2	V _I /2
V _{MO}	V _{CC} /2	V _{CC} /2



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \ \Omega$, slew rate \geq 1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 12. Load Circuit and Voltage Waveforms

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21-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AUP1T97DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1T97YEPR	OBSOLETE	WCSP	YEP	6		TBD	Call TI	Call TI	
SN74AUP1T97YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
SN74AUP1T97YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

21-Oct-2011

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

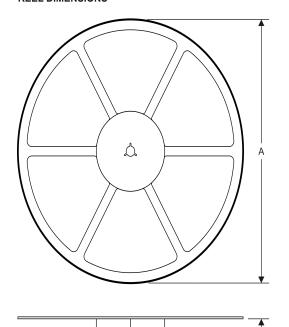
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 19-May-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T97DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T97DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T97DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.52	1.2	4.0	8.0	Q3
SN74AUP1T97DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74AUP1T97DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T97DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1T97YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1T97YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T97DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T97DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T97DCKR	SC70	DCK	6	3000	214.0	199.0	55.0
SN74AUP1T97DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T97DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T97DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1T97YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1T97YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.





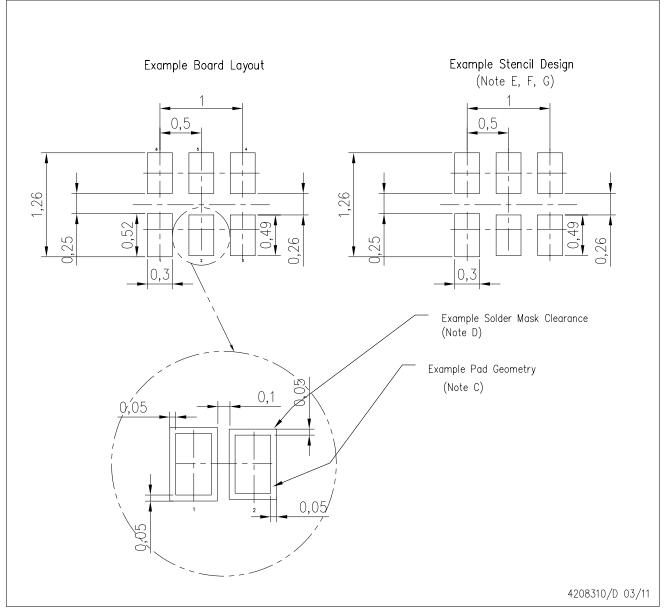
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- $frac{f}{K}$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



DRY (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC MO-287 variation X2AAF.





PLASTIC SMALL OUTLINE NO-LEAD



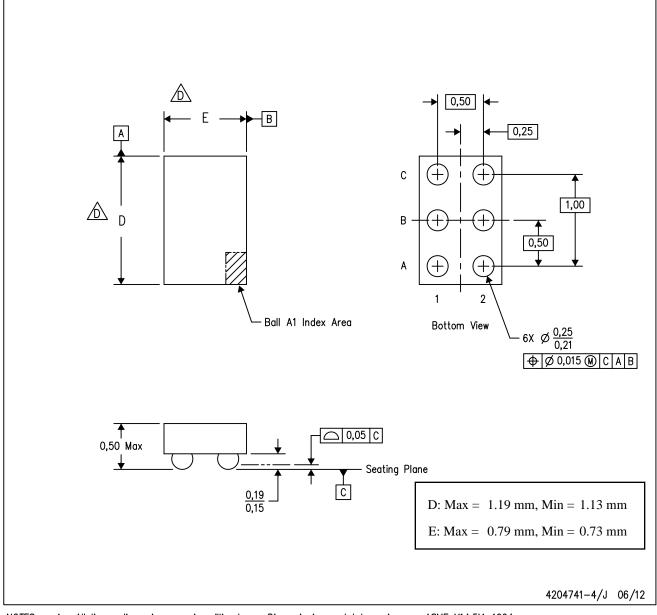
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

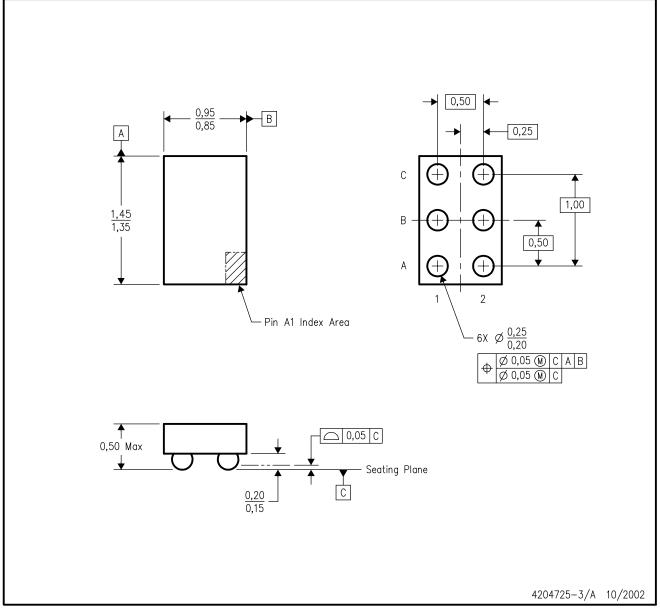
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



YEP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

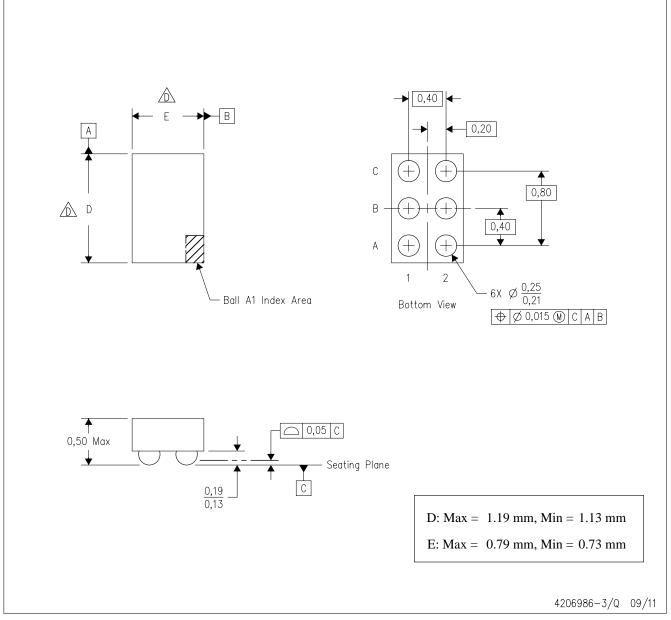
- B. This drawing is subject to change without notice.
- C. NanoStar \mathbf{M} package configuration.
- D. This package is tin-lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.



YFP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.

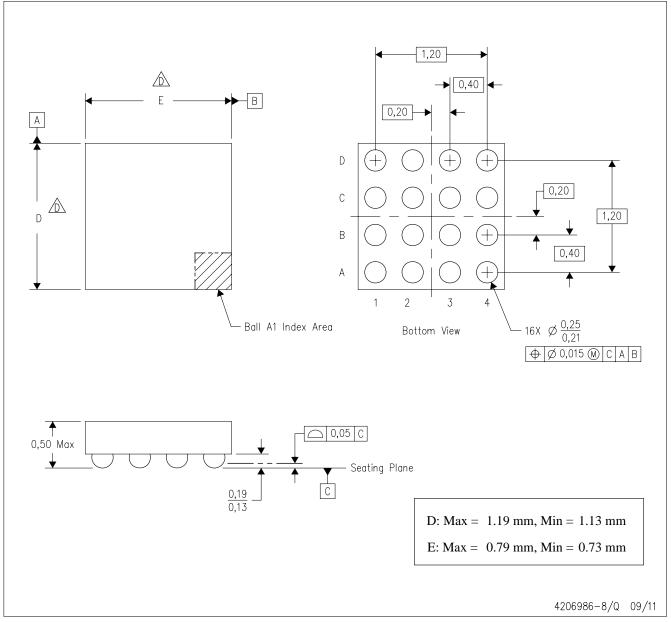
- E. Reference Product Data Sheet for array population. 2 x 3 matrix pattern is shown for illustration only.
- F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments



YFP (S-XBGA-N16)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.4 x 4 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments



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