## DATA SHEET

## 74LVC163

Presettable synchronous 4-bit binary counter; synchronous reset

## Presettable synchronous 4-bit binary counter; synchronous reset

## FEATURES

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B/JESD36
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Synchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock.
- ESD protection:
- HBM EIA/JESD22-A114-B exceeds 2000 V
- MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.


## DESCRIPTION

The 74LVC163 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC163 is a synchronous presettable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (pin CP). The outputs (pins Q0 to Q3) of the counters may be preset to a

HIGH-level or LOW-level. A LOW-level at the parallel enable input (pin $\overline{\mathrm{PE}}$ ) disables the counting action and causes the data at the data inputs (pins D0 to D3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (pins CEP and CET). A LOW-level at the master reset input (pin $\overline{\mathrm{MR}}$ ) sets all four outputs of the flip-flops (pins Q0 to Q3) to LOW-level after the next positive-going transition on the clock input (pin CP) (provided that the set-up and hold time requirements for PE are met). This action occurs regardless of the levels at input pins $\overline{P E}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.
The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (pins CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (pin TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH-level output of Q0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by $\mathrm{t}_{\text {PHL }}$ (propagation delay CP to TC) and $\mathrm{t}_{\text {su }}$ (set-up time CEP to CP) according to the
formula: $f_{\max }=\frac{1}{\mathrm{t}_{\mathrm{PHL}(\max )}+\mathrm{t}_{\text {su }}}$.

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QUICK REFERENCE DATA
GND $=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns}$.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
| :--- | :--- | :--- | :--- | :--- |
| t $_{\text {PHL }} / \mathrm{t}_{\text {PLH }}$ | propagation delay: |  |  |  |
|  | CP to Qn |  |  |  |
|  | CP to TC |  |  |  |
|  | CET to TC |  | 4.0 | ns |
|  |  |  | 3.6 | ns |
| $\mathrm{f}_{\text {clk }(\max )}$ | maximum clock frequency |  | 200 | $\mathrm{pF} \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$ |
| $\mathrm{C}_{\mathrm{l}}$ | input capacitance |  | 5.0 | pF |
| $\mathrm{C}_{\text {PD }}$ | power dissipation capacitance per gate | notes 1 and 2 | 17 | pF |

## Notes

1. $\mathrm{C}_{P D}$ is used to determine the dynamic power dissipation ( $\mathrm{P}_{\mathrm{D}}$ in $\mu \mathrm{W}$ ).
$P_{D}=C_{P D} \times V_{C C}{ }^{2} \times f_{i} \times N+\Sigma\left(C_{L} \times V_{C C}{ }^{2} \times f_{o}\right)$ where:
$\mathrm{f}_{\mathrm{i}}=$ input frequency in MHz ;
$\mathrm{f}_{\mathrm{o}}=$ output frequency in MHz ;
$\mathrm{C}_{\mathrm{L}}=$ output load capacitance in pF ;
$\mathrm{V}_{\mathrm{CC}}=$ supply voltage in Volts;
$\mathrm{N}=$ total load switching outputs;
$\Sigma\left(C_{L} \times V_{C C}^{2} \times f_{0}\right)=$ sum of the outputs.
2. The condition is $\mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ to $\mathrm{V}_{\mathrm{CC}}$.

ORDERING INFORMATION

| TYPE NUMBER | TEMPERATURE <br> RANGE | PINS | PACKAGE | MATERIAL | CODE |
| :--- | :---: | :---: | :---: | :---: | :---: |
| 74 LVC 163 D | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 | SO16 | plastic | SOT109-1 |
| 74LVC163DB | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 | SSOP16 | plastic | SOT338-1 |
| $74 \mathrm{LVC} 163 P W$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 | TSSOP16 | plastic | SOT403-1 |
| 74 LVC 163 BQ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 | DHVQFN16 | plastic | SOT763-1 |

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## FUNCTION TABLE

See note 1.

| OPERATING MODES | INPUT |  |  |  |  |  | OUTPUT |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{M R}$ | CP | CEP | CET | PE | Dn | Qn | TC |
| Reset (clear) | I | $\uparrow$ | X | X | X | X | L | L |
| Parallel load | h | $\uparrow$ | X | X | 1 | 1 | L | L |
|  | h | $\uparrow$ | X | X | I | h | H | * |
| Count | h | $\uparrow$ | h | h | h | X | count | * |
| Hold (do nothing) | h | X | 1 | X | h | X | $\mathrm{q}_{\mathrm{n}}$ | * |
|  | h | X | X | I | h | X | $\mathrm{q}_{\mathrm{n}}$ | L |

## Note

1.     * = the TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).
$\mathrm{H}=\mathrm{HIGH}$ voltage level.
$h=$ HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$\mathrm{q}=$ lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.

X = don't care.
$\uparrow=$ LOW-to-HIGH clock transition.

PINNING

| PIN | SYMBOL |  |
| :---: | :--- | :--- |
| 1 | $\overline{\text { MR }}$ | DESCRIPTION |
| 2 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 3 | D0 | data input |
| 4 | D1 | data input |
| 5 | D2 | data input |
| 6 | D3 | data input |
| 7 | CEP | count enable input |
| 8 | GND | ground (0 V) |
| 9 | $\overline{\text { PE }}$ | parallel enable input (active LOW) |
| 10 | CET | count enable carry input |
| 11 | Q3 | flip-flop output |
| 12 | Q2 | flip-flop output |
| 13 | Q1 | flip-flop output |
| 14 | Q0 | flip-flop output |
| 15 | TC | terminal count output |
| 16 | VCC | supply voltage |

## Presettable synchronous 4-bit binary

 counter; synchronous reset

Fig. 1 Pin configuration SO16 and (T)SSOP16.


Fig. 3 Logic symbol.


Transparent top view
(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig. 2 Pin configuration DHVQFN16


Fig. 4 Logic symbol (IEEE/IEC).

## Presettable synchronous 4-bit binary counter; synchronous reset



Fig. 5 Functional diagram.


Fig. 6 State diagram.

SO KEW tOOZ

Fig． 8 Logic diagram．

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| :---: | :---: |
|  |  |

## Presettable synchronous 4-bit binary counter; synchronous reset

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{V}_{\mathrm{CC}}$ | supply voltage | for maximum speed performance | 2.7 | 3.6 | V |
|  |  | for low-voltage applications | 1.2 | 3.6 | V |
| $\mathrm{~V}_{\mathrm{I}}$ | input voltage |  | 0 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{O}}$ | output voltage |  | 0 | $\mathrm{~V}_{\mathrm{CC}}$ | V |
| $\mathrm{T}_{\mathrm{amb}}$ | operating ambient temperature | in free air | -40 | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | input rise and fall times | $\mathrm{V}_{\mathrm{CC}}=1.2 \mathrm{~V}$ to 2.7 V | 0 | 20 | $\mathrm{~ns} / \mathrm{V}$ |
|  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ to 3.6 V | 0 | 10 | $\mathrm{~ns} / \mathrm{V}$ |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{V}_{\mathrm{CC}}$ | supply voltage |  | -0.5 | +6.5 | V |
| $\mathrm{I}_{\mathrm{IK}}$ | input diode current | $\mathrm{V}_{\mathrm{I}}<0 \mathrm{~V}$ | - | -50 | mA |
| $\mathrm{~V}_{\mathrm{I}}$ | input voltage | note 1 | -0.5 | +6.5 | V |
| $\mathrm{I}_{\mathrm{OK}}$ | output diode current | $\mathrm{V}_{\mathrm{O}}>\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{O}}<0 \mathrm{~V}$ | - | $\pm 50$ | mA |
| $\mathrm{~V}_{\mathrm{O}}$ | output voltage | note 1 | -0.5 | $\mathrm{~V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{I}_{\mathrm{O}}$ | output source or sink current | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{CC}}$ | - | $\pm 50$ | mA |
| $\mathrm{I}_{\mathrm{CC}}, \mathrm{I}_{\mathrm{GND}}$ | $\mathrm{V}_{\text {CC }}$ or GND current |  | - | $\pm 100$ | mA |
| $\mathrm{~T}_{\text {stg }}$ | storage temperature |  | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{P}_{\text {tot }}$ | power dissipation | $\mathrm{T}_{\text {amb }}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C} ;$ note 2 | - | 500 | mW |

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO16 packages: above $70^{\circ} \mathrm{C}$ the value of $P_{\text {tot }}$ derates linearly with $8 \mathrm{~mW} / \mathrm{K}$.

For SSOP16 and TSSOP16 packages: above $60^{\circ} \mathrm{C}$ the value of $P_{\text {tot }}$ derates linearly with $5.5 \mathrm{~mW} / \mathrm{K}$.
For DHVQFN16 packages: above $60^{\circ} \mathrm{C}$ the value of $\mathrm{P}_{\text {tot }}$ derates linearly with $4.5 \mathrm{~mW} / \mathrm{K}$.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V ).

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN. | TYP. ${ }^{(1)}$ | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | OTHER | $\mathrm{V}_{\mathrm{Cc}}(\mathrm{V})$ |  |  |  |  |
| $\mathrm{T}_{\text {amb }}=-40^{\circ} \mathrm{C}$ to $+85{ }^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH-level input voltage |  | 1.2 | $\mathrm{V}_{\mathrm{CC}}$ | - | - | V |
|  |  |  | 2.7 to 3.6 | 2.0 | - | - | V |
| $\mathrm{V}_{\text {IL }}$ | LOW-level input voltage |  | 1.2 | - | - | GND | V |
|  |  |  | 2.7 to 3.6 | - | - | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH-level output voltage | $\begin{gathered} \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ \mathrm{I}_{\mathrm{O}}=-100 \mu \mathrm{~A} \\ \mathrm{I}_{\mathrm{O}}=-12 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}}=-18 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}}=-24 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & 2.7 \text { to } 3.6 \\ & 2.7 \\ & 3.0 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}-0.2 \\ & \mathrm{~V}_{\mathrm{CC}}-0.5 \\ & \mathrm{~V}_{\mathrm{CC}}-0.6 \\ & \mathrm{~V}_{\mathrm{CC}}-0.8 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}} \\ & - \\ & - \\ & - \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW-level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{I}} & =\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ \mathrm{I}_{\mathrm{O}} & =100 \mu \mathrm{~A} \\ \mathrm{I}_{\mathrm{O}} & =12 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}} & =24 \mathrm{~mA} \end{aligned}$ | $\begin{array}{\|l} \hline 2.7 \text { to } 3.6 \\ 2.7 \\ 3.0 \\ \hline \end{array}$ | $\left.\right\|_{-} ^{-}$ |  | $\begin{array}{\|l\|} \hline 0.2 \\ 0.4 \\ 0.55 \\ \hline \end{array}$ | $\begin{array}{\|l} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~V} \\ \hline \end{array}$ |
| $\mathrm{ILI}^{\prime}$ | input leakage current | $\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ or GND | 3.6 | - | $\pm 0.1$ | $\pm 5$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ | quiescent supply current | $\begin{aligned} & \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}} \text { or } \mathrm{GND} ; \\ & \mathrm{I}_{\mathrm{O}}=0 \mathrm{~A} \\ & \hline \end{aligned}$ | 3.6 | - | 0.1 | 10 | $\mu \mathrm{A}$ |
| $\Delta \mathrm{l}_{\mathrm{CC}}$ | additional quiescent supply current per input pin | $\begin{aligned} & \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}}-0.6 \mathrm{~V} ; \\ & \mathrm{l}=0 \mathrm{~A} \end{aligned}$ | 2.7 to 3.6 | - | 5 | 500 | $\mu \mathrm{A}$ |

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| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN. | TYP. ${ }^{(1)}$ | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | OTHER | $\mathrm{V}_{\mathrm{Cc}}(\mathrm{V})$ |  |  |  |  |
| $\mathrm{T}_{\text {amb }}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH-level input voltage |  | 1.2 | $\mathrm{V}_{\mathrm{CC}}$ | - | - | V |
|  |  |  | 2.7 to 3.6 | 2.0 | - | - | V |
| $\mathrm{V}_{\text {IL }}$ | LOW-level input voltage |  | 1.2 | - | - | GND | V |
|  |  |  | 2.7 to 3.6 | - | - | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH-level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{I}} & =\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ \mathrm{I}_{\mathrm{O}} & =-100 \mu \mathrm{~A} \\ \mathrm{I}_{\mathrm{O}} & =-12 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}} & =-18 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}} & =-24 \mathrm{a} \end{aligned}$ | $\begin{aligned} & 2.7 \text { to } 3.6 \\ & 2.7 \\ & 3.0 \\ & 3.0 \end{aligned}$ | $\begin{array}{\|l} V_{C C}-0.3 \\ V_{C C}-0.65 \\ V_{C C}-0.75 \\ V_{C C}-1 \\ \hline \end{array}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW-level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{I}} & =\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ \mathrm{I}_{\mathrm{O}} & =100 \mu \mathrm{~A} \\ \mathrm{I}_{\mathrm{O}} & =12 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}} & =24 \mathrm{~mA} \end{aligned}$ | $\begin{array}{\|l} \hline 2.7 \text { to } 3.6 \\ 2.7 \\ 3.0 \\ \hline \end{array}$ |  | $\left.\right\|_{-} ^{-}$ | $\begin{array}{\|l\|} \hline 0.3 \\ 0.6 \\ 0.8 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~V} \\ \hline \end{array}$ |
| $\mathrm{I}_{\mathrm{LI}}$ | input leakage current | $\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ or GND | 3.6 | - | - | $\pm 20$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ | quiescent supply current | $\begin{aligned} & \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}} \text { or } \mathrm{GND} ; \\ & \mathrm{I}_{\mathrm{O}}=0 \mathrm{~A} \\ & \hline \end{aligned}$ | 3.6 | - | - | 40 | $\mu \mathrm{A}$ |
| $\Delta \mathrm{l}_{\mathrm{CC}}$ | additional quiescent supply current per input pin | $\begin{aligned} & \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}}-0.6 \mathrm{~V} ; \\ & \mathrm{I}_{\mathrm{O}}=0 \mathrm{~A} \end{aligned}$ | 2.7 to 3.6 | - | - | 5000 | $\mu \mathrm{A}$ |

## Note

1. Typical values are measured at $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$.

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## AC CHARACTERISTICS

$\mathrm{GND}=0 \mathrm{~V} ; \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} ; \mathrm{R}_{\mathrm{L}}=500 \Omega$.

| SYMBOL | PARAMETER | CONDITIONS |  | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | WAVEFORMS | $\mathrm{V}_{\mathrm{Cc}}(\mathrm{V})$ |  |  |  |  |
| $\mathrm{T}_{\text {amb }}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$; note 1 |  |  |  |  |  |  |  |
| $\mathrm{t}_{\text {PHL }} / \mathrm{t}_{\text {PLH }}$ | propagation delay CP to Qn | see Figs 9 and 14 | 1.2 | - | 18 | - | ns |
|  |  |  | 2.7 | 1.5 | - | 7.3 | ns |
|  |  |  | 3.0 to 3.6 | 1.5 | $4.0^{(2)}$ | 7.3 | ns |
|  | propagation delay CP to TC | see Figs 9 and 14 | 1.2 | - | 23 | - | ns |
|  |  |  | 2.7 | 1.5 | - | 8.1 | ns |
|  |  |  | 3.0 to 3.6 | 1.5 | $4.6{ }^{(2)}$ | 7.9 | ns |
|  | propagation delay CET to TC | see Figs 10 and 14 | 1.2 | - | 16 | - | ns |
|  |  |  | 2.7 | 1.5 | - | 6.9 | ns |
|  |  |  | 3.0 to 3.6 | 1.5 | $3.5{ }^{(2)}$ | 6.4 | ns |
| tw | clock pulse width HIGH or LOW | see Fig. 9 | 2.7 | 5.0 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 4.0 | $1.2^{(2)}$ | - | ns |
| $\mathrm{t}_{\text {su }}$ | set-up time Dn to CP | see Fig. 12 | 2.7 | 3.0 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 2.5 | $1.0^{(2)}$ | - | ns |
|  | set-up time $\overline{\mathrm{MR}}, \overline{\mathrm{PE}}$ to CP | see Fig. 12 | 2.7 | 3.5 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 3.0 | $1.2^{(2)}$ | - | ns |
|  | set-up time CEP, CET to CP | see Fig. 13 | 2.7 | 5.5 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 5.0 | $2.1{ }^{(2)}$ | - | ns |
| $\mathrm{th}_{\mathrm{h}}$ | hold time Dn, PE, CEP, CET to CP | see Figs 12 and 13 | 2.7 | 0.0 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 0.5 | $0.0{ }^{(2)}$ | - | ns |
| $f_{\max }$ | maximum clock pulse frequency | see Fig. 9 | 2.7 | 150 | - | - | MHz |
|  |  |  | 3.0 to 3.6 | 150 | 200 ${ }^{(2)}$ | - | MHz |
| $\mathrm{t}_{\text {sk(0) }}$ | skew | note 3 | 3.0 to 3.6 | - | - | 1.0 | ns |

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| SYMBOL | PARAMETER | CONDITIONS |  | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | WAVEFORMS | $\mathrm{V}_{\mathrm{Cc}}(\mathrm{V})$ |  |  |  |  |
| $\mathrm{T}_{\text {amb }}=-40{ }^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |
| $\mathrm{t}_{\text {PHL }} / \mathrm{t}_{\text {PLH }}$ | propagation delay CP to Qn | see Figs 9 and 14 | 1.2 | - | - | - | ns |
|  |  |  | 2.7 | 1.5 | - | 9.5 | ns |
|  |  |  | 3.0 to 3.6 | 1.5 | - | 9.5 | ns |
|  | propagation delay CP to TC | see Figs 9 and 14 | 1.2 | - | - | - | ns |
|  |  |  | 2.7 | 1.5 | - | 10.5 | ns |
|  |  |  | 3.0 to 3.6 | 1.5 | - | 10.0 | ns |
|  | propagation delay CET to TC | see Figs 10 and 14 | 1.2 | - | - | - | ns |
|  |  |  | 2.7 | 1.5 | - | 9.0 | ns |
|  |  |  | 3.0 to 3.6 | 1.5 | - | 8.0 | ns |
| tw | clock pulse width HIGH or LOW | see Fig. 9 | 2.7 | 5.0 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 4.0 | - | - | ns |
| $\mathrm{t}_{\text {su }}$ | set-up time Dn to CP | see Fig. 12 | 2.7 | 3.0 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 2.5 | - | - | ns |
|  | set-up time $\overline{\mathrm{MR}}, \overline{\mathrm{PE}}$ to CP | see Fig. 12 | 2.7 | 3.5 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 3.0 | - | - | ns |
|  | set-up time CEP, CET to CP | see Fig. 13 | 2.7 | 5.5 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 5.0 | - | - | ns |
| $t_{\text {h }}$ | hold time Dn, PE, CEP, CET to CP | see Figs 12 and 13 | 2.7 | 0.0 | - | - | ns |
|  |  |  | 3.0 to 3.6 | 0.5 | - | - | ns |
| $\mathrm{f}_{\text {max }}$ | maximum clock pulse frequency | see Fig. 9 | 2.7 | 150 | - | - | MHz |
|  |  |  | 3.0 to 3.6 | 150 | - | - | MHz |
| $\mathrm{t}_{\text {sk(0) }}$ | skew | note 3 | 3.0 to 3.6 | - | - | 1.5 | ns |

## Notes

1. All typical values are measured at $\mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$.
2. Typical values are measured at $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

## Presettable synchronous 4-bit binary counter; synchronous reset

## AC WAVEFORMS


$\mathrm{V}_{\mathrm{M}}=1.5 \mathrm{~V}$ at $\mathrm{V}_{\mathrm{CC}} \geq 2.7 \mathrm{~V}$.
$\mathrm{V}_{\mathrm{M}}=0.5 \mathrm{~V}_{\mathrm{CC}}$ at $\mathrm{V}_{\mathrm{CC}}<2.7 \mathrm{~V}$.
$\mathrm{V}_{\mathrm{OL}}$ and $\mathrm{V}_{\mathrm{OH}}$ are typical output voltage drop that occur with the output load.

Fig. 9 Clock (CP) to outputs (Qn, TC) propagation delays, the clock pulse width and the maximum clock frequency.

$V_{M}=1.5 \mathrm{~V}$ at $\mathrm{V}_{\mathrm{CC}} \geq 2.7 \mathrm{~V}$.
$\mathrm{V}_{\mathrm{M}}=0.5 \mathrm{~V}_{\mathrm{CC}}$ at $\mathrm{V}_{\mathrm{CC}}<2.7 \mathrm{~V}$.
$\mathrm{V}_{\mathrm{OL}}$ and $\mathrm{V}_{\mathrm{OH}}$ are typical output voltage drop that occur with the output load.
Fig. 10 Input (CET) to output (TC) propagation delays.

## Presettable synchronous 4-bit binary counter; synchronous reset



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 11 Master reset (MR) pulse width, the master reset to output (Qn, TC) propagation delays and the master reset to clock (CP) removal times.


The shaded areas indicate when the input is permitted to change for predictable output performance.
Fig. 12 Set-up and hold times for the input (Dn) and parallel enable input ( $\overline{\mathrm{PE}}$ ).

## Presettable synchronous 4-bit binary counter; synchronous reset



The shaded areas indicate when the input is permitted to change for predictable output performance.
Fig. 13 CEP and CET set-up and hold times.


| $\mathbf{V}_{\mathbf{C C}}$ | $\mathbf{V}_{\mathbf{I}}$ | $\mathbf{C}_{\mathbf{L}}$ |  | $\mathbf{R}_{\mathbf{L}}$ | $\mathbf{V}_{\mathbf{E X T}}$ |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |
|  |  |  |  |  | $\mathbf{t}_{\mathbf{P Z H}} / \mathbf{t}_{\mathbf{P H Z}}$ | $\mathbf{t}_{\mathbf{P Z L}} / \mathbf{t}_{\mathbf{P L Z}}$ |  |
| 1.2 V | $\mathrm{~V}_{\mathrm{CC}}$ | 50 pF | $500 \Omega^{(1)}$ | open | GND | $2 \times \mathrm{V}_{\mathrm{CC}}$ |  |
| 2.7 V | 2.7 V | 50 pF | $500 \Omega$ | open | GND | $2 \times \mathrm{V}_{\mathrm{CC}}$ |  |
| 3.0 V to 3.6 V | 2.7 V | 50 pF | $500 \Omega$ | open | GND | $2 \times \mathrm{V}_{\mathrm{CC}}$ |  |

## Note

1. The circuit performs better when $R_{L}=1000 \Omega$.

Definitions for test circuits:
$\mathrm{R}_{\mathrm{L}}=$ Load resistor.
$C_{L}=$ Load capacitance including jig and probe capacitance.
$R_{T}=$ Termination resistance should be equal to the output impedance $Z_{0}$ of the pulse generator.

Fig. 14 Load circuitry for switching times.

## Presettable synchronous 4-bit binary counter; synchronous reset

## PACKAGE OUTLINES



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | $\begin{gathered} \mathrm{A} \\ \max . \end{gathered}$ | $\mathrm{A}_{1}$ | $\mathrm{A}_{2}$ | $\mathrm{A}_{3}$ | $\mathrm{b}_{\mathrm{p}}$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $\mathrm{H}_{\mathrm{E}}$ | L | $L_{p}$ | Q | v | w | y | $Z^{(1)}$ | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 1.75 | $\begin{aligned} & 0.25 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 1.45 \\ & 1.25 \end{aligned}$ | 0.25 | $\begin{aligned} & 0.49 \\ & 0.36 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 0.19 \end{aligned}$ | $\begin{gathered} \hline 10.0 \\ 9.8 \end{gathered}$ | $\begin{aligned} & 4.0 \\ & 3.8 \end{aligned}$ | 1.27 | $\begin{aligned} & 6.2 \\ & 5.8 \end{aligned}$ | 1.05 | $\begin{aligned} & 1.0 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 0.7 \\ & 0.6 \end{aligned}$ | 0.25 | 0.25 | 0.1 | $\begin{aligned} & 0.7 \\ & 0.3 \end{aligned}$ | $8^{0}$ |
| inches | 0.069 | $\begin{array}{\|l\|} \hline 0.010 \\ 0.004 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 0.057 \\ 0.049 \\ \hline \end{array}$ | 0.01 | $\begin{array}{\|l\|} \hline 0.019 \\ 0.014 \end{array}$ | $\begin{array}{\|l\|} \hline 0.0100 \\ 0.0075 \end{array}$ | $\begin{aligned} & 0.39 \\ & 0.38 \end{aligned}$ | $\begin{aligned} & 0.16 \\ & 0.15 \end{aligned}$ | 0.05 | $\begin{array}{\|l\|} \hline 0.244 \\ 0.228 \\ \hline \end{array}$ | 0.041 | $\begin{aligned} & \hline 0.039 \\ & 0.016 \end{aligned}$ | $\begin{aligned} & 0.028 \\ & 0.020 \end{aligned}$ | 0.01 | 0.01 | 0.004 | $\begin{aligned} & 0.028 \\ & 0.012 \end{aligned}$ | $0^{\circ}$ |

Note

1. Plastic or metal protrusions of $0.15 \mathrm{~mm}(0.006 \mathrm{inch})$ maximum per side are not included.

| OUTLINE <br> VERSION | REFERENCES |  |  |  | EUROPEAN <br> PROJECTION | ISSUE DATE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | JEITA |  |  |  |
| SOT109-1 | $076 E 07$ | MS-012 |  |  | - |  |

## Presettable synchronous 4-bit binary counter; synchronous reset



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | $\mathrm{A}_{1}$ | $\mathrm{A}_{2}$ | $\mathrm{A}_{3}$ | $b_{p}$ | C | $D^{(1)}$ | $E^{(1)}$ | e | $\mathrm{H}_{\mathrm{E}}$ | L | $L_{p}$ | Q | v | W | y | $Z^{(1)}$ | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 2 | $\begin{aligned} & 0.21 \\ & 0.05 \end{aligned}$ | $\begin{aligned} & 1.80 \\ & 1.65 \end{aligned}$ | 0.25 | $\begin{aligned} & 0.38 \\ & 0.25 \end{aligned}$ | $\begin{aligned} & 0.20 \\ & 0.09 \end{aligned}$ | $\begin{aligned} & 6.4 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 5.4 \\ & 5.2 \end{aligned}$ | 0.65 | $\begin{aligned} & 7.9 \\ & 7.6 \end{aligned}$ | 1.25 | $\begin{aligned} & 1.03 \\ & 0.63 \end{aligned}$ | $\begin{aligned} & 0.9 \\ & 0.7 \end{aligned}$ | 0.2 | 0.13 | 0.1 | $\begin{aligned} & 1.00 \\ & 0.55 \end{aligned}$ | $8^{\circ}$ $0^{\circ}$ |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE <br> VERSION | REFERENCES |  |  |  | EUROPEAN <br> PROJECTION | ISSUE DATE |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | JEITA |  |  | $-99-12-27$ |
| SOT338-1 |  | MO-150 |  |  | $03-02-19$ |  |

## Presettable synchronous 4-bit binary counter; synchronous reset

| UNIT | A max. | $\mathrm{A}_{1}$ | $\mathrm{A}_{2}$ | $\mathrm{A}_{3}$ | $\mathrm{b}_{\mathrm{p}}$ | c | D ${ }^{(1)}$ | $E^{(2)}$ | e | $\mathrm{H}_{\mathrm{E}}$ | L | $\mathrm{L}_{\mathrm{p}}$ | Q | v | w | y | $Z^{(1)}$ | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 1.1 | $\begin{aligned} & 0.15 \\ & 0.05 \end{aligned}$ | $\begin{aligned} & 0.95 \\ & 0.80 \end{aligned}$ | 0.25 | $\begin{aligned} & 0.30 \\ & 0.19 \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 5.1 \\ & 4.9 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 4.3 \end{aligned}$ | 0.65 | $\begin{aligned} & \hline 6.6 \\ & 6.2 \end{aligned}$ | 1 | $\begin{aligned} & 0.75 \\ & 0.50 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.3 \end{aligned}$ | 0.2 | 0.13 | 0.1 | $\begin{aligned} & 0.40 \\ & 0.06 \end{aligned}$ | 8 $0^{\circ}$ |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |  |  | EUROPEAN PROJECTION | ISSUE DATE |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | JEITA |  |  |
| SOT403-1 |  | MO-153 |  | $\bigcirc$ | $\begin{aligned} & \hline-9-12-27 \\ & 03-02-18 \end{aligned}$ |

## Presettable synchronous 4-bit binary counter; synchronous reset

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85 \mathrm{~mm}$

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |  |  | EUROPEAN PROJECTION | ISSUE DATE |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | JEITA |  |  |
| SOT763-1 | --- | MO-241 | -- - |  | $\begin{aligned} & \hline 02-10-17 \\ & 03-01-27 \end{aligned}$ |

# Presettable synchronous 4-bit binary counter; synchronous reset 

## DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ${ }^{(1)}$ | PRODUCT STATUS ${ }^{(2)(3)}$ | DEFINITION |
| :---: | :---: | :---: | :---: |
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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