



2.5-V/3.3-V OSCILLATOR GAIN STAGE/BUFFERS

FEATURES

- Low-Voltage PECL Input and Low-Voltage **PECL or LVDS Outputs**
- **Clock Rates to 1 GHz**
 - 250-ps Output Transition Times
 - 0.12 ps Typical Intrinsic Phase Jitter
 - Less than 630 ps Propagation Delay Times
- 2.5-V or 3.3-V Supply Operation

2-mm x 2-mm Small-Outline **No-Lead Package**

APPLICATIONS

- **PECL-to-LVDS Translation**
- **Clock Signal Amplification**

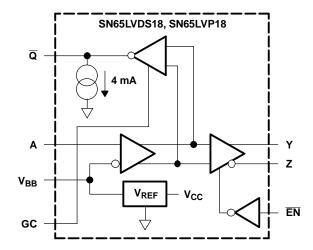
DESCRIPTION

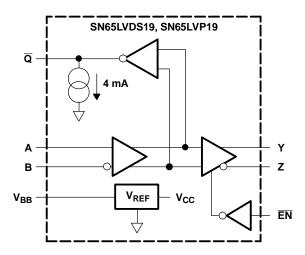
These four devices are high frequency oscillator gain stages supporting both LVPECL or LVDS on the high gain outputs in 3.3-V or 2.5-V systems. Additionally, provides the option of both single-ended input (PECL levels on the SN65LVx18) and fully differential inputs on the SN65LVx19.

The SN65LVx18 provides the user a Gain Control (GC) for controlling the Q output from 300 mV to 860 mV either by leaving it open (NC), grounded, or tied to V_{CC} . (When left open, the \overline{Q} output defaults to 575 mV.) The Q on the SN65LVx19 defaults to 575 mV as well.

Both devices provide a voltage reference (V_{BB}) of typically 1.35 V below V_{CC} for use in receiving single-ended PECL input signals. When not used, V_{BB} should be unconnected or open.

All devices are characterized for operation from -40°C to 85°C.







Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS(1)

INPUT	OUTPUT	GAIN CONTROL	BASE PART NUMBER	PART MARKING
Single-ended	LVDS	Yes	SN65LVDS18	ER
Single-ended	LVPECL	Yes	SN65LVP18	EP
Differential	LVDS	No	SN65LVDS19	ET
Differential	LVPECL	No	SN65LVP19	ES

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{CC}	Supply voltage (2)	−0.5 V to 4 V
V_{I}	Input voltage	-0.5 V to V _{CC} + 0.5 V
Vo	Output voltage	-0.5 V to V _{CC} + 0.5 V
IO	V _{BB} output current	±0.5 mA
	HBM electrostatic discharge ⁽³⁾	±3 kV
	CDM electrostatic discharge ⁽⁴⁾	±1500 V
	Continuous power dissipation	See Power Dissipation Ratings Table

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	T _A < 25°C	OPERATING FACTOR	T _A = 85°C
	POWER RATING	ABOVE T _A = 25°C	POWER RATING
DRF	403 mW	4.0 mW/°C	161 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT	
V _{CC}	Supply Voltage		2.375	2.5 or 3.3	3.6	V	
V_{IC}	Common-mode input voltage (V _{IA} + V _{IB})/2	SN65LVDS19 or SN65LVP19	1.2		$V_{CC} - (V_{ID}/2)$	V	
$ V_{ID} $	Differential input voltage magnitude V _{IA} - V _{IB}	SN65LVDS19 or SN65LVP19	0.8		1	V	
V	High level input veltage	EN	2		V _{CC}	V	
V _{IH}	High-level input voltage	SN65LVDS18 or SN65LVP18	V _{CC} - 1.17		V _{CC} - 0.44	V	
V	Low lovel input voltoge	EN	0		0.8	V	
V _{IL}	Low-level input voltage	SN65LVDS18 or SN65LVP18	V _{CC} - 2.25	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	V _{CC} - 1.52	V	
Io	Output current to V _{BB}		-400 ⁽¹⁾		400	μΑ	
R_L	Differential load resistance		90		132	Ω	
T _A	Operating free-air temperature		-40		85	°C	

⁽¹⁾ The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

⁽²⁾ All voltage values, except differential voltages, are with respect to network ground (see Figure 1).

⁽³⁾ Tested in accordance with JEDEC Standard 22, Test Method A114-A-7

⁽⁴⁾ Tested in accordance with JEDEC Standard 22, Test Method C101



ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
1	Cupply current	$R_L = 100 \Omega$, \overline{EN} at 0 V, Other inputs open		30	36	A
I _{CC}	Supply current	Outputs unloaded, EN at 0 V, Other inputs open		17	22	mA
V_{BB}	Reference voltage (2)	I _{BB} = -400 μA	V _{CC} - 1.44	V _{CC} - 1.35	V _{CC} - 1.25	V
Ін	High-level input current, EN	V _I = 2 V	-20		20	
I _{IAH} or I _{IBH}	High-level input current, A or B	$V_{I} = V_{CC}$	-20		20	
I _{IL}	Low-level input current, EN	V _I = 0.8 V	-20		20	μA
I _{IAL} or I _{IBL}	Low-level input current, A or B	V _I = GND	-20		20	
SN65LVDS1	8/19 Y AND Z OUTPUT CHARACTER	ISTICS	-		Į.	
V _{OD}	Differential output voltage magnitude, V _{OY} - V _{OZ}		247	340	454	.,
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states	See Figure 1 and Figure 2			50	mV
V _{OC(SS)}	Steady-state common- mode output voltage (see Figure 3)		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage			50	100	
l _{OYZ} or l _{OZZ}	High-impedance output current	$\overline{\text{EN}}$ at V_{CC} , $V_{\text{O}} = 0 \text{ V or } V_{\text{CC}}$	-1		1	μΑ
l _{OYS} or l _{OZS}	Short-circuit output current	$\overline{\text{EN}}$ at 0 V, V_{OY} or $V_{OZ} = 0$ V	-50		50	
I _{OS(D)}	Differential short-circuit output current, I _{OY} -I _{OZ}	EN at 0 V, V _{OY} = V _{OZ}	-12		12	mA
SN65LVP18/	19 Y AND Z OUTPUT CHARACTERIS	TICS	,		1	
V _{OYH} or V _{OZH}	High-level output voltage	3.3 V; 50 Ω from Y and Z	V _{CC} - 1.13		V _{CC} - 0.85	
V _{OYL} or V _{OZL}	Low-level output voltage	to V _{CC} - 2 V	V _{CC} - 1.87		V _{CC} - 1.61	V
V _{OYL} or V _{OZL}	Low-level output voltage	2.5 V; 50 Ω from Y and Z to $V_{CC}-$ 2 V	V _{CC} - 1.92		V _{CC} - 1.61	V
V _{OD}	Differential output voltage magnitude, V _{OH} - V _{OL}		0.6	0.8	1	
I _{OYZ} or I _{OZZ}	High-impedance output current	$\overline{\text{EN}}$ at V_{CC} , $V_{\text{O}} = 0 \text{ V or } V_{\text{CC}}$	-1		1	μΑ
Q OUTPUT (CHARACTERISTICS (see Figure 1)				1	
V _{OH}	High-level output voltage	No load		V _{CC} - 0.94		V
		GC Tied to GND, No load		V _{CC} - 1.22		
V_{OL}	Low-level output voltage	GC Open, No load		V _{CC} - 1.52		
		GC Tied to V _{CC} , No load		V _{CC} - 1.82		
		GC Tied to GND		300		
$V_{O(pp)}$	Peak-to-peak output voltage	GC Open		575		
- 1007		CGT Tied to V _{CC}		860		

Typical values are at room temperature and with a V_{CC} of 3.3 V. Single-ended input operation is limited to V_{CC} \geq 3.0 V.



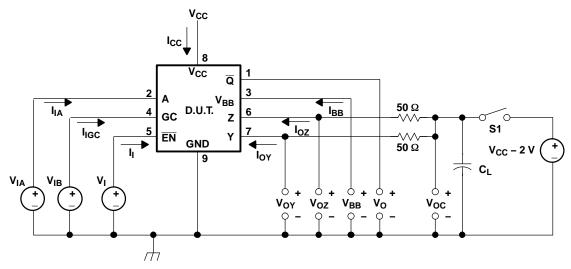
SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
	Duran matical delevations 4	A to Q	See Figure 4		340	460	
t _{PD}	Propagation delay time, t _{PLH} or t _{PHL}	D to Y or Z	See Figure 4		460	630	ps
t _{SK(P)}	Pulse skew, t _{PLH} - t _{PHL}					20	
	Don't to nort alcour (2)		V _{CC} = 3.3 V			80	20
t _{SK(PP)}	Part-to-part skew (2)		V _{CC} = 2.5 V			130	ps
	200/ to 200/ differential simple via time		LVDS, See Figure 4		140	250	
t _r	20%-to-80% differential signal rise tin	ne	LVPECL, See Figure 4		190	300	ps
	000/ 1- 000/ -1///	_	LVDS, See Figure 4		140	250	
t _f	20%-to-80% differential signal fall time		LVPECL, See Figure 4		210	300	ps
t _{jit(per)}	RMS period jitter ⁽³⁾		2-GHz 50%-duty-cycle square-wave input,		2	4	
t _{jit(cc)}	Peak cycle-to-cycle jitter (4)		See Figure 5		17	24	ps
t _{jit(ph)}	Intrinsic phase jitter		1 GHz		0.12		ps
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output					30	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output		See Figure 6	30			ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output		See Figure 6	30			
t _{PZL}	Propagation delay time, high-impedance-to-low-level output					30	

- Typical values are at room temperature and with a V_{CC} of 3.3 V. Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
- Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle

PARAMETER MEASUREMENT INFORMATION

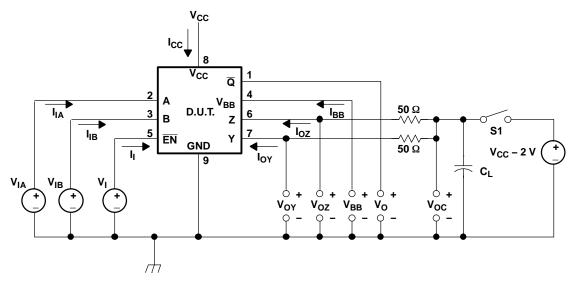


- (1) C_L is the instrumentation and test fixture capacitance.
- (2) S1 is open for the SN65LVDS18 and closed for the SN65LVP18.

Figure 1. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP18



PARAMETER MEASUREMENT INFORMATION (continued)



- (1) C_L is the instrumentation and test fixture capacitance.
- (2) S1 is open for the SN65LVDS19 and closed for the SN65LVP19.

Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP19

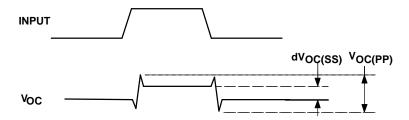


Figure 3. V_{OC} Definitions

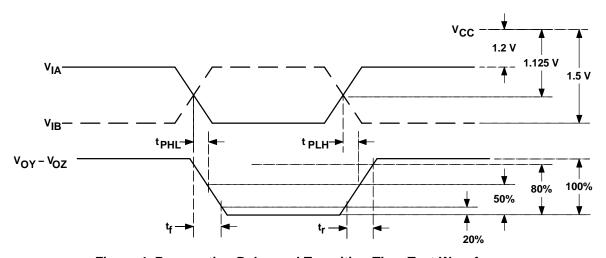


Figure 4. Propagation Delay and Transition Time Test Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)

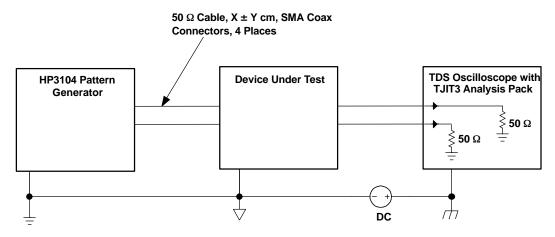


Figure 5. Jitter Measurement Setup

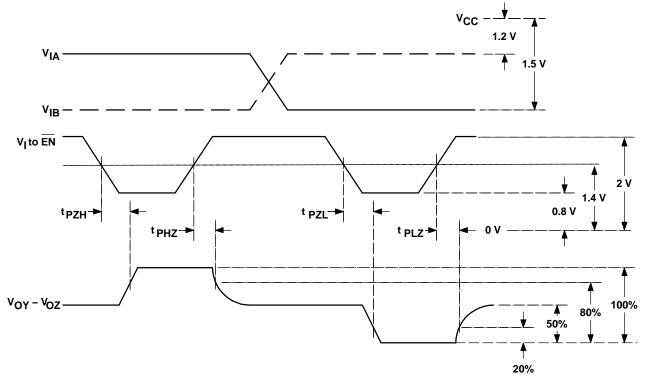


Figure 6. Enable and Disable Time Test Waveforms



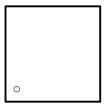
DEVICE INFORMATION

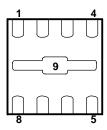
FUNCTION TABLE (1)

	SN65LVI	DS18, SN	65LVP18		SN65LVDS19, SN65LVP19					
Α	EN	Q	Υ	Z	Α	В	EN	Q	Υ	Z
Н	L	L	Н	L	Н	Н	L	?	?	?
L	L	Н	L	Н	L	Н	L	Н	L	Н
Х	Н	?	Z	Z	Н	L	L	L	Н	L
Open	L	?	?	?	L	L	L	?	?	?
Х	Open	?	?	?	Х	Х	Н	?	Z	Z
					Open	Open	L	?	?	?
					Х	Х	Open	?	?	?

(1) H = high, L = low, Z = high impedance, ? = indeterminate

DRF PACKAGE TOP VIEW





BOTTOM VIEW

Package Pin Assignments - Numerical Listing

SN65LVDS1	8, SN65LVP18	SN65LVDS19, SN65LVP19					
PIN	SIGNAL	PIN	SIGNAL				
1	Q	1	Q				
2	Α	2	Α				
3	V _{BB}	3	В				
4	GC	4	V _{BB}				
5	ĒN	5	EN				
6	Z	6	Z				
7	Y	7	Y				
8	V _{CC}	8	V _{cc}				
9	GND	9	GND				



TYPICAL CHARACTERISTICS

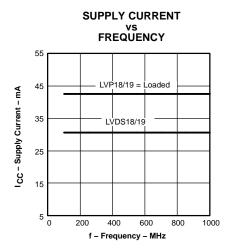


Figure 7.

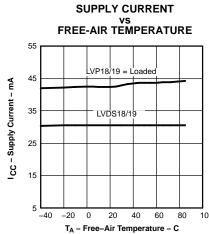


Figure 8.

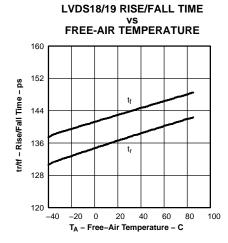


Figure 9.

PERIOD JITTER



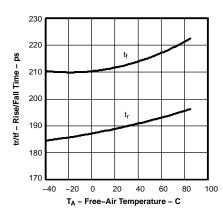


Figure 10.

LVDS18/19 PROPAGATION DELAY TIME

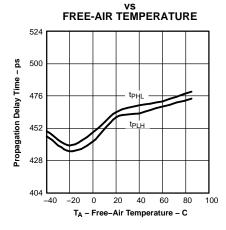
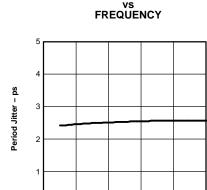


Figure 11.



f – Frequency – MHz Figure 12.

600

1000

400

200

CYCLE-TO-CYCLE JITTER vs FREQUENCY

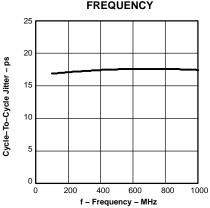


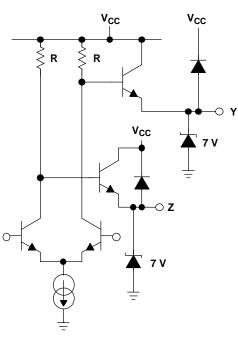
Figure 13.

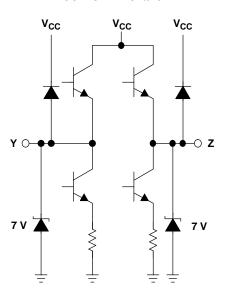


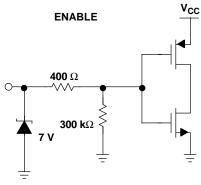
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

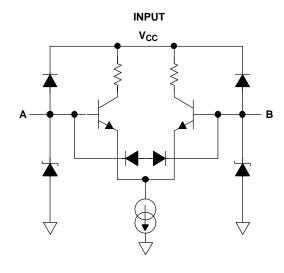


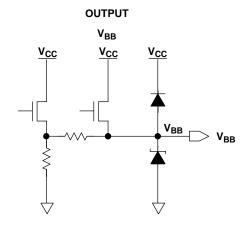
OUTPUT LVDS18/19















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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65LVDS18DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVDS18DRFTG4	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVDS19DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVDS19DRFTG4	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVP18DRFR	ACTIVE	WSON	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVP18DRFRG4	ACTIVE	WSON	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVP18DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVP18DRFTG4	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVP19DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVP19DRFTG4	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

30-Jul-2011

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS18DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS19DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP18DRFR	WSON	DRF	8	3000	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP18DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP19DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2

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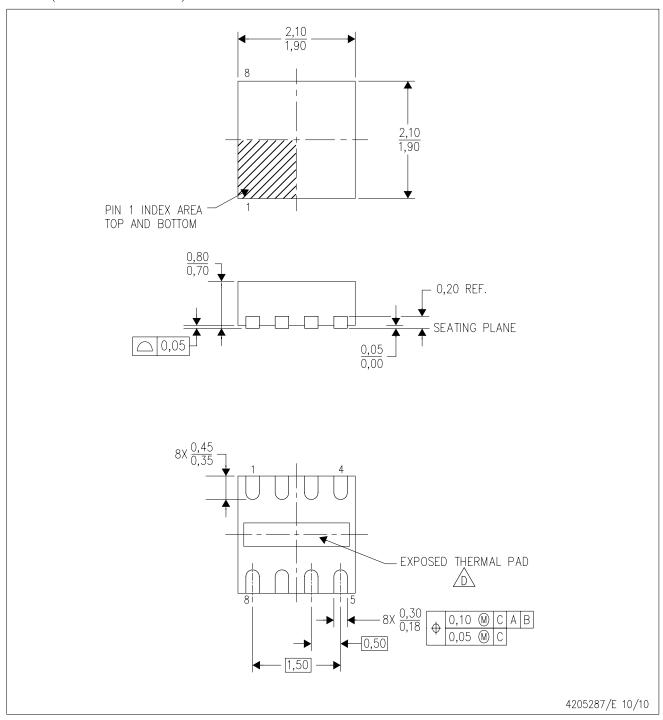


*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS18DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVDS19DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP18DRFR	WSON	DRF	8	3000	337.0	343.0	29.0
SN65LVP18DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP19DRFT	WSON	DRF	8	250	337.0	343.0	29.0

DRF (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- Ç. Quad Flatpack, No-Leads (QFN) package configuration.
- The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-229.



DRF (S-PWSON-N8)

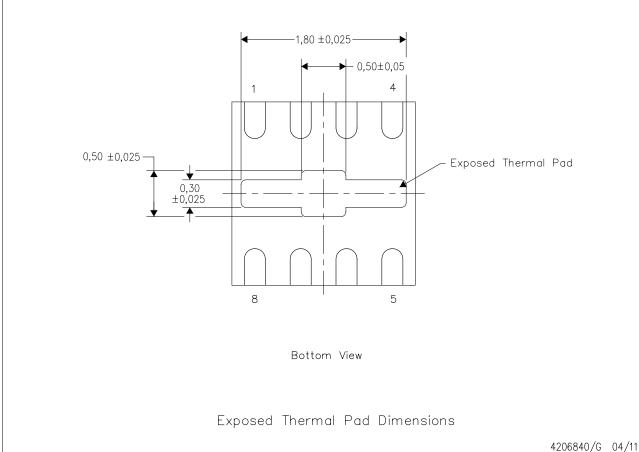
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

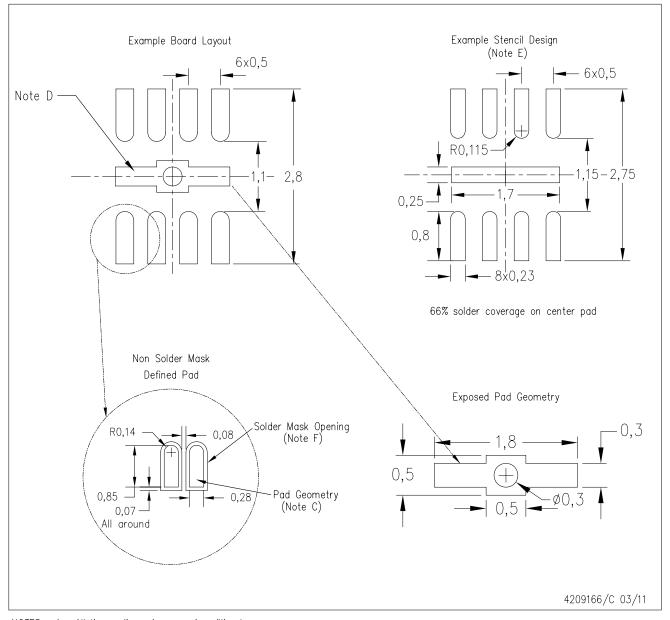
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters

DRF (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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