SCLS121D - DECEMBER 1982 - REVISED OCTOBER 2003

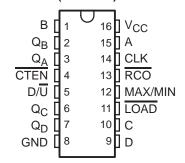
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>
- Typical t<sub>pd</sub> = 13 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Single Down/Up Count-Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable With Load Control

#### description/ordering information

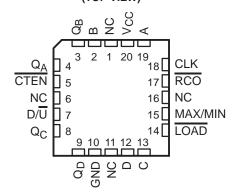
The 'HC191 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low- to high-level transition of the clock (CLK) input if the count-enable ( $\overline{CTEN}$ ) input is low. A high at  $\overline{CTEN}$  inhibits counting. The direction of the count is determined by the level of the down/up (D/ $\overline{U}$ ) input. When D/ $\overline{U}$  is low, the counter counts up, and when D/ $\overline{U}$  is high, it counts down.

SN54HC191 . . . J OR W PACKAGE SN74HC191 . . . D, N, OR NS PACKAGE (TOP VIEW)



SN54HC191 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube of 25	SN74HC191N	SN74HC191N		
		Tube of 40	SN74HC191D			
-40°C to 85°C	SOIC - D	Reel of 2500	SN74HC191DR	HC191		
		Reel of 250	SN74HC191DT	1		
	SOP - NS	Reel of 2000	SN74HC191NSR	HC191		
	CDIP – J	Tube of 25	SNJ54HC191J	SNJ54HC191J		
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC191W	SNJ54HC191W		
	LCCC - FK	Tube of 55	SNJ54HC191FK	SNJ54HC191FK		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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#### description/ordering information (continued)

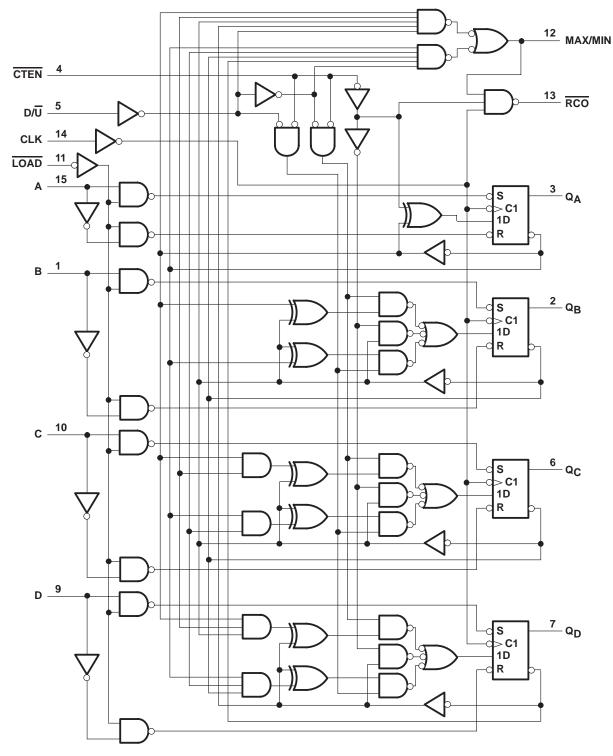
These counters feature a fully independent clock circuit. Change at the control ( $\overline{\text{CTEN}}$  and  $D/\overline{U}$ ) inputs that modifies the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, each of the outputs can be preset to either level by placing a low on the load (LOAD) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of CLK. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock  $(\overline{RCO})$  and maximum/minimum (MAX/MIN) count. MAX/MIN produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down, or maximum (9 or 15) counting up.  $\overline{RCO}$  produces a low-level output pulse under those same conditions, but only while CLK is low. The counters can be cascaded easily by feeding  $\overline{RCO}$  to  $\overline{CTEN}$  of the succeeding counter if parallel clocking is used, or to CLK if parallel enabling is used. MAX/MIN can be used to accomplish look ahead for high-speed operation.



## logic diagram (positive logic)

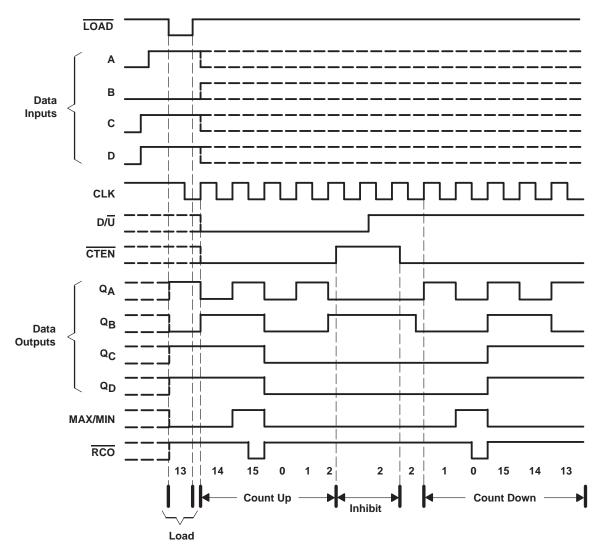


Pin numbers shown are for the D, J, N, NS, and W packages.

#### typical load, count, and inhibit sequence

The following sequence is illustrated below:

- 1. Load (preset) to binary 13
- 2. Count up to 14, 15 (maximum), 0, 1, and 2
- 3. Inhibit
- 4. Count down to 1, 0 (minimum), 15, 14, and 13





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		$\dots$ -0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see	ee Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CO}$	c) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )		±25 mA
Continuous current through V <sub>CC</sub> or GND		
Package thermal impedance, θ <sub>JA</sub> (see Note 2):		
,	N package	67°C/W
	NS package	64°C/W
Storage temperature range, T <sub>stg</sub>		65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

			N2	N54HC19	)1	SN	174HC19	)1	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
VIH	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		VCC = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		V <sub>CC</sub> = 2 V			1000			1000	
Δt/Δv‡	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>‡</sup> If this device is used in the threshold region (from V<sub>IL</sub>max = 0.5 V to V<sub>IH</sub>min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEOT 0.0	TEST COMPITIONS			A = 25°C	;	SN54H	IC191	SN74HC191		UNIT	
PARAMETER	TEST CC	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
			2 V	1.9	1.998		1.9		1.9			
		I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4			
Voн	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V	
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84			
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34			
			2 V		0.002	0.1		0.1		0.1		
		$I_{OL} = 20 \mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1		
VoL	VI = VIH or VIL		6 V		0.001	0.1		0.1		0.1	V	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33		
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33		
lį	$V_I = V_{CC}$ or 0		6 V	·	±0.1	±100		±1000		±1000	nA	
ICC	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ	
Ci		_	2 V to 6 V		3	10		10		10	pF	

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# timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				T <sub>A</sub> = 2	25°C	SN54H	IC191	SN74H	IC191	
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		4.2		2.8		3.3	
fclock	Clock frequency		4.5 V		21		14		17	MHz
			6 V		24		16		19	
			2 V	120		180		150		
		LOAD low	4.5 V	24		36		30		
	Dulas dunation		6 V	21		31		26		
t <sub>W</sub>	Pulse duration		2 V	120		180		150		ns
		CLK high or low	4.5 V	24		36		30		
			6 V	21		31		26		
			2 V	150		230		188		
		Data before LOAD↑	4.5 V	30		46		38		
		6 V	25		38		32		ı	
		2 V	205		306		255			
		CTEN before CLK↑	4.5 V	41		61		51		ns
			6 V	35		53		44		
t <sub>su</sub>	Setup time		2 V	205		306		255		
		D/U before CLK↑	4.5 V	41		61		51		
			6 V	35		53		44		
			2 V	150		225		190		
		LOAD inactive before CLK↑	4.5 V	30		45		38		
			6 V	25		38		32		
			2 V	5		5		5		
		Data after LOAD↑	4.5 V	5		5		5		
			6 V	5		5		5		
			2 V	5		5		5		
th	Hold time	CTEN after CLK↑	4.5 V	5		5		5		ns
			6 V	5		5		5		
			2 V	5		5		5		
		D/U after CLK↑	4.5 V	5		5		5		
			6 V	5		5		5		

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# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

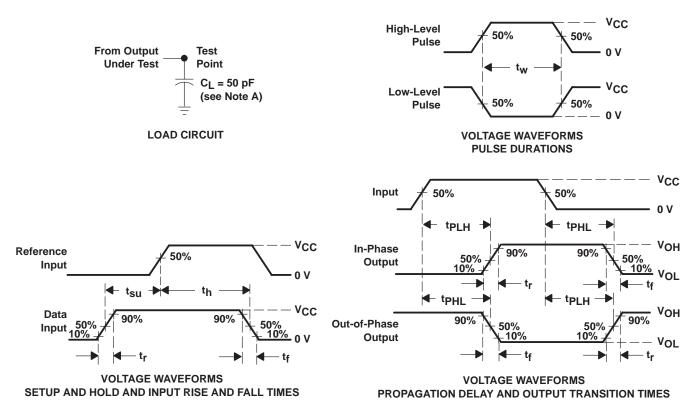
	FROM	то		T,	Δ = 25°C	;	SN54H	IC191	SN74H	C191	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	4.2	8		2.8		3.3		
fmax			4.5 V	21	42		14		17		MHz
			6 V	24	48		16		19		
			2 V		130	264		396		330	
	LOAD	Any Q	4.5 V		40	53		79		66	
			6 V		33	45		67		56	
			2 V		135	240		360		300	
	A, B, C, or D	$Q_A$ , $Q_B$ , $Q_C$ , or $Q_D$	4.5 V		36	48		72		60	
		о, <b>ч</b> р	6 V		30	41		61		51	
			2 V		58	120		180		150	
		RCO	4.5 V		17	24		36		30	
			6 V		14	21		31		26	
			2 V		107	192		288		240	ns
	CLK	Any Q	4.5 V		31	38		58		48	
4			6 V		26	32		49		41	
<sup>t</sup> pd		MAX/MIN	2 V		123	252		378		315	
			4.5 V		39	50		76		63	
			6 V		32	43		65		54	
			2 V		102	228		342		285	
		RCO	4.5 V		29	46		68		57	
	D/ <del>U</del>		6 V		24	38		59		49	
	D/U		2 V		86	192		288		240	
		MAX/MIN	4.5 V		24	38		58		48	
			6 V		20	32		49		41	
			2 V		50	132		198		165	
	CTEN	RCO			15	26		40		33	
			6 V		13	23		34		28	
			2 V		38	75		110		95	
t <sub>t</sub>		Any	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	

## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	50	pF



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f = 6$  ns,  $t_f = 6$  ns.
- C. For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-86891012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8689101EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
SN54HC191J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74HC191D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC191N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74HC191NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC191NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC191NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54HC191FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC191J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	





www.ti.com 5-Sep-2011

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54HC191, SN74HC191:

Catalog: SN74HC191

Military: SN54HC191

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



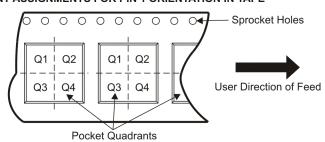
#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC191DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC191NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC191DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC191NSR	SO	NS	16	2000	346.0	346.0	33.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE

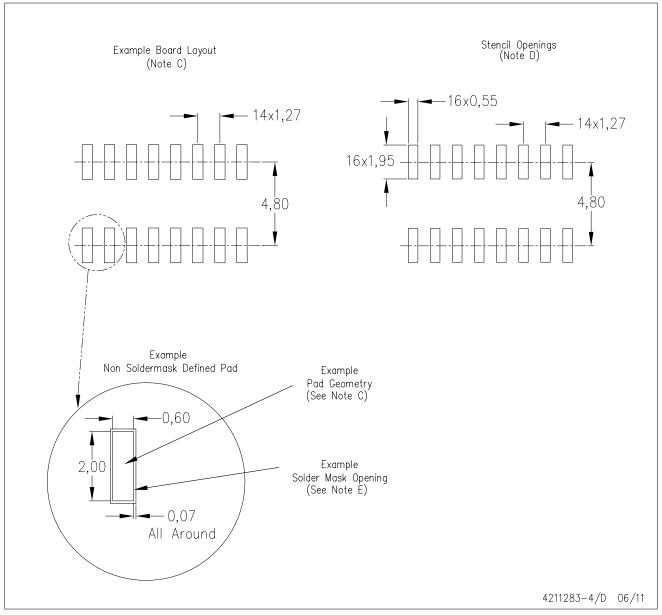


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



## D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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