TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

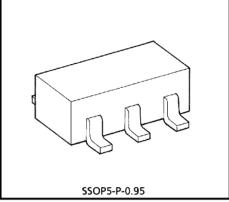
TC4S81F

2 INPUT AND GATE

The TC4S81F is 2-input positive logic AND gates. Gate output with inverter buffer improve the inputoutput characteristics and even if the load capacitance increases, it can be stopped the change of propagation time.

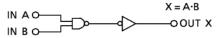
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} = 0.5 \sim V_{SS} + 20$	V
Input Voltage	VIN	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	٧
Output Voltage	Vout	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	٧
DC Input Current	I _{IN}	± 10	mA
Power Dissipation	PD	200	mW
Operating Temperature	_	- 40~85	°C
Range	T _{opr}	- 40~65	
Storage Temperature	-	GE . 150	°C
Range	T _{stg}	−65~150	,
Lead Temperature (10s)	TL	260	°C

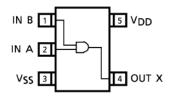


Weight: 0.016g (Typ.)

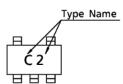
LOGIC DIAGRAM



PIN CONFIGURATION (TOP VIEW)



MARKING



RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}	_	3		18	V
Input Voltage	VIN	_	0	_	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

I CHARACTERISTIC I		SYM-	TEST CONDITION	V _{DD}	– 40°C		25°C			85°C		UNIT
		BOL	TEST CONDITION	(V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High-Level			l _{OUT} <1μΑ	5	4.95		4.95		l	4.95	I I	
Output Voltage		۷он	V _{IN} = V _{DD}	10	9.95		9.95		l	9.95	l	
Output Vo.	rage		VIIN - VUU	15	14.95		14.95		_	14.95		v
Low-Level			 l _{OUT} <1μΑ	5	_	0.05		0.00	l	—	0.05	•
Output Vol	ltage	VOL	$V_{IN} = V_{DD}$, V_{SS}	10	—	0.05		0.00		—	0.05	
Cutput Vo.	rage			15	_	0.05	_	0.00		_	0.05	
			V _{OH} = 4.6V	5	- 0.61	_	- 0.51	- 1.0	ı	- 0.42	I I	
Output Hig	jh	ІОН	V _{OH} = 2.5V	5	- 2.5	_	- 2.1	- 4.0	—	- 1.7	—	
Current		Юн	V _{OH} = 9.5V	10	– 1.5		- 1.3	- 2.2	ı	- 1.1	—	
			$V_{IN} = V_{DD}$	15	- 4.0	_	- 3.4	- 9.0		- 2.8	_	
			$V_{OL} = 0.4V$	5	0.61	_	0.51	1.2	_	0.42	_	mA
Output Lov	N		$V_{OL} = 0.5V$	10	1.5	_	1.3	3.2	—	1.1	—	
Current		lOL	V _{OL} = 1.5V	15	4.0	_	3.4	12.0	—	2.8	—	
			$V_{IN} = V_{DD}$, V_{SS}									
			V _{OUT} = 0.5V, 4.5V	5	3.5	_	3.5	2.75	_	3.5	_	
lmmt Ilimb	\/- - 	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{OUT} = 1.0V, 9.0V	10	7.0	_	7.0	5.5	—	7.0	—	
Input High	voitage	VIH	V _{OUT} = 1.5V, 13.5V	15	11.0	_	11.0	8.25	—	11.0	—	
			I _{OUT} <1μΑ	1								.,
			V _{OUT} = 0.5V	5	_	1.5		2.25	1.5	<u> </u>	1.5	V
		l.,	V _{OUT} = 1.0V	10	l —	3.0	—	4.5	3.0	l —	3.0	
Input Low	voitage	VIL	V _{OUT} = 1.5V	15	_	4.0		6.75	4.0	—	4.0	
			I _{OUT} <1μΑ	1								
Input	H Level	۱н	V _{IH} = 18V	18	_	0.1	_	10-5			1.0	^
Current	L Level	IJL	V _{IL} = 0V	18		- 0.1	_	– 10 ^{– 5}	-0.1	_	- 1.0	μ A
Quiescent			$V_{IN} = V_{SS}$, V_{DD}	5	_	0.25	_	0.001	ı	_	7.5	
Device Current		IDD	* v M = v22' vDD	10	—	0.5		0.001	0.5	—	15	μ A
			•	15	_	1.0	_	0.002	1.0	—	30	

2

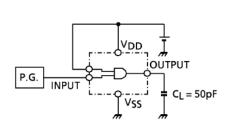
^{*} All valid input combinations.

DYNAMIC ELECTRICAL	. CHARACTERISTICS	Ta = 25°C,	$V_{SS} = 0V$, C_{I} :	= 50pF)
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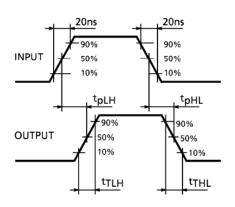
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time			5		70	200	
Output Transition Time	tTLH	_	10	_	35	100	ns
(Low to High)			15	_	30	80	
Output Transition Time (High to Low)			5		70	200	
	[†] THL	_	10	_	35	100	
			15	_	30	80	
	t _{pLH}	_	5		65	200	
Propagation Delay Time			10	_	30	100	
			15	_	25	80	
Propagation Delay Time	t _{pHL}	_	5		65	200	ns
			10	_	30	100	
			15	_	25	80	
Input Capacitance	CIN	_		5	7.5	pF	

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

TEST CIRCUIT



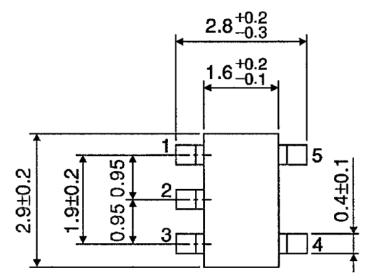
WAVEFORM

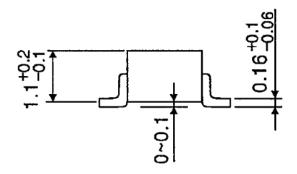


PACKAGE DIMENSIONS

SSOP5-P-0.95

Unit: mm





Weight: 0.016g (Typ.)

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