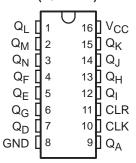
#### SN54HC4020, SN74HC4020 14-BIT ASYNCHRONOUS BINARY COUNTERS

SCLS158E - DECEMBER 1982 - REVISED SEPTEMBER 2003

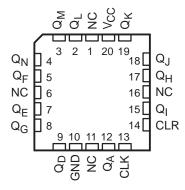
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>

SN54HC4020 . . . J OR W PACKAGE SN74HC4020 . . . D, DB, N, NS, OR PW PACKAGE (TOP VIEW)



- Typical t<sub>pd</sub> = 12 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

# SN54HC4020 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### description/ordering information

The 'HC4020 devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock (CLK) input when the clear (CLR) input goes high.

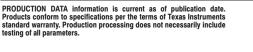
#### **ORDERING INFORMATION**

TA	PACKA	GE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC4020N	SN74HC4020N
		Tube of 40	SN74HC4020D	
	SOIC - D	Reel of 2500	SN74HC4020DR	HC4020
		Reel of 250	SN74HC4020DT	
-40°C to 85°C	SOP - NS	Reel of 2000	SN74HC4020NSR	HC4020
	SSOP - DB	Reel of 2000	SN74HC4020DBR	HC4020
		Tube of 90	SN74HC4020PW	
	TSSOP - PW	Reel of 2000	SN74HC4020PWR	HC4020
		Reel of 250	SN74HC4020PWT	
	CDIP – J	Tube of 25	SNJ54HC4020J	SNJ54HC4020J
−55°C to 125°C	CFP – W	Tube of 150	SNJ54HC4020W	SNJ54HC4020W
	LCCC – FK	Tube of 55	SNJ54HC4020FK	SNJ54HC4020FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



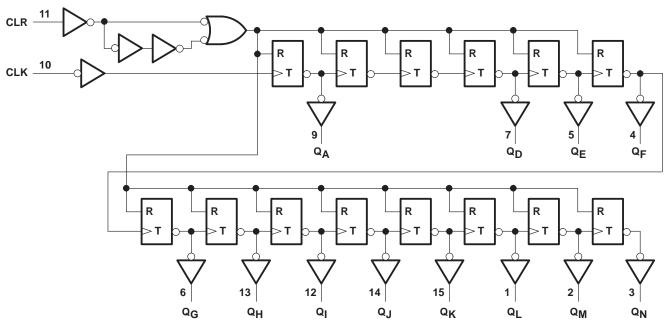
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# FUNCTION TABLE (each buffer)

INP	UTS	FUNCTION
CLK	CLR	FUNCTION
1	L	No change
$\downarrow$	L	Advance to next stage
Х	Н	All outputs L

#### logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see	e Note 1)	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	(see Note 1)	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$ .		±25 mA
Continuous current through V <sub>CC</sub> or GND		±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): I	D package	73°C/W
	DB package	82°C/W
J	N package	67°C/W
J	NS package	64°C/W
l l	PW package	108°C/W
Storage temperature range, T <sub>sto</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

			SN	54HC40	20	SN	74HC40	20	LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
ViH	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		V <sub>CC</sub> = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		VCC = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
		V <sub>CC</sub> = 2 V			1000			1000	
Δt/Δν	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			.,	Т	A = 25°C	;	SN54H	C4020	SN74H0	C4020	
PARAMETER	TEST CO	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			2 V	1.9	1.998		1.9		1.9		
		$I_{OH} = -20  \mu A$	4.5 V	4.4	4.499		4.4		4.4		
∨он	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
	VI = VIH or VIL		2 V		0.002	0.1		0.1		0.1	
		I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
VOL			6 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
ICC	$V_I = V_{CC}$ or 0,	I <sub>O</sub> = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF

#### SN54HC4020, SN74HC4020 14-BIT ASYNCHRONOUS BINARY COUNTERS

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# timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			\ ,_	T <sub>A</sub> = 1	25°C	SN54H	C4020	SN74H	C4020	
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
					5.5		3.7		4.3	
f <sub>clock</sub> Clock frequency			4.5 V		28		19		22	MHz
			6 V		33		22		25	
			2 V	90		135		115		
	D. des dessifica	CLK high or low	4.5 V	18		27		23		
١.			6 V	15		23		20		
t <sub>W</sub>	Pulse duration	CLR high	2 V	70		105		90		ns
			4.5 V	14		21		18		
			6 V	12		18		25		
			2 V	60		90		75		
t <sub>su</sub>	Setup time, CLR inactive before CLK $\downarrow$		4.5 V	12		18		15		ns
			6 V	10		15		13		

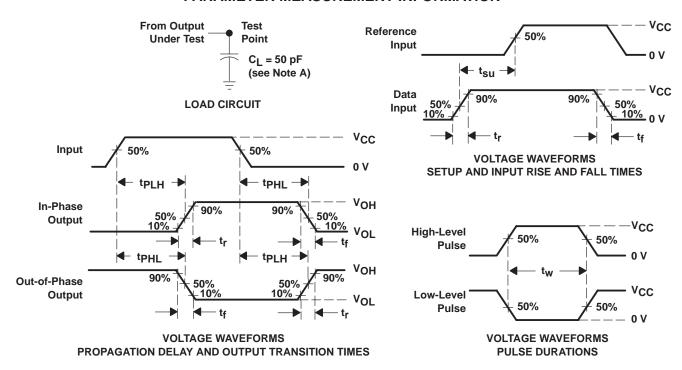
# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

545445755	FROM	то	,,	T	λ = 25°C	;	SN54H	C4020	SN74H	C4020	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	5.5	10		3.7		4.3		
f <sub>max</sub>			4.5 V	28	45		19		22		MHz
			6 V	33	53		22		25		
			2 V		62	150		225		190	
<sup>t</sup> pd	CLK	QA	4.5 V		16	30		45		38	ns
·			6 V		12	26		38		32	
			2 V		63	140		210		175	
<sup>t</sup> PHL	CLR	Any	4.5 V		17	28		42		35	ns
			6 V		13	24		36		30	
			2 V		28	75		110		95	
t <sub>t</sub>		Any	4.5 V		8	15		22		19	ns
·			6 V		6	13		19		16	

### operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Ср	Power dissipation capacitance	No load	88	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_r = 6 \ ns$ ,  $t_f = 6 \ ns$ .
- C. For clock inputs, f<sub>max</sub> is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
85003012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8500301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
8500301FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN54HC4020J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74HC4020D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC4020N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74HC4020NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC4020NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





5-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74HC4020PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4020PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54HC4020FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC4020J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54HC4020W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



#### **PACKAGE OPTION ADDENDUM**

5-Sep-2011

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54HC4020, SN74HC4020:

Catalog: SN74HC4020

www.ti.com

Military: SN54HC4020

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

Military - QML certified for Military and Defense Applications

#### **PACKAGE MATERIALS INFORMATION**

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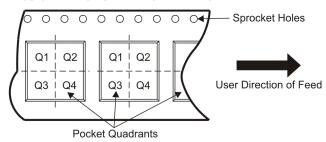
#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All differsions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4020DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4020NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC4020PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

A MI GITTOTO GITO TOTALING.								
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74HC4020DR	SOIC	D	16	2500	333.2	345.9	28.6	
SN74HC4020NSR	SO	NS	16	2000	346.0	346.0	33.0	
SN74HC4020PWR	TSSOP	PW	16	2000	346.0	346.0	29.0	
SN74HC4020PWT	TSSOP	PW	16	250	346.0	346.0	29.0	

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F16)

### CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



## FK (S-CQCC-N\*\*)

#### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE

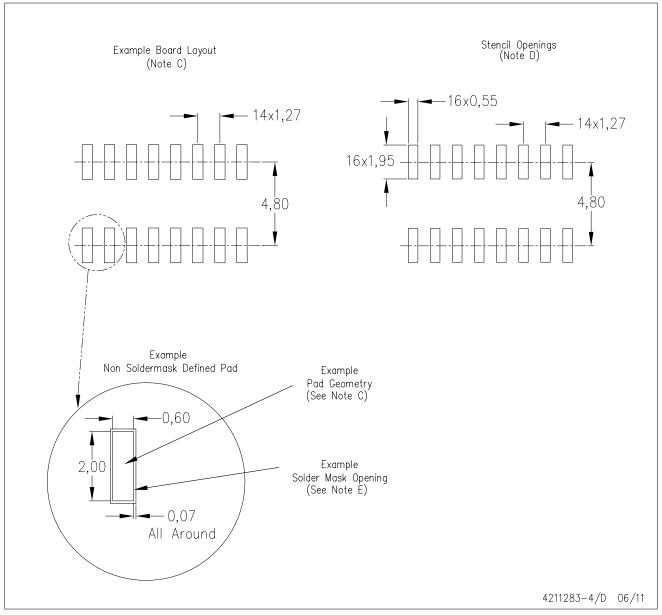


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

#### PLASTIC SMALL OUTLINE

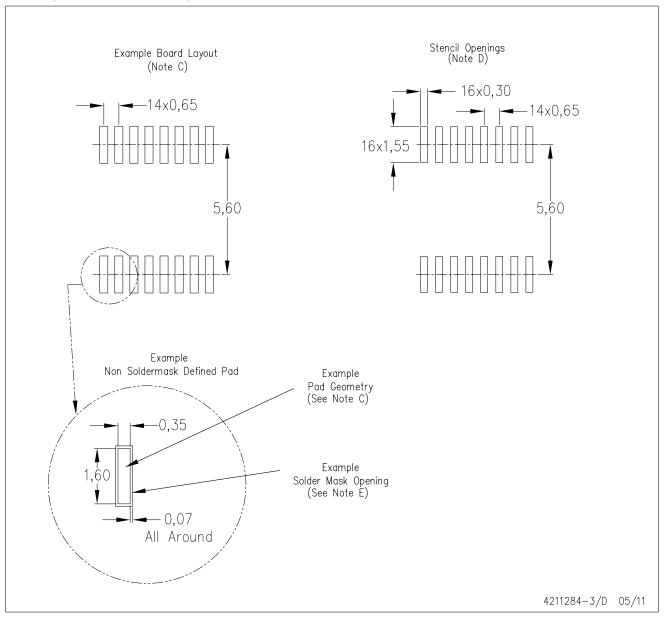


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

#### NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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