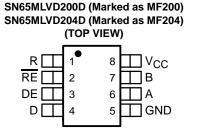
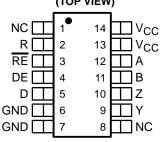
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- Low-Voltage Differential 30- Ω Line Drivers and Receivers for Signaling Rates[†] up to 100 Mbps
- **Power Dissipation at 100 Mbps** - Driver: 50 mW Typical
 - Receiver: 30 mW Typical
- Meets or Exceeds Current Revision of M-LVDS Standard TIA/EIA-899 for **Multipoint Data Interchange**
- **Controlled Driver Output Voltage Transition** • **Times for Improved Signal Quality**
- -1-V to 3.4-V Common-Mode Voltage Range Allows Data Transfer With up to 2 V of **Ground Noise**
- Type-1 Receivers Incorporate 25 mV of **Hysteresis**

- **Type-2 Receivers Provide an Offset** (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions
- **Operates From a Single 3.3-V Supply**
- **Propagation Delay Times Typically 2.3 ns** for Drivers and 5 ns for Receivers
- Power-Up/Down Glitch-Free Driver
- **Driver Handles Operation Into a Continuous Short Circuit Without Damage**
- **Bus Pins High Impedance When Disabled** or $V_{CC} \le 1.5 V$
- 200-Mbps Devices Available (SN65MLVD201, 203, 206, and 207)

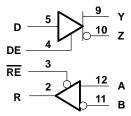


SN65MLVD202D (Marked as MLVD202) SN65MLVD205D (Marked as MLVD205) (TOP VIEW)



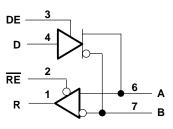
NC - No internal connection

SN65MLVD202, SN65MLVD205



logic diagram (positive logic)

SN65MLVD200, SN65MLVD204



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†]The signaling rate of a line is the number of voltage transitions that are made per second expressed in bps (bits per second) units.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description

This series of SN65MLVD20x devices are low-voltage differential line drivers and receivers complying with the proposed multipoint low-voltage differential signaling (M-LVDS) standard (TIA/EIA-899). These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. Driver output current has been increased to support doubly-terminated, $50-\Omega$ load multipoint applications. Driver output slew rates are optimized for signaling rates up to 100 Mbps.

Types 1 and 2 receivers are available. Both types of receivers operate over a common-mode voltage range of -1 V to 3.4 V to provide increased noise immunity in harsh electrical environments. Type-1 receivers have their differential input voltage thresholds near zero volts (±50 mV), and include 25 mV of hysteresis to prevent output oscillations in the presence of noise. Type-2 receivers include an offset threshold to detect open-circuit, idle-bus, and other fault conditions, and provide a known output state under these conditions.

The intended application of these devices is in half-duplex or multipoint baseband data transmission over controlled impedance media of approximately $100 \cdot \Omega$ characteristic impedance. The transmission media may be printed circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application-specific characteristics).

NOMINAL SIGNALING RATE, Mbps	FOOTPRINT	RECEIVER TYPE	PART NUMBER [†]
100	SN75176	Type 1	SN65MLVD200D
100	SN75ALS180	Type 1	SN65MLVD202D
100	SN75176	Туре 2	SN65MLVD204D
100	SN75ALS180	Туре 2	SN65MLVD205D

AVAILABLE OPTIONS

These devices are characterized for operation from -40°C to 85°C.

[†] The D package is available taped and reeled. Add the R suffix to the device type (e.g., SN65MLVD200DR)

Function Tables

TYPE-1 RECEIVER (200, 202)			
INPUTS		OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
V _{ID} ≥ 50 mV	L	н	
–50 mV < V _{ID} < 50 mV	L	?	
V _{ID} ≤ −50 mV	L	L	
Х	Н	Z	
Х	Open	Z	
Open Circuit	L	?	

TYPE-2 RECEIV	TYPE-2 RECEIVER (204, 205)				
INPUTS		OUTPUT			
$V_{ID} = V_A - V_B$	RE	R			
V _{ID} ≥ 150 mV	L	Н			
50 mV < V _{ID} < 150 mV	L	?			
$V_{ID} \le 50 \text{ mV}$	L	L			
Х	Н	Z			
Х	Open	Z			
Open Circuit	L	L			

DRIVER						
INPUT	ENABLE	OUTP	UTS			
D	DE	DE A OR Y B OR Z				
L	Н	L	Н			
Н	Н	Н	L			
OPEN	Н	L	н			
Х	OPEN	Z	Z			
Х	L	Z	Z			

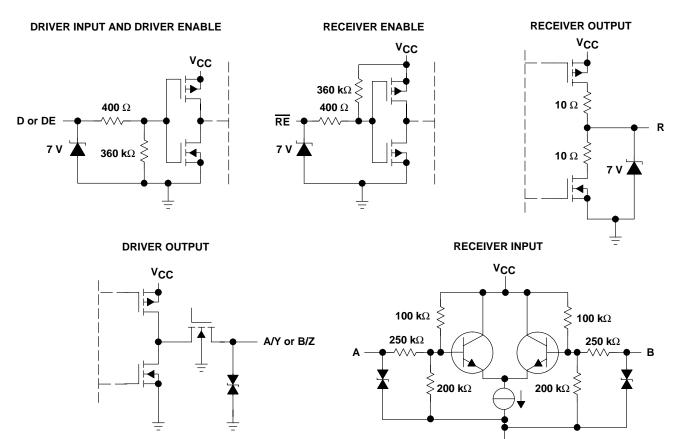
H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate



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equivalent input and output schematic diagrams





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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{CC} (see Note 1)	-0.5 V to 4 V
Input voltage range: D, DE, RE	
A, B (200, 204)	
A, B (202, 205)	
Output voltage range: R	
Y, Z, A, or B	
Electrostatic discharge: Human body model (see Note 2)	A, B, Y, or Z ±3 kV
	All pins ±2 kV
Charged-device model (see Note 3)	All pins±500 V
Continuous power dissipation	(see Dissipation Rating table)
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seco	nds 260°C

[†] Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.

3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING

PACKAGE	T _A ≤ 25°C POWER RATING	OPERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
D(8)	725 mW	5.8 mW/°C	377 mW
D(14)	950 mW	7.6 mW/°C	494 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	3	3.3	3.6	V
High-level input voltage, VIH	2		VCC	V
Low-level input voltage, VIL	0		0.8	V
Magnitude of differential input voltage, VID	0.05		VCC	V
Voltage at any bus terminal, V _A , V _Y , V _{Z, or} V _B	-1.4		3.8	V
Common-mode input voltage V _{CM} , (V _A + V _B)/2	-1		3.4	V
Receiver load capacitance, CL	5		15	pF
Operating free-air temperature, T _A	-40		85	°C



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device electrical characteristics over recommended operating conditions (unless otherwise noted)

		PARAMETER	TEST CONDITIONS	MIN [†]	TYP‡	MAX	UNIT
		Receiver disabled and driver enabled	RE and DE at V _{CC} , R _L = 50 Ω, All others open		13	22	
		Driver and receiver disabled	\overline{RE} at V _{CC} , DE at 0 V, R _L = No load, All others open		1	7	
ICC	Supply current	Receiver enabled and driver enabled	RE at 0 V, DE at V _{CC} , R _L = 50 Ω, All others open, No receiver load		16	26	mA
		Receiver enabled and driver disabled	RE at 0 V, DE at 0 V, All others open, No receiver load		4	11	

[†] The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet. [‡] All typical values are at 25°C and with a 3.3-V supply voltage.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN†	ΤΥΡ [‡] ΜΑΧ	UNIT
V _{AB} or V _{YZ}	Differential output voltage magnitude	See Figure 2	480	650	mV
$\Delta V_{AB} $ or $\Delta V_{YZ} $	Change in differential output voltage magnitude between logic states	See Figure 2	-50	50	mV
VOS(SS)	Steady-state common-mode output voltage		0.8	1.2	V
ΔVOS(SS)	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50	50	mV
VOS(PP)	Peak-to-peak common-mode output voltage			150	mV
V _{A(OC)} or V _{Y(OC)}	Maximum steady-state open-circuit output voltage	0.5.7	0	2.4	V
V _{B(OC)} or V _{Z(OC)}	Maximum steady-state open-circuit output voltage	See Figure 7	0	2.4	V
V _{P(H)}	Voltage overshoot, low-to-high level output			1.2V _{SS}	V
V _{P(L)}	Voltage overshoot, high-to-low level output	See Figure 5	-0.2V _{SS}		V
Чн	High-level input current	$V_{IH} = 2 V$	0	10	μA
۱ _{IL}	Low-level input current	V _{IL} = 0.8 V	0	10	μA
los	Differential short-circuit output current	See Figure 4		24	mA
loz	High-impedance state output current (driver only)	$-1.4 \text{ V} \le (\text{V}_{Y} \text{ or } \text{V}_{Z}) \le 3.8 \text{ V},$ Other output at 1.2 V	-15	10	μΑ
lO(OFF)	Power-off output current (driver only)	$\begin{array}{l} -1.4 \ V \leq (V_Y \ or \ V_Z) \leq 3.8 \ V, \\ V_{CC} \leq 1.5 \ V, \\ Other \ output \ at \ 1.2 \ V \end{array}$	-10	10	μA

[†]The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

[‡] All typical values are at 25°C and with a 3.3-V supply voltage.



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receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
M	Desitive raise differential is not value as three held	Type 1				50	
V _{IT+}	Positive-going differential input voltage threshold	Type 2				150	mV
N.—		Type 1	See Figure 8,	-50			
V _{IT} –	Negative-going differential input voltage threshold	Type 2	Table 1 and Table 2	50			mV
		Type 1			25		
VID(HYS)	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$	Type 2			0		mV
VOH	High-level output voltage		I _{OH} = –8 mA	2.4			V
VOL	Low-level output voltage		I _{OL} = 8 mA			0.4	V
IIН	High-level input current		V _{IH} = 2 V	-10		0	μA
١ _{IL}	Low-level input current		V _{IL} = 0.8 V	-10		0	μA
IOZ	High-impedance output current		$V_{O} = 0 V \text{ or } 3.6 V$	-10		15	μA

[†] All typical values are at 25°C and with a 3.3-V supply voltage.

bus input and output electrical characteritics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ΤΥΡ [†] ΜΑΧ	UNIT
		V _A = 3.8 V, V _B = 1.2 V	0	32	
IA	Receiver input or transceiver input/output current	$V_A = 0 V \text{ or } 2.4 V$, $V_B = 1.2 V$	-20	20	μA
	oution	$V_A = -1.4 V$, $V_B = 1.2 V$	-32	0	
	5 · · · · · · · · · · · · · · · · · · ·	$V_B = 3.8 V$, $V_A = 1.2 V$	0	32	
IB	Receiver input or transceiver input/output current	$V_B = 0 \text{ V or } 2.4 \text{ V}, V_A = 1.2 \text{ V}$	-20	20	μA
		$V_{B} = -1.4 V$, $V_{A} = 1.2 V$	-32	0	
I _{AB}	Receiver input or transceiver input/output differential current (I _A – I _B)	$V_A = V_B, \qquad -1.4 \le V_A \le 3.8 \text{ V}$	-4	4	μΑ
		$V_{\mbox{\scriptsize A}} = 3.8 \ \mbox{V}, \qquad \qquad V_{\mbox{\scriptsize B}} = 1.2 \ \mbox{V}, V_{\mbox{\scriptsize CC}} \leq 1.5 \ \mbox{V}$	0	32	
lA(OFF)	Receiver input or transceiver input/output power-off current	$V_{A} = 0 \text{ V or } 2.4 \text{ V}, V_{B} = 1.2 \text{ V}, V_{CC} \leq 1.5 \text{ V}$	-20	20	μA
· · ·		$V_{A} = -1.4 \text{ V}, \qquad \qquad V_{B} = 1.2 \text{ V}, V_{CC} \leq 1.5 \text{ V}$	-32	0	
	5 · · · · · · · · · · · · · · · · · · ·	$V_B = 3.8 \text{ V}, \qquad \qquad V_A = 1.2 \text{ V}, V_{CC} \leq 1.5 \text{ V}$	0	32	
^I B(OFF)	Receiver input or transceiver input/output power-off current	$V_B = 0 \text{ V or } 2.4 \text{ V}, V_A = 1.2 \text{ V}, V_{CC} \leq 1.5 \text{ V}$	-20	20	μA
		$V_B = -1.4 \text{ V}, \qquad V_A = 1.2 \text{ V}, V_{CC} \leq 1.5 \text{ V}$	-32	0	
IAB(OFF)	Receiver input or transceiver input/output power-off differential current $(I_A - I_B)$	$V_A = V_B, \qquad -1.4 \leq V_A \leq 3.8 \text{ V}, V_{CC} \leq 1.5 \text{ V}$	-4	4	μΑ
C _A	Receiver input, driver high-impedance output, or transceiver input/output	$V_A = 0.4 \sin(2E8\pi t) + 0.5$, $V_B = 1.2 V$		3	pF
CB	capacitance	$V_B = 0.4 \sin(2E8\pi t) + 0.5$, $V_A = 1.2 V$		3	pF

[†] All typical values are at 25°C and with a 3.3-V supply voltage.



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driver switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output		1.6	2.3	4.1	ns
^t PHL	Propagation delay time, high-to-low-level output		1.6	2.3	4.1	ns
t _r	Differential output signal rise time	t See Figure 6	1.5	2	3	ns
t _f	Differential output signal fall time	See Figure 5	1.5	2	3	ns
^t sk(p)	Pulse skew (tpHL tpLH)			30		ps
^t sk(pp)	Part-to-part skew (see Note 4)				900	ps
^t PZH	Propagation delay time, high-impedance-to-high-level output		1.5	3.7	6.5	ns
^t PZL	Propagation delay time, high-impedance-to-low-level output		1.5	3.7	6.5	ns
^t PHZ	Propagation delay time, high-level-to-high-impedance output	See Figure 6	1.3	3.5	6.8	ns
^t PLZ	Propagation delay time, low-level-to-high-impedance output		1.8	3.5	6.1	ns
^t jit(per)	Period jitter, rms (1 standard deviation) (see Notes 5 and 6)	50-MHz clock input (see Figure 8)		23		ps
^t jit(cc)	Cycle-to-cycle jitter, peak (see Notes 5 and 6)	50-MHz clock input (see Figure 8)		180		ps
^t jit(pp)	Peak-to-peak jitter, (see Notes 5, 7, and 8)	100 Mbps 2 ¹⁵ –1 PRBS input (see Figure 8)		210		ps

[†] All typical values are at 25°C and with a 3.3-V supply voltage.

NOTES: 4. t_{Sk(DD)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5. Jitter parameters are based on design and characterization. Stimulus system jitter of 11 ps t_{jit(per)}, 43 ps t_{jit(pc)}, or 54 ps t_{jit(pp)} have been subtracted from the values.

6. Input voltage = 0 V to V_{CC}, t_{f} = t_f \leq 1 ns (20% to 80%), measured over 30k samples.

7. Input voltage = 0 V to V_{CC}, $t_f = t_f \le 1$ ns (20% to 80%), measured over 100k samples.

8. Peak-to-peak jitter includes jitter due to pulse skew (tsk(p)).



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receiver switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
^t PLH	Propagation delay time, low-to-high-level output		3	5	6.7	ns		
^t PHL	Propagation delay time, high-to-low-level output		3	4.6	6.7	ns		
^t sk(p)	Pulse skew (tp _{HL} tp _{LH})			400		ps		
tsk(pp)	Part-to-part skew (see Note 9)	C _L = 5 pF, See Figure 10			1.5	ns		
t _r	Output signal rise time		0.8	1.4	2	ns		
t _f	Output signal fall time			0.8	1.5	2	ns	
^t PLH	Propagation delay time, low-to-high-level output		3.4	5.8	9	ns		
^t PHL	Propagation delay time, high-to-low-level output		3.4	5.4	9	ns		
^t sk(p)	Pulse skew (tp _{HL} tp _{LH})			400		ps		
^t sk(pp)	Part-to-part skew (see Note 9)	$C_L = 15 pF$, See Figure 10			2.5	ns		
t _r	Output signal rise time		1	2	2.6	ns		
t _f	Output signal fall time		1	1.4	2.6	ns		
^t PHZ	Propagation delay time, high-level-to-high-impedance output		4.5	6	15	ns		
^t PLZ	Propagation delay time, low-level-to-high-impedance output			2	3.4	5	ns	
^t PZH	Propagation delay time, high-impedance-to-high-level output	See Figure 11	3.5	9.8	15	ns		
^t PZL	Propagation delay time, high-impedance-to-low-level output				8.7	15	ns	
_	Period jitter, rms (1 standard deviation)	ation) 50-MHz clock input Type			10			
^t jit(per)	(see Notes 10 and 11)	(see Figure 12)	Type 2		10		ps	
		50-MHz clock input	Type 1		93			
^t jit(cc)	Cycle-to-cycle jitter, peak (see Notes 10 and 11)	(see Figure 12) Type 2			86		ps	
		100 Mbps 2 ¹⁵ –1 PRBS	Type 1		850	ps		
^t jit(pp)	Peak-to-peak jitter, (see Notes 10, 12, and 13)	input (see Figure 12)	Type 2		790			

[†] All typical values are at 25°C and with a 3.3-V supply voltage.

NOTES: 9. t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

10. Jitter parameters are based on design and characterization. Stimulus system jitter of 11 ps tjit(per), 43 ps tjit(cc), or 54 ps tjit(pp) have been subtracted from the values.

- 11. Differential input voltage = 250 mV_{p-p} (Type 1) or 500 mV_{p-p} (Type 2), V_{CM} = 1 V, $t_r = t_f \le 1$ ns (20% to 80%), measured over 30k samples.
- 12. Differential input voltage = 250 mV_{p-p} (Type 1) or 500 mV_{p-p} (Type 2), V_{CM} = 1 V, t_f = t_f \leq 1 ns (20% to 80%), measured over 100k samples.

13. Peak-to-peak jitter includes jitter due to pulse skew (tsk(p)).



SN65MLVD200, SN65MLVD202 SN65MLVD204, SN65MLVD205 MULTIPOINT-LVDS LINE DRIVERS AND RECEIVERS SLLS463E - SEPTEMBER 2001 - REVISED JUNE 2003

PARAMETER MEASUREMENT INFORMATION

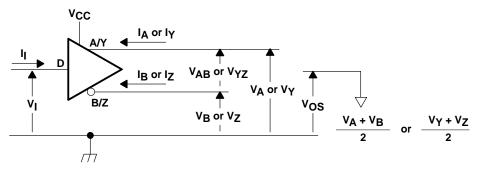
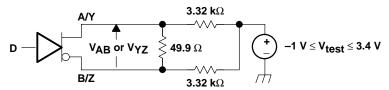
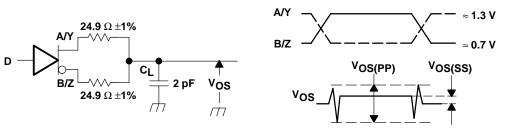


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.25 Mpps, pulse width = 500 \pm 10 ns. CL includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of VOS(PP) is made on test equipment with a -3-dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

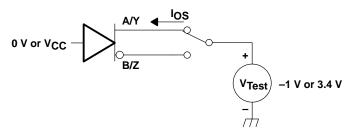
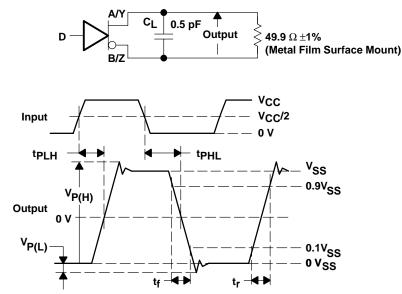


Figure 4. Driver Short-Circuit Test Circuit



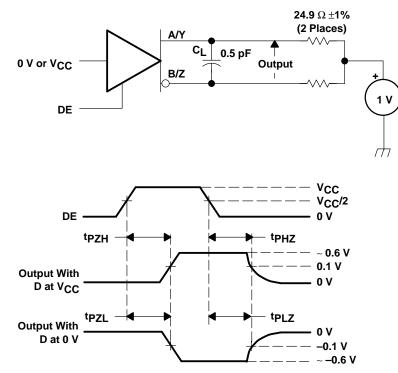
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PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ±0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE: All input pulses are supplied by a generator having the following characteristics: t_f or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.25 Mpps, pulse width = 500 ±10 ns. CL includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Driver Enable and DIsable Time Circuit and Definitions



SN65MLVD200, SN65MLVD202 SN65MLVD204, SN65MLVD205 MULTIPOINT-LVDS LINE DRIVERS AND RECEIVERS SLLS463E - SEPTEMBER 2001 - REVISED JUNE 2003

PARAMETER MEASUREMENT INFORMATION

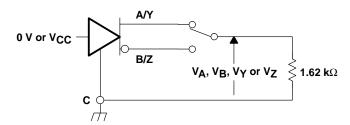
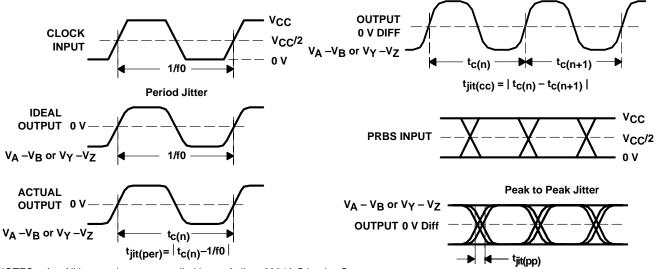


Figure 7. Maximum Steady-State Output Voltage Test Circuit



NOTES: A. All input pulses are supplied by an Agilent 8304A Stimulus System.

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

- C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 200Mbps 2¹⁵–1 PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

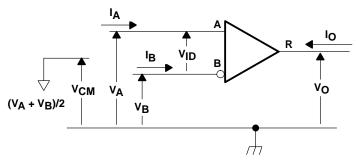


Figure 9. Receiver Voltage and Current Definitions



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PARAMETER MEASUREMENT INFORMATION

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER OUTPUT
VA	VB	V _{ID}	V _{CM}	٧ ₀
3.425 V	3.375 V	50 mV	3.4 V	Н
3.375 V	3.425 V	–50 mV	3.4 V	L
–0.975 V	–1.025 V	50 mV	–1.0 V	Н
–1.025 V	–0.975 V	–50 mV	–1.0 V	L
3.800 V	3.000 V	800 mV	3.4 V	Н
3.000 V	3.800 V	–800 mV	3.4 V	L
–0.600 V	-1.400 V	800 mV	–1.0 V	Н
-1.400 V	-1.400 V -0.600 V -800 mV		–1.0 V	L

Table 1. Type-1 Receiver Input Threshold Test Voltages

NOTE: H= high level, L = low level. Output state assumes receiver is enabled (\overline{RE} is Low).

Table 2. Type-2 Receiver Input Threshold Test Voltages

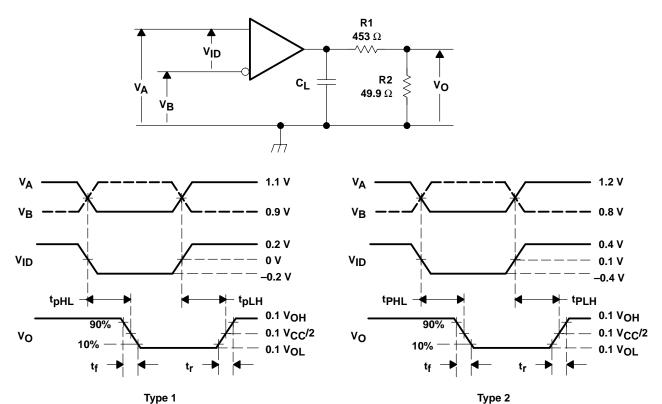
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER OUTPUT
VA	٧ _B	V _{ID}	VCM	٧ ₀
3.475 V	3.325 V	150 mV	3.4 V	Н
3.425 V	3.375 V	50 mV	3.4 V	L
–0.925 V	–1.075 V	150 mV	-1.0 V	Н
–0.975 V	–1.025 V	50 mV	-1.0 V	L
3.800 V	3.000 V	800 mV	3.4 V	Н
3.000 V	3.800 V	–800 mV	3.4 V	L
–0.600 V	-1.400 V	800 mV	–1.0 V	Н
-1.400 V	–0.600 V	–800 mV	–1.0 V	L

NOTE: H= high level, L = low level. Output state assumes receiver is enabled (\overline{RE} is Low).



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PARAMETER MEASUREMENT INFORMATION



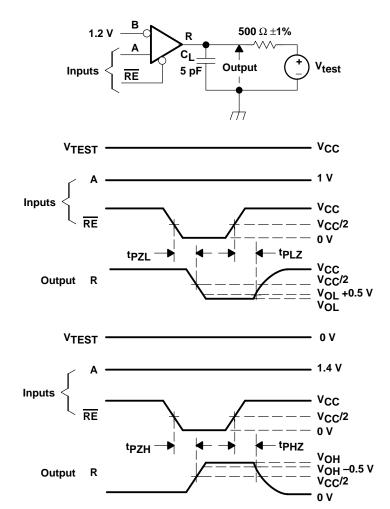
NOTES: A. All input pulses are supplied by a generator having the following characteristics: tr or tf ≤1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = $0.5 \pm 0.05 \,\mu$ s.

- B. Resistors are 1% tolerance, metal film, and surface mount.
- C. CL is 20% tolerance, low-loss ceramic, and surface mount.
- D. R1 and C_L are located within 2 cm of the D.U.T.
- E. R2 is located within 15 cm of the D.U.T.

Figure 10. Receiver Timing Test Circuit and Waveforms



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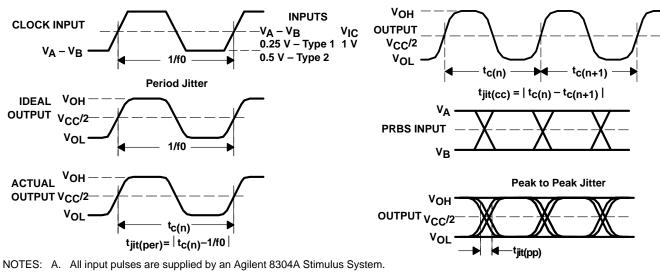
PARAMETER MEASUREMENT INFORMATION

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.25 Mpps, pulse width = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms



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PARAMETER MEASUREMENT INFORMATION

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

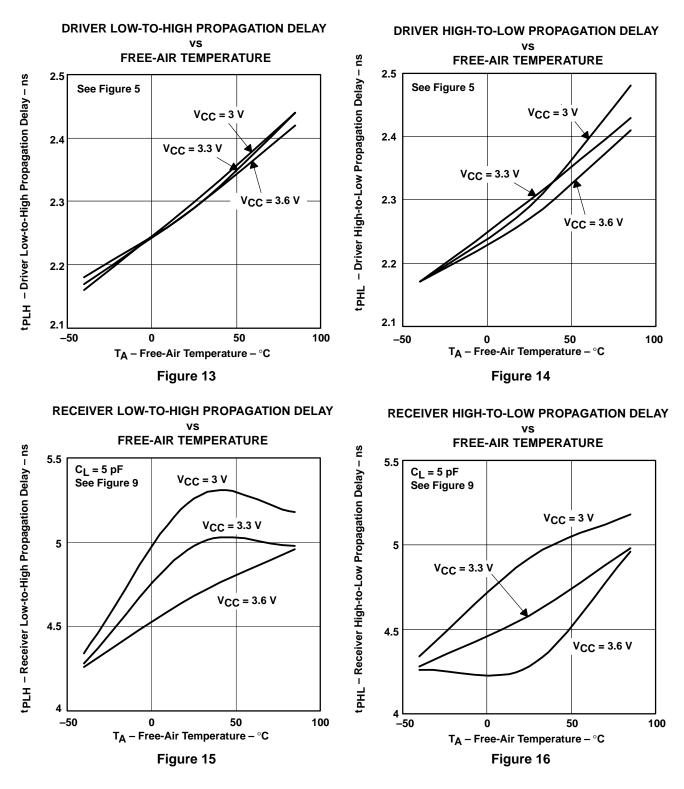
C. Period jitter is measured using a 100 MHz 50 \pm 1% duty cycle clock input.

D. Peak-to-peak jitter is measured using a 200Mbps 2¹⁵–1 PRBS input.

Figure 12. Receiver Jitter Measurement Waveforms



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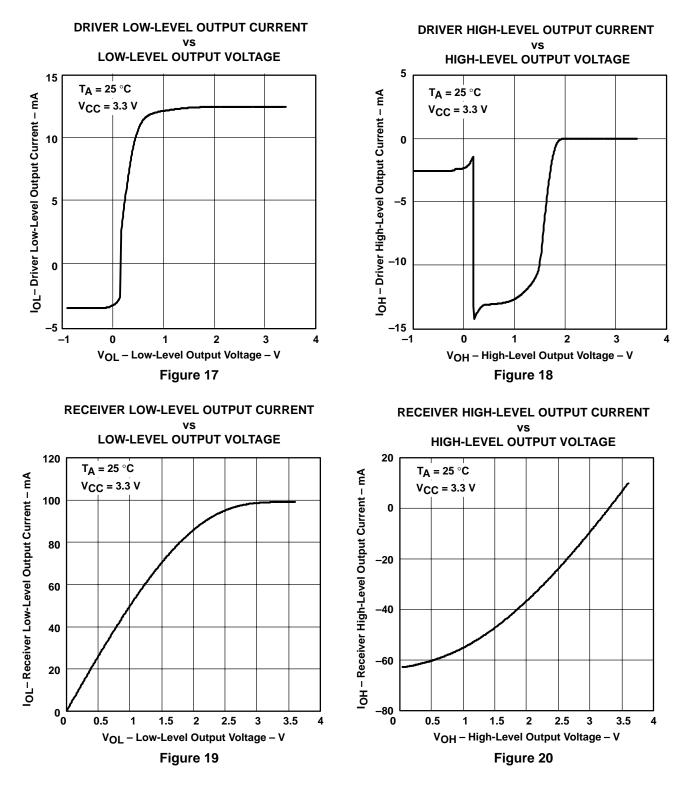


TYPICAL CHARACTERISTICS



SN65MLVD200, SN65MLVD202 SN65MLVD204, SN65MLVD205 MULTIPOINT-LVDS LINE DRIVERS AND RECEIVERS SLLS463E - SEPTEMBER 2001 - REVISED JUNE 2003

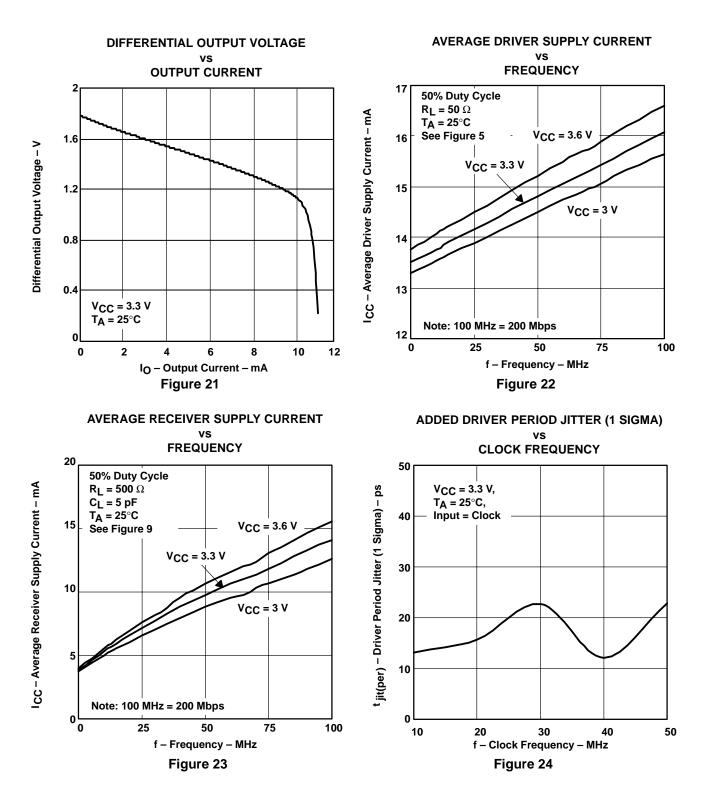






SN65MLVD200, SN65MLVD202 SN65MLVD204, SN65MLVD205 MULTIPOINT-LVDS LINE DRIVERS AND RECEIVERS SLLS463E - SEPTEMBER 2001 - REVISED JUNE 2003

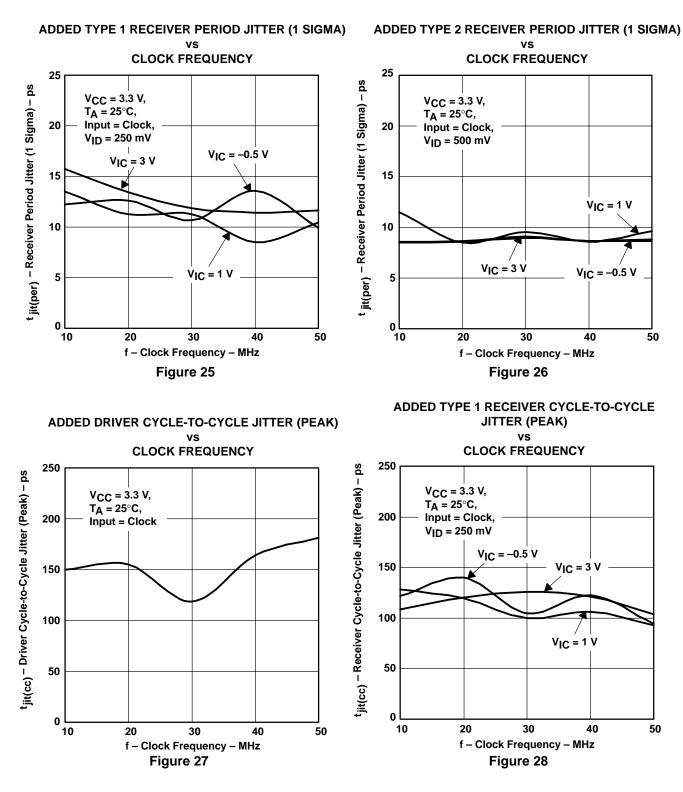
TYPICAL CHARACTERISTICS





SN65MLVD200, SN65MLVD202 SN65MLVD204, SN65MLVD205 MULTIPOINT–LVDS LINE DRIVERS AND RECEIVERS SLLS463E – SEPTEMBER 2001 – REVISED JUNE 2003

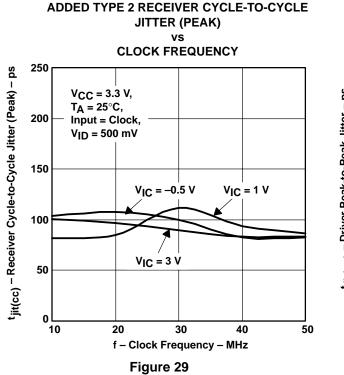
TYPICAL CHARACTERISTICS

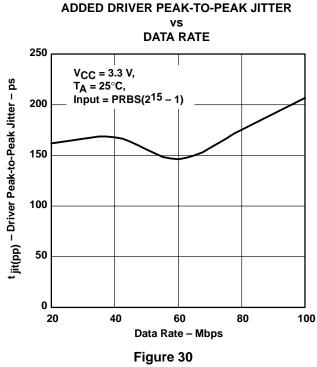




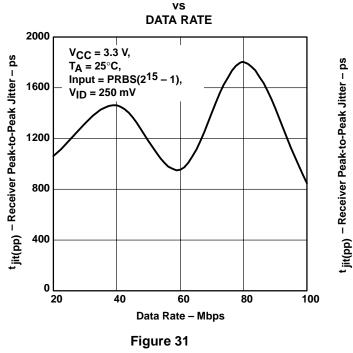
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TYPICAL CHARACTERISTICS



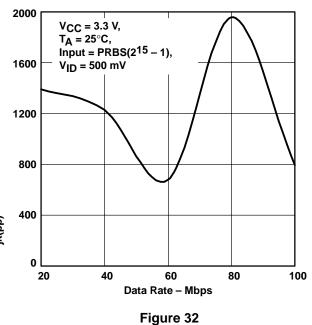


ADDED TYPE 2 RECEIVER PEAK-TO-PEAK JITTER vs



ADDED TYPE 1 RECEIVER PEAK-TO-PEAK JITTER

DATA RATE





SN65MLVD200, SN65MLVD202 SN65MLVD204, SN65MLVD205 MULTIPOINT-LVDS LINE DRIVERS AND RECEIVERS SLLS463E - SEPTEMBER 2001 - REVISED JUNE 2003

Output High

APPLICATION INFORMATION

Type-1 and Type-2 receivers

Receiver Type

The M-LVDS standard defines Type-1 and Type-2 receivers. Type-1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. Type-1 receivers maximize the differential noise margin and are intended for maximum signaling rates. Type-2 receivers are intended for control signals and slower signaling rates. The impact on receiver output by the offset input can be seen in Table 3 and Figure 33.

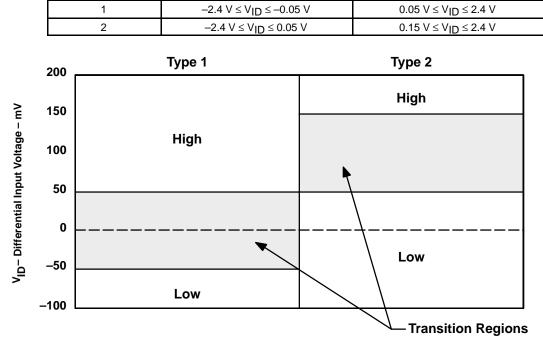


Table 3. M-LVDS Receiver Input Voltage Threshold Requirements

Output Low

Figure 33. Receiver Differential Input Voltage Showing Transition Region



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APPLICATION INFORMATION

comparison of M-LVDS with RS-485

RS-485 applications are similar to M-LVDS. The two standards define balanced multipoint systems with some basic architecture changes due to the different applications. Table 4 gives a high-level comparison of the two different technologies.

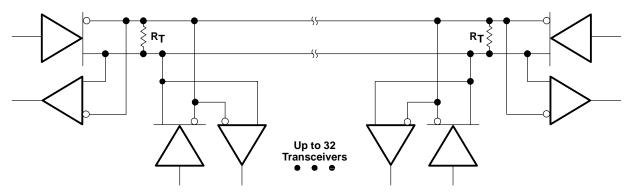
Table 4. Comparison Between M-LVDS and RS-485 Standards

	Number of Loads	Differential Voltage Range	Common-Mode Voltage Range	Maximum Signaling Rate (Mbps)	Receiver Minimum Threshold		
RS-485	32	1.5 V to 5 V	-7 V to 12 V	50 Mbps	±200 mV		
M-LVDS	32	480 mV to 650 mV	-1 V to 3.4 V	500 Mbps	±50 mV		

It can be seen that with the greater differential output voltage and common-mode voltage range of the RS-485-type device, it can handle longer signaling distances where M-LVDS offers ten times the signaling rate of RS-485.

SN65MLVD200

SN65MLVD200



NOTE A: The line should be terminated at both ends in its characteristic impedance (R_T = Z_O). Stub lengths off the main line should be kept as short as possible.

Figure 34. Typical Application Circuit



28-Aug-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65MLVD200D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202DG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202DR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202DRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205DG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is



PACKAGE OPTION ADDENDUM

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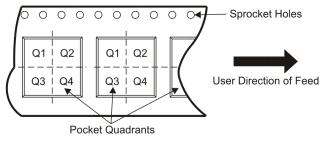
TEXAS INSTRUMENTS www.ti.com

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

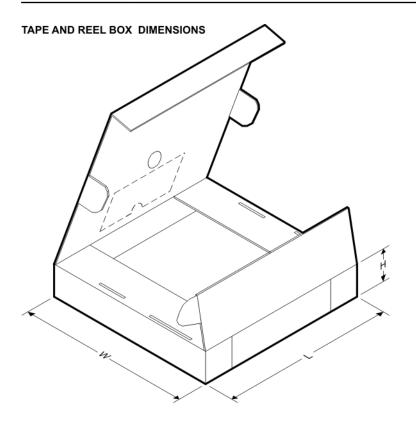


*All	*All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	SN65MLVD200DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
	SN65MLVD202DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
	SN65MLVD204DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

9-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD200DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65MLVD202DR	SOIC	D	14	2500	333.2	345.9	28.6
SN65MLVD204DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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