SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

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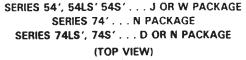
'160,'161,'LS160A,'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR '162,'163,'LS162A,'LS163A,'S162,'S163 . . . FULLY SYNCHRONOUS COUNTERS

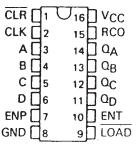
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

		TYPICAL	
	TYPICAL PROPAGATION	MAXIMUM	TYPICAL
TYPE	TIME, CLOCK TO	CLOCK	POWER
	Q OUTPUT	FREQUENCY	DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

description

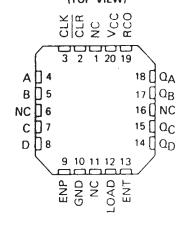
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160,'162,'LS160A,'LS162A, and 'S162 are decade counters and the '161,'163,'LS161A,'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.





NC-No internal connection

SERIES 54LS', 54S'...FK PACKAGE (TOP VIEW)



NC-No internal connection

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.



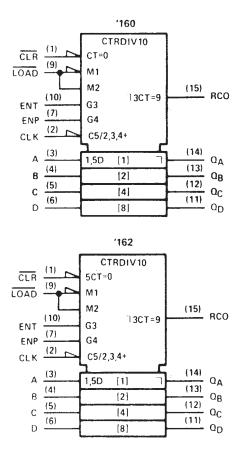
SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

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The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

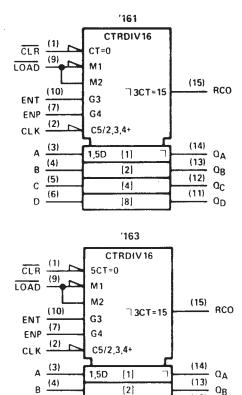
'LS160A thru 'LS163A,'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.



[4]

[8]

(5)

(6)

С

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(12)

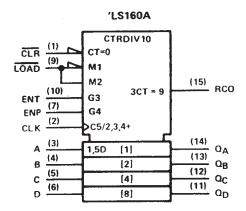
(11)

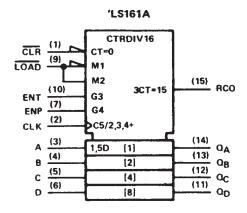
 α_{C}

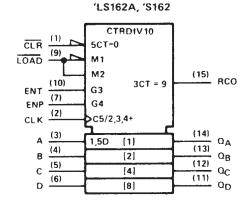
 Q_D

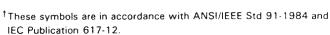


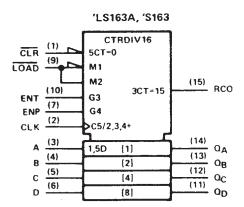
logic symbols (continued)†





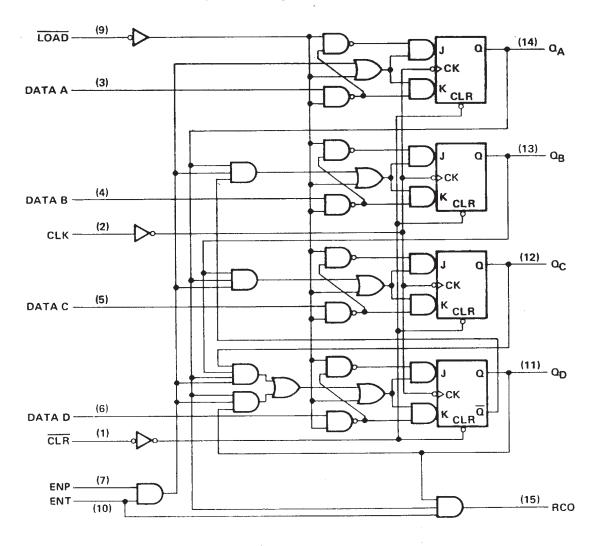






SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

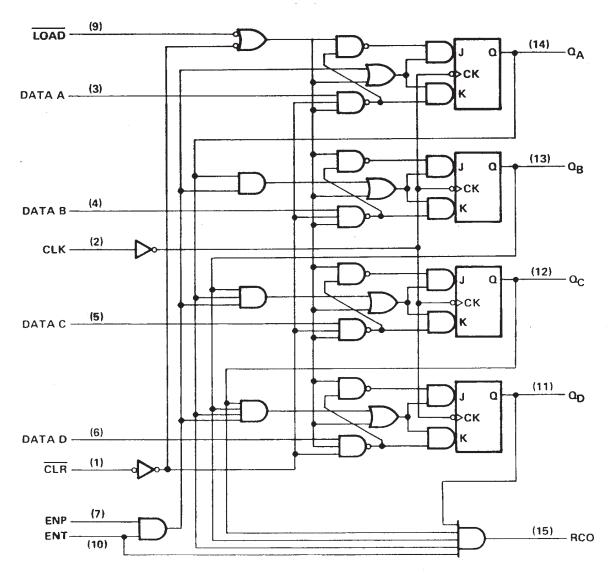
SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.





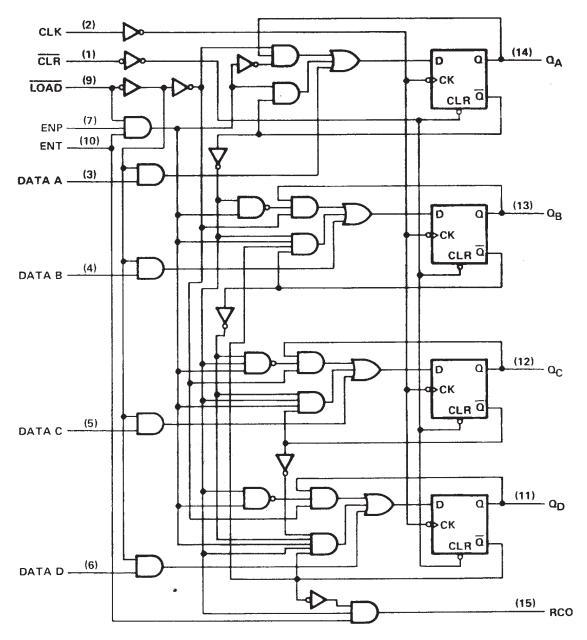
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54LS160A, SN74LS160A SYNCHRONOUS DECADE COUNTERS

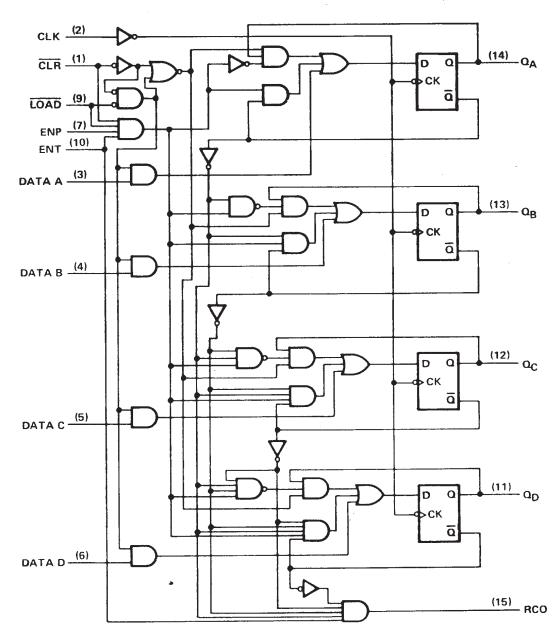
SN54LS162A, SN74LS162A synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163A, SN74LS163A binary counters at right.





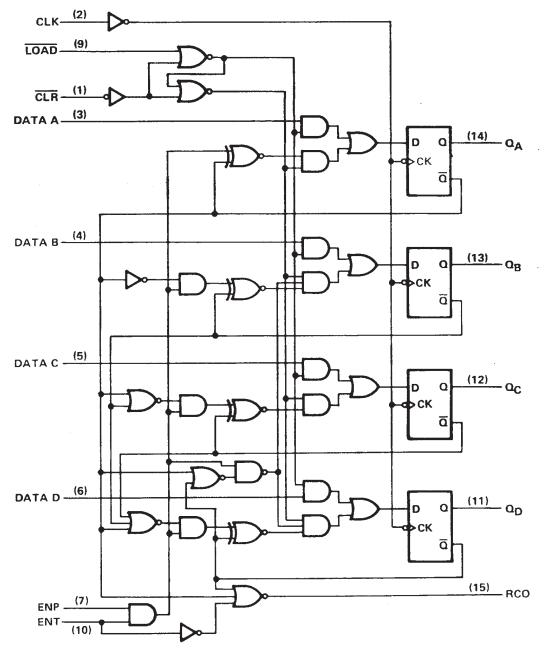
SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



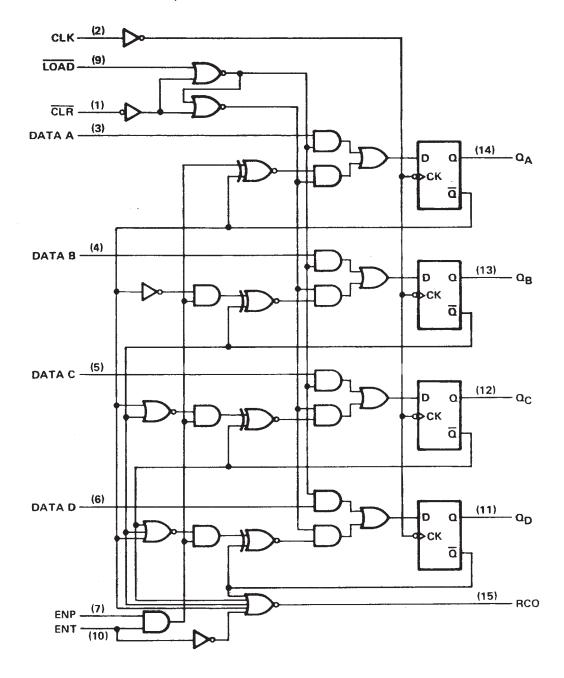


SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTER





SN54S163, SN74S163 SYNCHRONOUS DECADE COUNTER



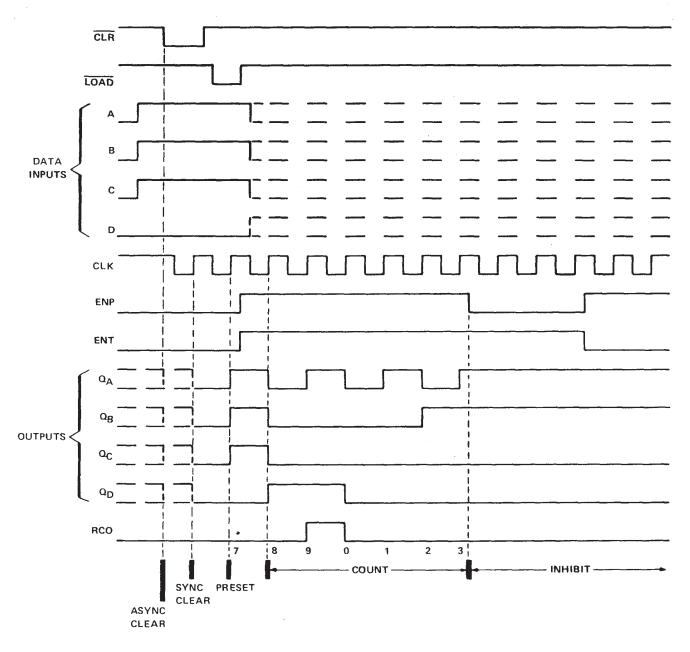
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'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

- 1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A, and 'S162 are synchronous)
- 2. Preset to BCD seven
- 3. Count to eight, nine, zero, one, two, and three
- 4. Inhibit



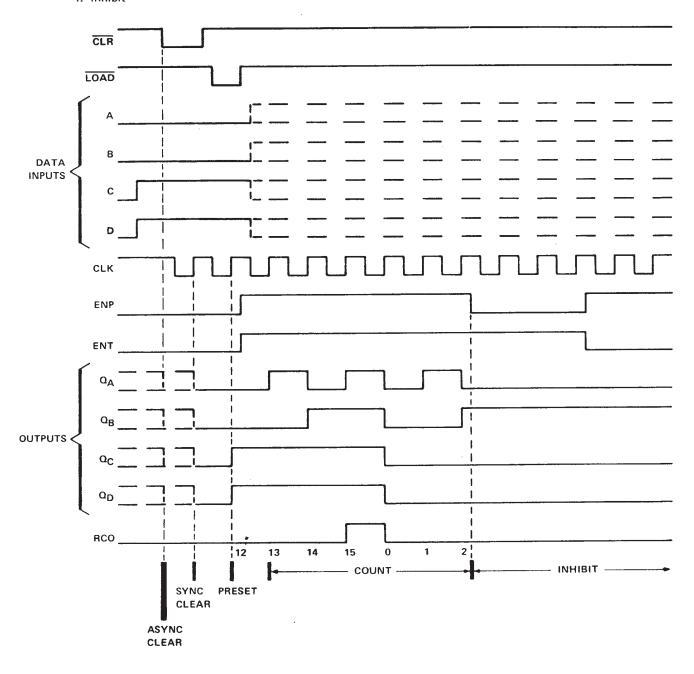


'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

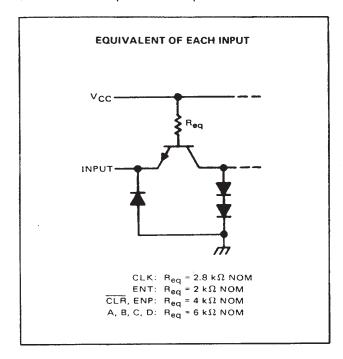
typical clear, preset, count, and inhibit sequences

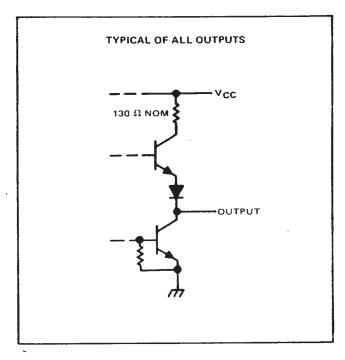
Illustrated below is the following sequence:

- 1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
- 2. Preset to binary twelve
- 3. Count to thirteen, fourteen fifteen, zero, one, and two
- 4. Inhibit



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55° C to 125° C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN541	60, SN5	4161	SN741	60, SN	74161	
		SN541	62, SN5	4163	SN741	62, SN	74163	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-	-800			-800	μΑ
Low-level output current, IOL				16			16	mA
Clock frequency, f _{clock}		0		25	0		25	MHz
Width of clock pulse, tw(clock)		25			25			ns
Width of clear pulse, tw(clear)		20			20			ns
	Data inputs A, B, C, D	20			20			
5. 1.0	ENP	20			20		,	ns
Setup time, t _{su} (see Figures 1 and 2)	LOAD	25			25] ""
	CLRT	20			20			
Hold time at any input, th		0	_		0			ns
Operating free-air temperature, TA		-55		125	0		70	¹c_

[†]This applies only for '162 and '163, which have synchronous clear inputs.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PAR	AMETER	TEST CO	NDITIONS†	1	160, SN 162, SN		1	160, SN 162, SN		UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	1
VIH	High-level input	voltage			2			2			V
VIL	Low-level input	voltage					0.8			0.8	٧
VIK	Input clamp volt	tage	V _{CC} = MIN,	I _I =12 mA			-1.5			-1.5	V
Vон	High-level outpu	t voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{1H} = 2 V, I _{OH} = -800 μA	2.4	3.4		2.4	3.4	,	v
VOL	Low-level outpu	t voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	***		0.2	0.4		0.2	0.4	V
11	Input current at	maximum input voltage	V _{CC} = MAX,	V _I = 5.5 V			1			1	mA
	High-level	CLK or ENT					80			80	
ΉΗ	input current	Other inputs	VCC = MAX,	V ₁ = 2.4 V			40			40	μΑ
	Low-level	CLK or ENT					-3.2			-3.2	
IJĽ	input current	Other inputs	V _{CC} = MAX,	V ₁ = 0.4 V			-1.6			-1.6	mA
los	Short-circuit out	put current§	V _{CC} = MAX		-20	-	-57	-18		-57	mA
ССН	Supply current,	all outputs high	V _{CC} = MAX,	See Note 3		59	85		59	94	mA
ICCL	Supply current,	all outputs low	V _{CC} = MAX,	See Note 4		63	91		63	101	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. ICCH is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I CCL is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
^t PLH	CLK		7		23	35	ns
tPHL	CLK	RCO			23	35] ''5
tpLH	CLK	Апу	$C_L = 15 pF$,		13	20	ns
^t PHL	(LOAD input high)	a	$R_L = 400 \Omega$		15	23	1 "
tPLH	CLK	Any	See Figures 1 and 2		17	25	ns
tPHL	(LOAD input low)	Q	and Note 5		19	29] '''
tPLH .					11	16	-
^t PHL	ENT	RCO			11	16	ns
tphL	CLR	Any Q	7		26	38	ns

[¶]f_{max} = Maximum clock frequency

NOTE 5: Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25°C.

Not more than one output should be shorted at a time.

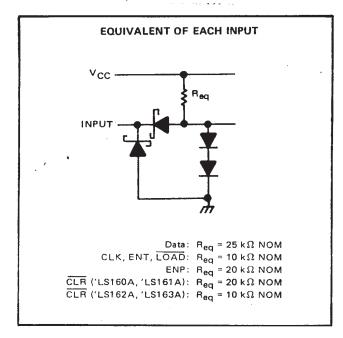
tpLH = propagation delay time, low-to-high-level output

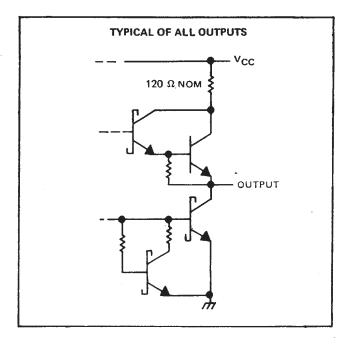
tpHL = propagation delay time, high-to-low-level output

SN54LS160 THRU SN54LS163A, SN74LS160 THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

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schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 7)			 	 	 	 7 V
Input voltage			 	 	 	 7 V
Operating free-air temperature range:	SN54LS	' Circuits	 	 	 	 55°C to 125°C
	SN74LS	' Circuits	 	 	 	 0°C to 70°C
Storage temperature range			 	 	 	 65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54L	S'	;	SN74LS	•	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
10н	High-level output current				- 400			- 400	μА
lor	Low-level output current				4			8	mΑ
fclock	Clock frequency		0		25	0		25	MHz
tw(clock)	Width of clock pulse		25			25			ns
tw(clear)	Width of clear pulse		20			20			ns
		Data inputs A, B, C, D	20			20			
		ENP or ENT	20			20			
	Control (see Single 1 and 2)	LOAD	20			20			
t _{su}	Setup time, (see Figures 1 and 2)	LOAD inactive state	20			20			ns
		CLR [†]	20			20			
		CLR inactive state	25			25			
th	Hold time at any input		3			3			ns
TA	Operating free-air temperature		55		125	0		70	°C

 $[\]uparrow$ This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

						SN54LS	•		SN74LS	ŕ	
	PARA	AMETER	TEST CON	DITIONS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input v	oltage			2			2			V
VIL	Low-level input vo	oltage					0.7			0.8	٧
VIK	Input clamp volta	ge	VCC = MIN,	VCC = MIN, II = -18 mA			-1.5			-1.5	V
	High-level output	voltage		V _{IH} = 2 V, I _{OH} = -400 μA	2.5	3.4		2.7	3.4		٧
Voi	Low-level output	voltage	V _{CC} = MIN, V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	v
·OL			VIL = VIL max	10L = 8 mA					0.35	0.5	
.,	1	Data or ENP					0.1			0.1	
	Input current	LOAD, CLK, or ENT		V 7.V			0.2			0.2	mA
Ч	at maximum	CLR ('LS160A, 'LS161A)	V _{CC} = MAX,	V = / V			0.1			0.1] ""
	input voltage	CLR ('LS162A, 'LS163A)					0.2			0.2	
		Data or ENP					20			20	
	High-level	LOAD, CLK, or ENT	.,	V . 0.7.V			40			40]
ΉΗ	input current	CLR ('LS160A, 'LS161A)	V _{CC} = MAX,	V ₁ = 2.7 V			20			20	μА
		CLR ('LS162A, 'LS163A)					40			40] .
		Data or ENP					-0.4			-0.4	
	Low-level	LOAD, CLK, or ENT	1				-0.8			-0.8	
ΊL	input current	CLR ('LS160A, 'LS161A)	V _{CC} = MAX,	V ₁ = 0.4 V			-0.4			-0.4	mA
		CLR ('LS162A, 'LS163A)					-0.8			-0.8	
los			V _{CC} = MAX		-20		-100	-20		-100	mA
Іссн	Supply current, al	Il outputs high	V _{CC} = MAX,	See Note 3		18	31		18	31	mA
ICCL	CCL Supply current, all outputs low		V _{CC} = MAX,	See Note 4		19	32		19	32	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{ C}$

PARAMETER¶.	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
^t PLH	01.14	RCO			20	35	ns
tPHL	CLK	RCO	0 15 -5		18	35	
t _{PLH}	CLK	Any	$C_L = 15 pF$,		13	24	ns
tPHL	(LOAD input high)	Q	$R_L = 2 k\Omega$		18	27	110
tPLH	CLK	Any	See figures		13	24	ns
tPHL	(LOAD input low)	Q	1 and 2 and		18	27	
tPLH		200	Note 8		9	14	ns
tPHL	ENT	RCO			9	14	""
^t PHL	CLR	Any Q			20	28	ns

[¶]f_{max} = Maximum clock frequency

NOTE 8: Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.



 $[\]ddagger$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

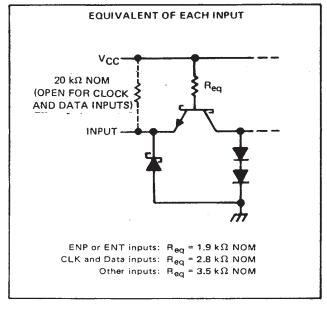
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

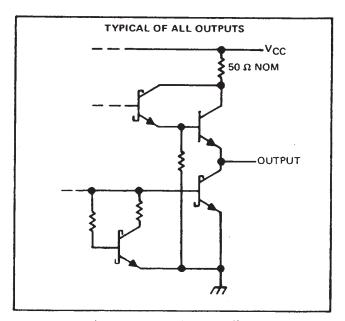
^{4.} ICCL is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

 t_{PLH} = propagation delay time, low-to-high-level output.

tpHL = propagation delay time, high-to-low-level output.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10)	55°C to 125°C
SN74S162, SN74S163	
Storage temperature range	-65°C to 150°C

recommended operating conditions

A Annual Control of the Control of t			SN54S	162, SN	54S163	SN 74S	162, SN7	74S163	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	GNII
Supply voltage, VCC			4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH					1			1	mA
Low-level output current, IQL					20			20	mA
Clock frequency, f _{clock}			0		40	0		40	MHz
Width of clock pulse, tw(clock) (high	or low)		10			10			ns
Width of clear pulse, tw(clear)			10			10			ns
		Data inputs, A, B, C, D	4			4			
		ENP or ENT	12			12]
		LOAD	14			14			ns
Setup time, t _{su} (see Figure 4)		CLR	14			14] '''
		LOAD inactive-state	12			12			
	•	CLR inactive-state	12			12			
Release time, t _{release} (see Figure 4)		ENP or ENT			4			4	ns
		Data inputs A, B, C, D	3			3			
Hold time, th (see Figure 4)		LOAD	0			0			ns
		CLR	0			0			
Operating free-air temperature, TA (s	ee Note 1	0)	55		125	0		70	С

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

- 2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the count enable inputs P and T
- 10. An SN54S162 or SN54S163 in the W package operating at free air temperatures above 91. C requires a heal sick that provides a thermal resistance from case to free-air, R $_{ heta CA}$, of not more than 26° C/W.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMET	ER	TEST CONDITIONS†			N54S16		1 -	i2 i3	UNIT	
				MIN	TYP‡	MAX	MIN	TYP‡	MAX		
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.8			8.0	V
VIF	Input clamp voltage		V _{CC} = MIN,	I _I = -18 mA			-1.2			-1.2	V
VОН	High-level output voltage		V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		v
VOL	Low-level output voltage		V _{CC} = MIN, V _{IL} = 0.8 V,	V _{1H} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
l _l	Input current at maximum	n input voltage	V _{CC} = MAX,	V ₁ = 5.5 V			1			1	mA
	The transfer of the same of th	CLK and data inputs	MAY	V - 27V			50			50	_
11H	High-level input current	Other inputs	V _{CC} = MAX,	V 1 - 2.7 V	-10		-200	-10		-200	μA
		ENT	****	0.5.1			-4			4	
IIL.	Low-level input current	Other inputs	V _{CC} = MAX,	V1 = 0.5 V			2			- 2	mA
los	Short-circuit output curre	nt [§]	V _{CC} - MAX		-40		-100	40		100	mA
1 _{CC}	Supply current		V _{CC} = MAX		1	95	160		95	160	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax				40	70		MHz
tPLH	01.14	200			14	25	ns
₹PHL	CLK	RCO	C_L 15 pF, R_L = 280 Ω , See Figures 1, 3, and 4		17	25	
tpLH	CLK	Any Q			8	15	ns
†PHL	CLN	Ally G			10	15	
tPLH -		200	1		10	15	ns
tPHL	ENT	RCO			10	15	

[¶]f_{max} ≡maximum cłock frequency

[‡]All typical values are at V_{CC} 5 V, T_A 25 C.

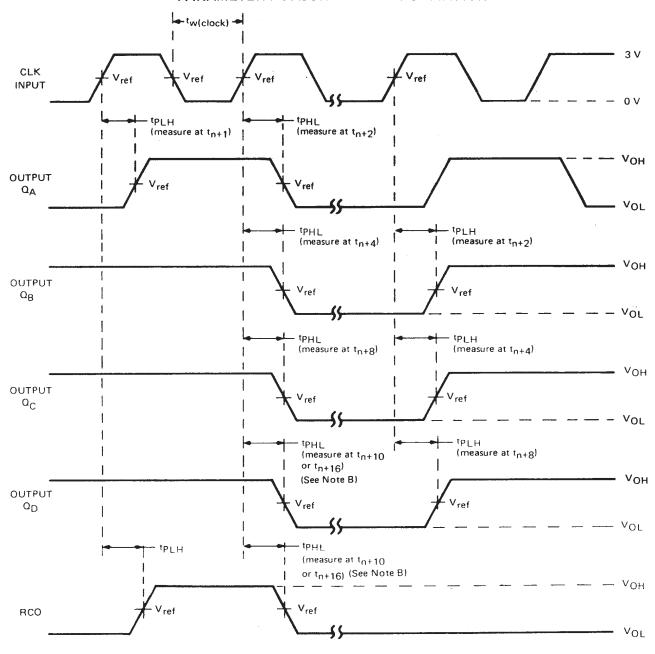
[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

 $t_{PLH} \equiv propagation$ delay time, low to high level output

tpHL = propagation delay time, high-to low level output

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PARAMETER MEASUREMENT INFORMATION

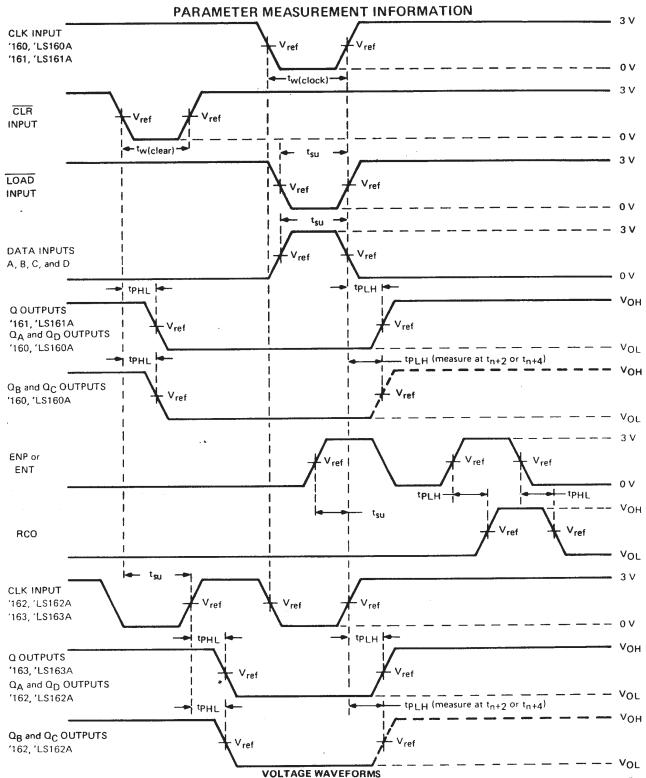


VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{out} \approx 50 Ω ; for '160 thru '163, t_r \leq 10 ns, t_f \leq 10 ns; for 'LS160A thru 'LS163A t_r \leq 15 ns, t_f \leq 6 ns; and for 'S162, 'S163, t_r \leq 2.5 ns. Vary PRR to measure f_{max}.
 - B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.
 - C. For '160 thru '163, 'S162, and 'S163, V_{ref} = 1.5 V; for 'LS160A thru 'LS163A, V_{ref} = 1.3 V.

FIGURE 1-SWITCHING TIMES





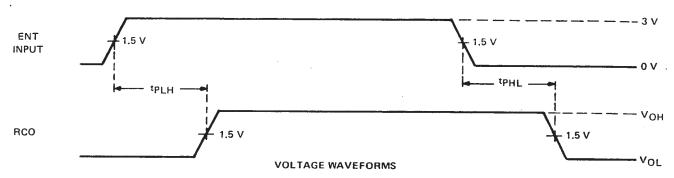
NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx$ 50 Ω ; for '160 thru '163, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns; and for 'LS160A thru 'LS163A, $t_r \leq$ 15 ns, $t_f \leq$ 6 ns.

- B. Enable P and enable T setup times are measured at t_{n+0}.
- C. For '160 thru '163, $V_{ref} = 1.5 \text{ V}$; for 'LS160A thru 'LS163A, $V_{ref} = 1.3 \text{ V}$.

FIGURE 2-SWITCHING TIMES

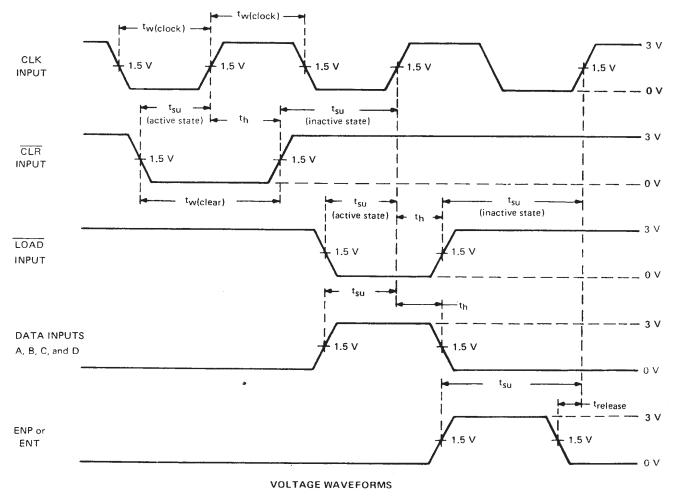


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_{\rm r} \lesssim$ 2.5 ns, $t_{\rm f} \approx$ 2.5 ns, PRR = 1 MHz, duty cycle \lesssim 50%, $Z_{\rm out} \approx$ 50 Ω .
 - B. tp_H and tpH_ from enable T input to carry output assume that the counter is at the maximum count (QA and QD high for 'S162, all Q outputs high for 'S163).

FIGURE 3-PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r = 2.5$ ns, $t_f = 2.5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{\rm out} \approx 50$ Ω_{\odot}

FIGURE 4-PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

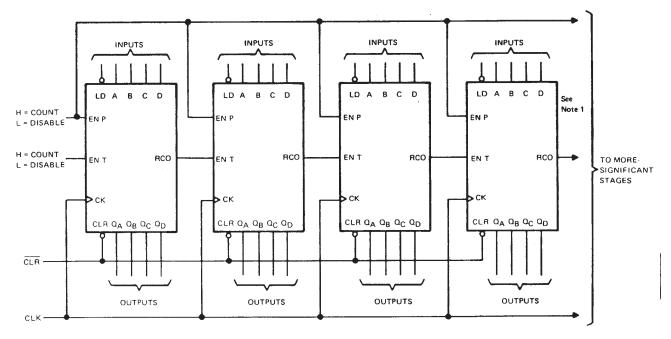


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TYPICAL APPLICATION DATA

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A, or 'S163 will count in binary. When additional stages are added the fMAX decreases in Figure 1, but remains unchanged in Figure 2.

N-BIT SYNCHRONOUS COUNTERS

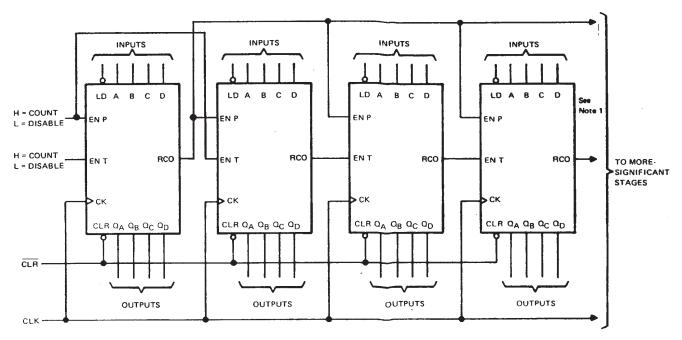


 $f_{MAX} = 1/(CLK \text{ to RCO tpLH}) + (ENT \text{ to RCO t pLH}) (N-2) + (ENT t_{SU})$

FIGURE 1

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TYPICAL APPLICATION DATA



fMAX = 1/(CLK to RCO tPLH) + (ENP tsu)

FIGURE 2





TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS161ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS163ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS163ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS161ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS161ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LS163ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS163ANSR	SO	NS	16	2000	346.0	346.0	33.0

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