LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs

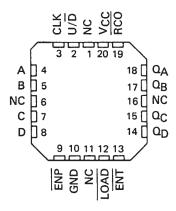
TVDE	TYPICAL I CLOCK FR		TYPICAL		
ТҮРЕ	COUNTING	COUNTING COUNTING			
	UP	DOWN	DISSIPATION		
'LS668, 'LS669	32 MHz	32 MHz	100 mW		

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. SN54LS668, SN54LS669 . . . J OR W PACKAGE SN74LS668, SN74LS669 . . . D OR N PACKAGE (TOP VIEW)

(TOP VIEVV)
U/D 1 16 V <u>CC</u> CLK 2 15 RCO A 3 14 QA B 4 13 QB C 5 12 QC D 6 11 QD ENP 7 10 ENT GND 8 9 LOAD

SN54LS668, SN54LS669 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (\overline{P} and \overline{T}) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input \overline{T} is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse when the count is maximum counting up or zero counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable \overline{P} or \overline{T} inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable P, enable T, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

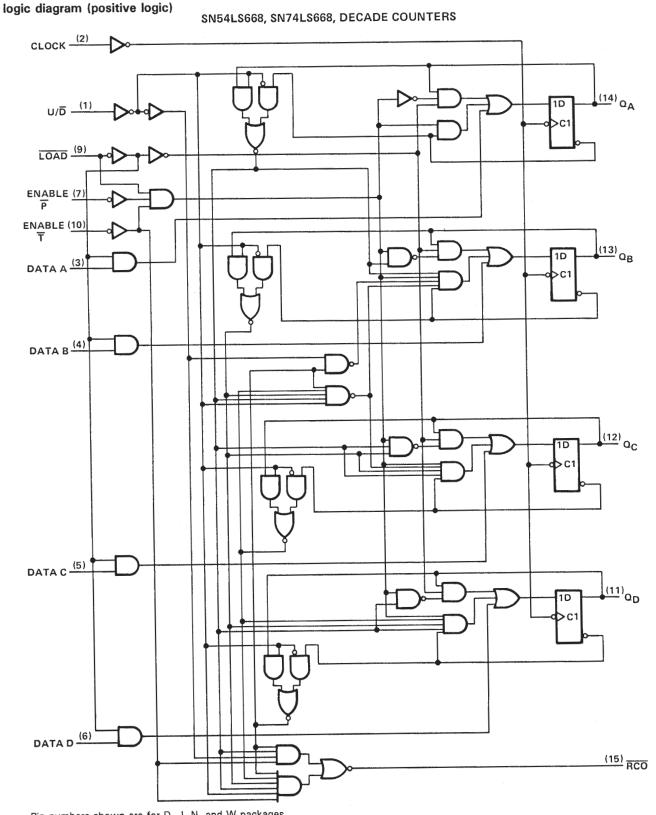
The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL}, and all buffered outputs.



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SN54LS668, SN74LS668 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

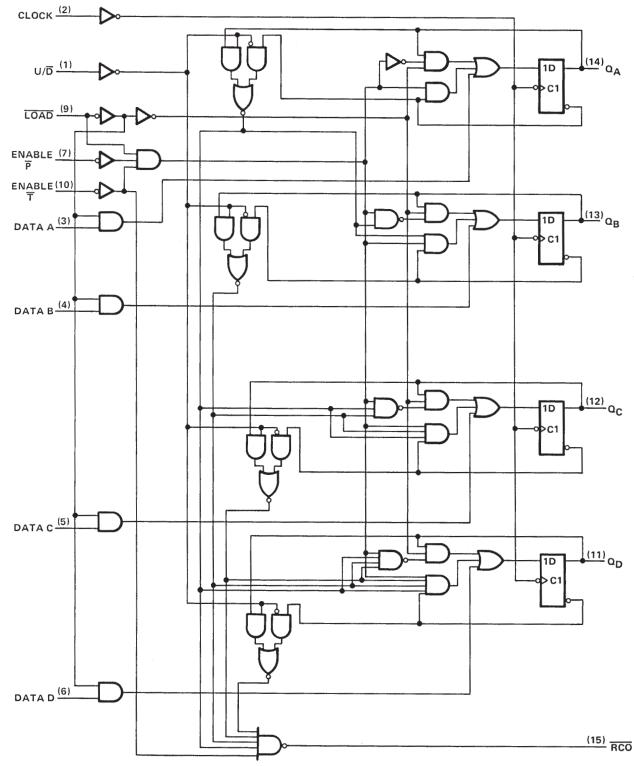
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SN54LS669, SN74LS669 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

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SN54LS669, SN74LS669, BINARY COUNTERS

logic diagram (positive logic) (continued)



SN54LS668, SN74LS668 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

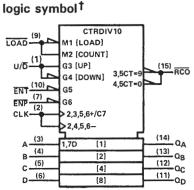
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'LS668 DECADE COUNTERS

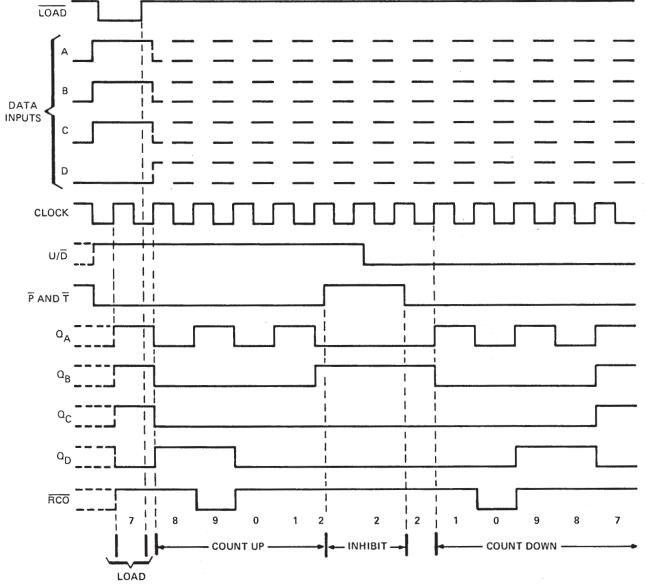
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

- 1. Load (preset) to BCD seven
- 2. Count up to eight, nine (maximum), zero, one, and two
- 3. Inhibit
- 4. Count down to one, zero (minimum), nine, eight, and seven



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.





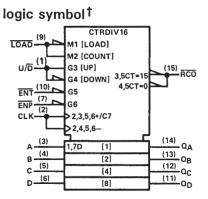
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'LS669 BINARY COUNTERS

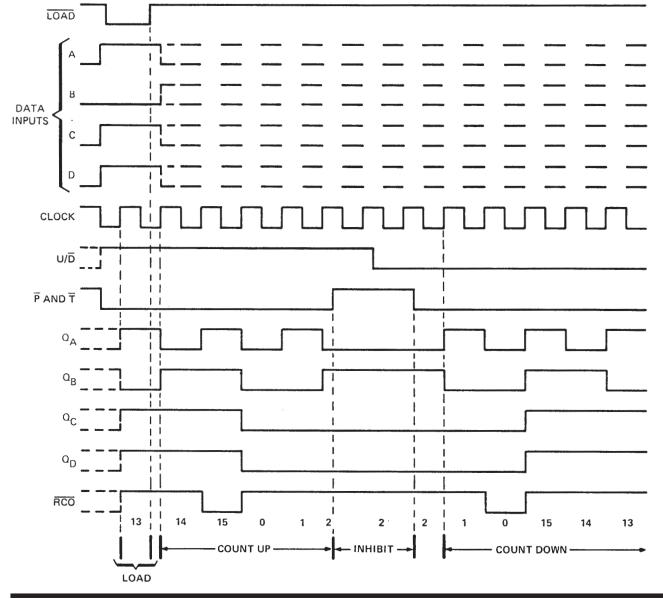
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

- 1. Load (preset) to binary thirteen
- 2. Count up to fourteen, fifteen (maximum), zero, one, and two
- 3. Inhibit
- 4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen

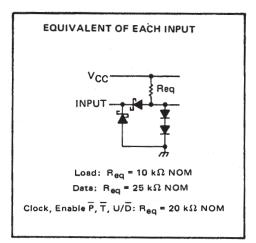


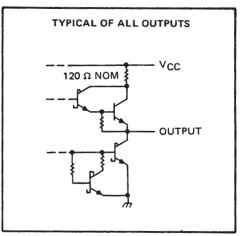
[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.



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schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	· • • • • • • • • • • • •	 	
Input voltage			
Operating free-air temperature range:	SN54LS668, SN54LS669 SN74LS668, SN74LS669		
Storage temperature range	•		

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			N54LS6 N54LS6				UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH		1		-400			-400	μA
Low-level output current, IOL				4			8	mA
Clock frequency, fclock				25	0		25	MHz
Width of clock pulse, tw(clock) (high or low)	(see Figure 1)	20			20			ns
idth of clock pulse, t _{w(clock)} (high or low) (etup time, t _{su} (see Figure 1)	Data inputs A, B, C, D	25			25			
	ENP or ENT	40			40			
	LOAD	30			30			ns
	U/D	45			45	NOM MAX 5 5.25 -400 8 25		
Hold time at any input with respect to clock					0			ns
Operating free-air temperature, T _A		-55		125	0		70	°C



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PARAMETER		TEST CONDITIONS [†]		SN54LS668 SN54LS669				68 69	UNIT			
				MIN	түр‡	MAX	MIN	түр‡	MAX]		
VIH	High-level input voltage				2			2			V	
VIL	Low-level input voltage						0.7			0.8	V	
VIK	Input clamp voltage		V _{CC} = MIN,	Ij = -18 mA			-1.5			-1.5	V	
VOH High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} max,		2.5	3.4		2.7	3.4		v		
Voi L	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	v	
			VIL = VIL max	10L = 8 mA					0.35	0.5		
	Input current	A, B, C, D, P, U/D					0.1	ł		0.1		
4	at maximum	Clock, T	V _{CC} = MAX,	VI = 7 V			0.1			0,1	mA	
	input voltage	LOAD					0.2			0.2	1	
	High-level	A, B, C, D, P, U/D					20			20		
ŧн	input current	Clock, T	V _{CC} = MAX,	V1 = 2.7 V			20			20	μA	
		LOAD					40			40	1	
	Low-level	A, B, C, D, P, U/D					-0.4			-0.4		
hL -	input current	Clock, T	V _{CC} = MAX,	V _{CC} = MAX,	Vi = 0.4 V			0.4			-0.4	mA
	LOAD				-0.8			-0.8	1			
los	Short-circuit output cur	rent§	V _{CC} = MAX		-20		-100	-20		-100	mA	
lcc	Supply current		V _{CC} = MAX,	See Note 2		20	34	1	20	34	mA	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: 1_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	ТҮР	МАХ	UNIT
fmax				25	32	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	MHz
^t PLH	CLK	RCO			26	40	
^t PHL	OLK	neo	$C_L = 15 pF$,		40	60	ns
^t PLH	CLK	Any				18	27
^t PHL	ULK	٥	$R_L = 2 k\Omega$,		18	27	ns
^t PLH	ENT	RCO	See Figures 2 and 3		11	17	
^t PHL	ENT		29	45	ns		
tPLH#			RCO		22`	35	†
tPHL#	Ū/Ū	HCU			26	40	ns

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

¶ f_{max} = Maximum clock frequency.

tpLH = propagation delay time, low-to-high-level output.

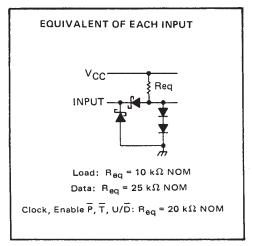
tpHL = propagation delay time, high-to-low-level output.

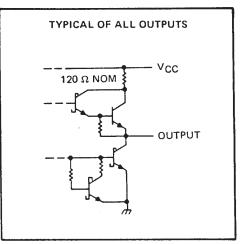
* Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.



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schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage			~
Operating free-air temperature range:	SN54LS668, SN54LS669	69	ъс
	SN74LS668, SN74LS669	69 0°C to 70	°С
Storage temperature range			°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			N54LS6 N54LS6			74LS66		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-400			-400	μA
Low-level output current, IOL				4			8	mA
Clock frequency, f _{clock}		0		25	0		25	MHz
Width of clock pulse, tw(clock) (high or low	w) (see Figure 1)	20			20			ns
idth of clock pulse, t _{w(clock)} (high or low)	Data inputs A, B, C, D	25			25			
Sotup time to Jaco Eigure 1)	ENP or ENT	40			40			ns
Setup time, t _{su} (see Figure 1)	LOAD	30			30	N74LS669 NOM MAX 5 5 5.25 400 8 0 25 0 5 0 5 0 5 0 0 5 0 0 5 0 0 5 0 0 0 0 0 0 0 0 0 0 0 0 0] "5	
llock frequency, f _{clock} /idth of clock pulse, t _{w(clock)} (high or low) (see Figure Setup time, t _{su} (see Figure 1)	U/D	45		1	45			
Hold time at any input with respect to clo	ck, th (see Figure 1)	0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C



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PARAMETER		TEST CONDITIONS [†]		SN54LS668 SN54LS669				68 69	UNIT		
					MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
νін	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage		V _{CC} = MIN,	l ₁ =18 mA			-1.5			-1.5	V
vон	OH High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} max,		, 2. 5	3.4		2.7	3.4		v
	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	v
VOL			VIL = VIL max	10L = 8 mA					0.35	0.5	
	Input current	A, B, C, D, P, U/D					0.1			0.1	
1	at maximum	Clock, T	V _{CC} = MAX, V _I = 7 V	V ₁ = 7 V			0.1			0.1	mΑ
	input voltage	LOAD					0.2			0.2]
		A, B, C, D, P, U/D					20			20	
ιн	High-level	Clock, T	V _{CC} = MAX,	VI = 2.7 V			20			20	μA
	input current	LOAD					40			40]
		A, B, C, D, P, U/D					-0.4			-0.4	
1L	Low-level	Clock, T	V _{CC} = MAX,	V _I = 0.4 V			-0.4			-0.4	mA
	input current	LOAD					-0.8			-0.8]
los	Short-circuit output cur	rent§	V _{CC} = MAX		-20		-100	-20		-100	mA
ICC	Supply current		V _{CC} = MAX,	See Note 2		20	34		20	34	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

 ${
m \$}$ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	МАХ	UNIT
f _{max}				25	32		MHz
^t PLH	CLK	RCO	C _L = 15 pF,	26	40	ns	
^t PHL	ULN	1100			40	60] "
^t PLH	OLK.	Any		R _L = 2 kΩ,		18	27
^t PHL	CLK	Q	See Figures 2 and 3		18	27] "`
^t PLH	ENT	RCO			11	17	ns
^t PHL	ENT	1100			29	45] '''
tPLH#		800			22	35	ns
tPHL#	U/D	RCO			26	40] ^{IIS}

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

1 fmax = Maximum clock frequency.

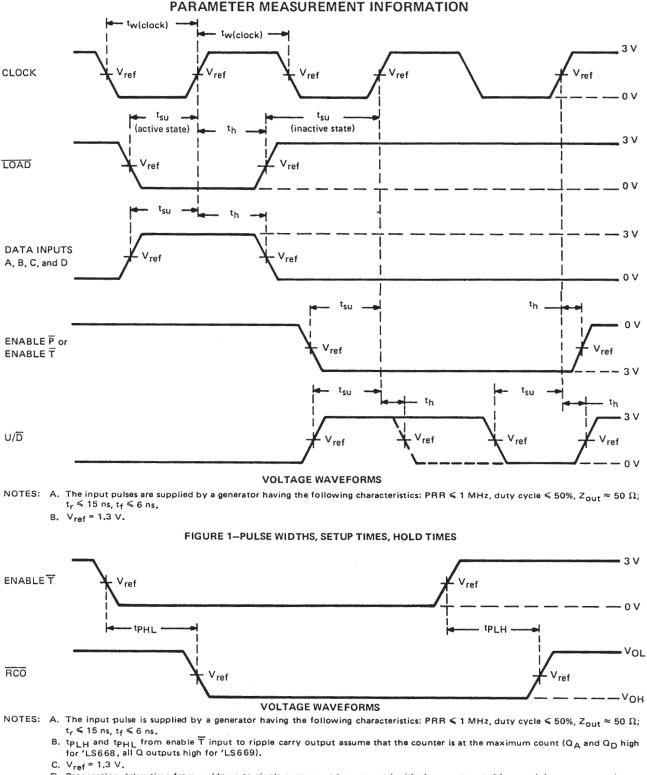
tpHL = propagation delay time, high-to-low-level output.

Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.



tpLH = propagation delay time, low-to-high-level output.

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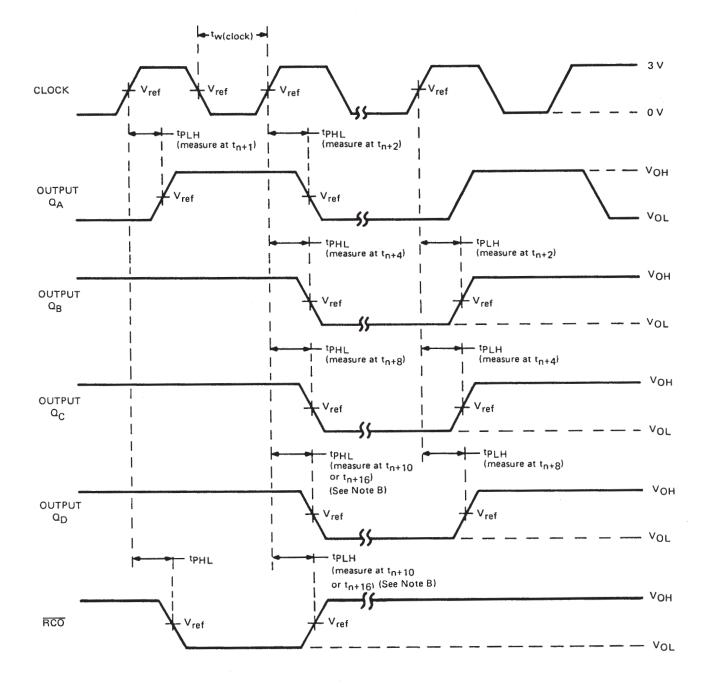


D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

FIGURE 2-PROPAGATION DELAY TIMES TO CARRY OUTPUT



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PARAMETER MEASUREMENT INFORMATION

UP-COUNT VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{out} \approx 50 Ω , t_r \leq 15 ns, t_f \leq 6 ns. Vary PRR to measure f_{max}.
 - B. Outputs Q_D and carry are tested at t_{n+10} for the 'LS668, and at t_{n+16} for the 'LS669, where t_n is the bit-time when all outputs are low.
 - C. $V_{ref} = 1.3 V$.

FIGURE 3-PROPAGATION DELAY TIMES FROM CLOCK



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