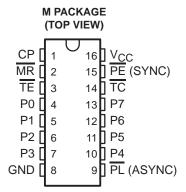
- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- Synchronous or Asynchronous Preset
- Cascadable in Synchronous or Ripple Mode
- Fanout (Over Temperature Range)
 - Standard Outputs ... 10 LSTTL Loads
 - Bus Driver Outputs ... 15 LSTTL Loads
- † Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- V_{CC} Voltage = 2 V to 6 V
- High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V



description/ordering information

The CD74HC40103 is manufactured with high-speed silicon-gate technology and consists of an 8-stage synchronous down counter with a single output, which is active when the internal count is zero. The device contains a single 8-bit binary counter. Each device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count (TC) output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the clock (CP) output. Counting is inhibited when the terminal enable ($\overline{\text{TE}}$) input is high. $\overline{\text{TC}}$ goes low when the count reaches zero, if $\overline{\text{TE}}$ is low, and remains low for one full clock period.

When the synchronous preset enable (\overline{PE}) input is low, data at the P0–P7 inputs are clocked into the counter on the next positive clock transition, regardless of the state of \overline{TE} . When the asynchronous preset enable (\overline{PL}) input is low, data at the P0–P7 inputs asynchronously are forced into the counter, regardless of the state of the \overline{PE} , \overline{TE} , or CP inputs. Inputs P0–P7 represent a single 8-bit binary word for the CD74HC40103. When the master reset (\overline{MR}) input is low, the counter asynchronously is cleared to its maximum count of 255₁₀, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

ORDERING INFORMATION

TA	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - M	Tape and reel	CD74HC40103QM96EP	HC40103QEP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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CD74HC40103-EP HIGH-SPEED CMOS LOGIC 8-STAGE SYNCHRONOUS DOWN COUNTER

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description/ordering information (continued)

If all control inputs except $\overline{\text{TE}}$ are high at the time of zero count, the counters jump to the maximum count, giving a counting sequence of 100_{16} or 256_{10} clock pulses long.

The CD74HC40103 may be cascaded using the $\overline{\text{TE}}$ input and the $\overline{\text{TC}}$ output in either synchronous or ripple mode. These circuits have the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits and can drive up to ten LSTTL loads.

FUNCTION TABLE†

	CONTRO	L INPUTS		DDEOET MODE	ACTION
MR	PL	PE	TE	PRESET MODE	ACTION
Н	Н	Н	Н		Inhibit counter
Н	Н	Н	L	Synchronous	Count down
Н	Н	L	Х		Preset on next positive clock transition
Н	L	Х	Х	Agunghrangua	Preset asynchronously
L	Х	Х	Х	Asynchronous	Clear to maximum count

†See Figure 2 for timing diagram.

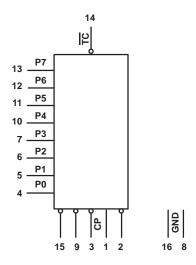
NOTE: H = high voltage level, L = low voltage level, X = don't care

Clock connected to clock input

Synchronous operation: changes occur on negative-to-positive clock transitions.

Load inputs: MSB = P7, LSB = P0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$)	±20 mA
Source or sink current per output pin, $I_O (V_O > -0.5 \text{ V or } V_O < V_{CC} + 0.5 \text{ V})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ _{JA} (see Note 2)	73°C/W
Maximum junction temperature, T _J	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch $(1,59 \pm 0,79$ mm) from case for 10 s max	300°C
Storage temperature range, T _{stq} –65	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	6	V
		V _{CC} = 2 V	1.5		
٧ıн	High-level input voltage	V _{CC} = 4.5 V	3.15		V
		V _{CC} = 6 V	4.2		
		V _{CC} = 2 V		0.5	
۷ _{IL}	Low-level input voltage	V _{CC} = 4.5 V		1.35	V
		V _C C = 6 V		1.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 2 V	0	1000	
t _t	Input transition (rise and fall) time	V _{CC} = 4.5 V	0	500	ns
		V _C C = 6 V	0	400	
TA	Operating free-air temperature		-40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



NOTES: 1. All voltages referenced to GND unless otherwise specified.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

CD74HC40103-EP **HIGH-SPEED CMOS LOGIC** 8-STAGE SYNCHRONOUS DOWN COUNTER SCLS548 - DECEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEOT 04	TEST CONDITIONS			T _A = 25°C			MAY	
PARAMETER	TEST CO				MIN	MAX	MIN	MAX	UNIT
			-0.02	2 V	1.9		1.9		
		CMOS loads	-0.02	4.5 V	4.4		4.4		
Voн	$V_I = V_{IH}$ or V_{IL}		-0.02	6 V	5.9		5.9		V
		TTI In a la	-4	4.5 V	3.98		3.7		
		TTL loads	-5.2	6 V	5.48		5.2		
			0.02	2 V		0.1		0.1	
		CMOS loads	0.02	4.5 V		0.1		0.1	
VOL	$V_I = V_{IH}$ or V_{IL}		0.02	6 V		0.1		0.1	V
		TTI In a la	4	4.5 V		0.26		0.4	
		TTL loads	5.2	6 V		0.26		0.4	
lį	$V_I = V_{CC}$ or GND	V _I = V _{CC} or GND		6 V		±0.1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND		0	6 V		8		160	μΑ
C _{IN}	C _L = 50 pF					10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				T _A =	25°C			
		PARAMETER	VCC	MIN	MAX	MIN	MAX	UNIT
			2 V	165		250		
		СР	4.5 V	33		50		
			6 V	28		43		
			2 V	125		190		
t _w	Pulse duration	PL	4.5 V	25		38		ns
			6 V	21		32		
			2 V	125		190		
		MR	4.5 V	25		38		
			6 V	21		32		
		•	2 V	3		2		
fmax	f _{max} CP frequency (see No	ote 4)	4.5 V	15		10		MHz
			6 V	18		12		
			2 V	100		150		
		P to CP	4.5 V	20		30		
			6 V	17		26		
			2 V	75		110		
		PE to CP	4.5 V	15		22		
			6 V	13		19		
t _{su}	Setup time		2 V	150		225		ns
		TE to CP	4.5 V	30		45		
			6 V	26		38		
			2 V	50		75		
		To CP, MR inactive	4.5 V	10		15		
			6 V	9		13		
			2 V	5		5		
		P to CP	4.5 V	5		5		
			6 V	5		5		
			2 V	0		0		
th	Hold time	TE to CP	4.5 V	0		0		ns
			6 V	0		0		
			2 V	2		2		
		PE to CP	4.5 V	2		2		
			6 V	2		2		

NOTE 4: Noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, count enables (PE or TE) to clock setup times, and count enables (PE or TE) to clock hold times determine maximum clock frequency. For example, with these HC devices:

$$CP f_{max} = \frac{1}{CP \text{ to } \overline{TC} \text{ prop delay } + \overline{TE} \text{ to } CP \text{ setup time } + \overline{TE} \text{ to } CP \text{ hold time}} = \frac{1}{60 + 30 + 0} \approx 11 \text{ MHz}$$



CD74HC40103-EP HIGH-SPEED CMOS LOGIC 8-STAGE SYNCHRONOUS DOWN COUNTER

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	,,	T	λ = 25°C	;			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	VCC	MIN	TYP	MAX	MIN MAX	UNIT	
		_		2 V			300	450		
		TC (asynchronous	C _L = 50 pF	4.5 V			60	90		
		preset)		6 V			51	77		
	CP	, ,	C _L = 15 pF	5 V		25				
	CP			2 V			300	450		
		TC (synchronous	$C_{L} = 50 pF$	4.5 V			60	90		
		preset)		6 V			51	77		
		, ,	C _L = 15 pF	5 V		25				
			C _L = 50 pF	2 V			200	300		
4 .	TE	TC		4.5 V			40	60]	
t _{pd}	16	10		6 V			34	51	ns	
			C _L = 15 pF	5 V		17				
	PL			2 V			275	415		
		TC	C _L = 50 pF	4.5 V			55	83]	
	PL	10		6 V			47	71		
			C _L = 15 pF	5 V		23				
				2 V			275	415		
	MR	TC	C _L = 50 pF	4.5 V			55	83		
	IVIK	10		6 V			47	71		
			C _L = 15 pF	5 V		23				
				2 V			75	110		
t _t			C _L = 50 pF	4.5 V			15	22	ns	
				6 V			13	19		
f _{max}	CP		C _L = 15 pF	5 V		25			MHz	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, input t_r , $t_f = 6 \text{ ns}$

	PARAMETER				
C _{pd}	Power dissipation capacitance (see Note 5)	25	pF		

NOTE 5: C_{pd} is used to determine the dynamic power consumption per package.

 $P_{D} = (C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_O)$

f_I = input frequency

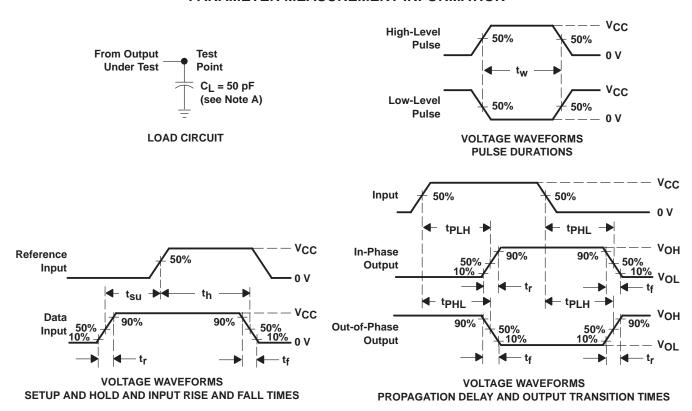
f_O = output frequency

C_L = output load capacitance

V_{CC} = supply voltage



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 6 \ ns$, $t_f = 6 \ ns$.
- C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

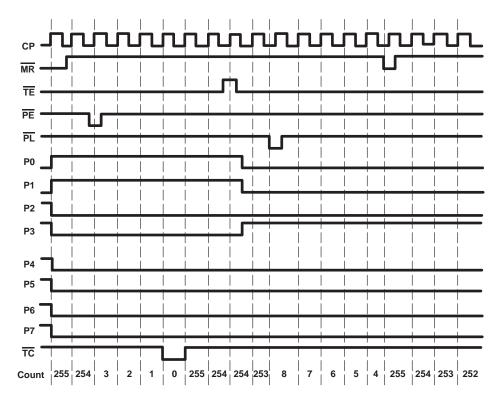


Figure 2. Timing Diagram







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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HC40103QM96EP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04702-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD74HC40103-EP:

Catalog: CD74HC40103

Automotive: CD74HC40103-Q1

• Military: CD54HC40103

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40103QM96EP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
CD74HC40103QM96EP	SOIC	D	16	2500	333.2	345.9	28.6	

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



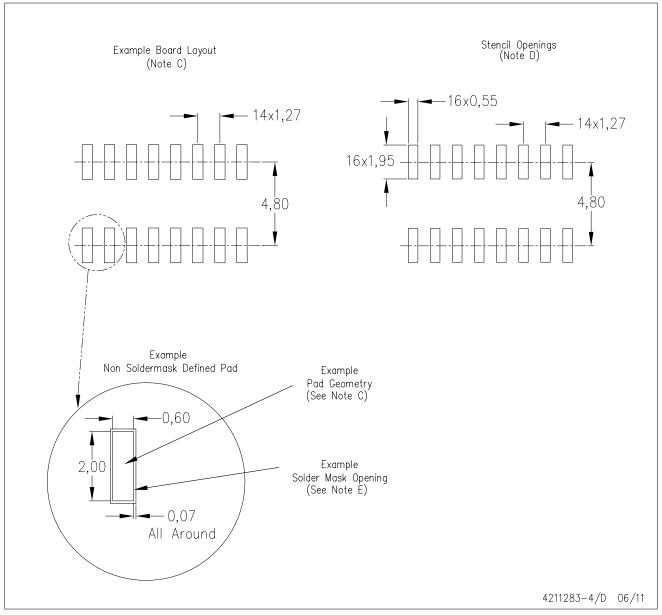
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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