SCCS016A - MAY 1994 - REVISED SEPTEMBER 2001

16 VCC

15 P₀

14 CP

13 RC

12 TC

11 PL

10 P₂

9 P3

Q OR SO PACKAGE

(TOP VIEW)

Ρı

Q₀

Q₁ [

CE I 4

U/D 5

Q₂ 6

Q₃ [7

GND 8

2

3

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22

 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- 64-mA Output Sink Current 32-mA Output Source Current

description

The CY74FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the CY74FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple-clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NAME	DESCRIPTION							
CE	Count enable input (active low)							
CP Clock pulse input (active rising edge)								
Р	Parallel data inputs							
PL	Asynchronous parallel load input (active low)							
U/D	Up/down count control input							
Q	Flip-flop outputs							
RC	Ripple clock output (active low)							
TC	Terminal count output							

PIN DESCRIPTION



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TA	PAC	CKAGE [†]	SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QSOP - Q Tape and reel SOIC - SO Tube Tape and reel	Tape and reel	6.2	CY74FCT191CTQCT	FT191-3
		Tube	6.2	CY74FCT191CTSOC	FCT191C
–40°C to 85°C		Tape and reel	6.2	CY74FCT191CTSOCT	FCTI9IC
	SOIC – SO	Tube	7.8	CY74FCT191ATSOC	FCT191A
	3010 - 30	Tape and reel	7.8	CY74FCT191ATSOCT	FCIIBIA

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

RC FUNCTION

INPU	JTS	OUTPUTS			
CE	СР	CP TC [†] RC			
L	Ţ	Н	Ъ		
Н	Х	Х	Н		
Х	Х	L	Н		

H = High logic level, L = Low logic level,

X = Don't care, $\neg _ \neg$ = Low pulse

[†]TC is generated internally.

MODE SELECT

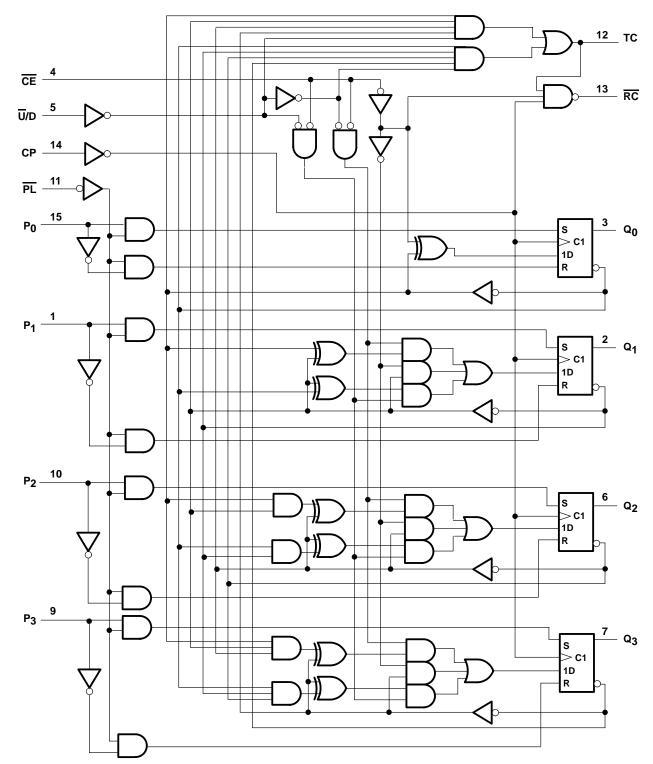
	INP	UTS	MODE						
PL	CE	Ū/D	СР	MODE					
Н	L	L	1 1	Count up					
Н	L	Н	Ŷ	Count down					
L	Х	Х	Х	Preset (asynchronous)					
Н	Н	Х	Х	No change (hold)					

H = High logic level, L = Low logic level, X = Don't care,

 \uparrow = Low-to-high clock transition



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logic diagram (positive logic)



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absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, T _A	–65°C to 135°C
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.75	5	5.25	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
ЮН	High-level output current			-32	mA
I _{OL}	Low-level output current			64	mA
Т _А	Operating free-air temperature	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



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PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.75 V,	I _{IN} = -18 mA			-0.7	-1.2	V
	V _{CC} = 4.75 V,	I _{OH} = -32 mA		2			V
VOH	V _{CC} = 4.75 V,	I _{OH} = -15 mA		2.4	3.3		v
VOL	V _{CC} = 4.75 V,	I _{OL} = 64 mA			0.3	0.55	V
VH	All inputs				0.2		V
lj	V _{CC} = 5.25 V,	$V_{IN} = V_{CC}$				5	μA
Iн	V _{CC} = 5.25 V,	V _{IN} = 2.7 V			±1	μA	
۱ _{IL}	V _{CC} = 5.25 V,	V _{IN} = 0.5 V			±1	μA	
los‡	V _{CC} = 5.25 V,	V _{OUT} = 0 V	-60	-120	-225	mA	
l _{off}	$V_{CC} = 0 V,$	V _{OUT} = 4.5 V			±1	μA	
ICC	$V_{CC} = 5.25 \text{ V}, \text{ V}_{IN} \le 0.2 \text{ V}, \text{ V}_{IN}$	$C = 5.25 \text{ V}, \text{ V}_{\text{IN}} \le 0.2 \text{ V}, \text{ V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V}$					mA
ΔICC	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f	i = 0, Outputs open			0.5	2	mA
ICCD	$\frac{V_{CC}}{MR} = 5.25 \text{ V}, \text{ One bit switchir} \\ \overline{MR} = V_{CC} = \overline{SR}, \ \overline{PL} = \overline{CE} = \overline{U}$	ng at 50% duty cycle, Preset J/D = CP = GND, $V_{IN} \le 0.2$ V	mode, Outputs open, V or $V_{IN} \ge V_{CC} - 0.2 V$		0.06	0.12	mA/ MHz
		One bit switching	$V_{IN} = V_{CC}$ or GND		0.4	0.8	mA
ı#	V _{CC} = 5.25 V, Preset mode,	at f ₁ = 5 MHz at 50% duty cycle	V_{IN} = 3.4 V or GND		0.7	1.8	mA
IC#	Outputs open, PL = $\overline{CE} = \overline{U}/\overline{D} = CP = GND$	Four bits switching	V _{IN} = V _{CC} or GND		1.3	2.6	mA
	FL = GL = 0/D = GF = GND	at f ₁ = 5 MHz at 50% duty cycle	$V_{IN} = 3.4 \text{ V or GND}$		2.3	6.6ll	mA
Ci		•	-		5	10	pF
Co					9	12	pF

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] Typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

* Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, IOS tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

[#] I_C = I_{CC} + Δ I_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

IC = Total supply current

ICC = Power-supply current with CMOS input levels

 ΔI_{CC} = Power-supply current for a TTL high input (VIN = 3.4 V)

D_H = Duty cycle for TTL inputs high

 N_T = Number of TTL inputs at D_H

 I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

 f_0 = Clock frequency for registered devices, otherwise zero

 f_1 = Input signal frequency

 N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

I Values for these conditions are examples of the I_{CC} formula.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

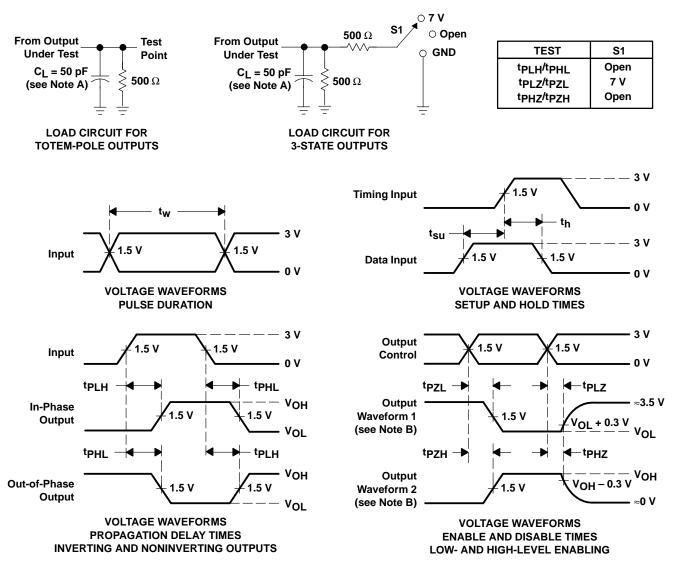
		PARAMETER		CY74FCT	191AT	CY74FCT	UNIT	
		PARAMETER		MIN	MAX	MIN	MAX	UNIT
t Dulas duration		СР	High or Low	4		4		-
t _W Pulse duration	Fuise duration	PL low		5.5		5		ns
		Data before $\overline{PL}\downarrow$	High or Low	4		3.5		
t _{su}	Setup time	CE before CP↑	Low	9		7.2		ns
		U/D before CP↑	High or Low	10		8		
		Data after PL↓	High or Low	1.5		1		
t _h	Hold time	CE after CP↑	Low	0		0		ns
		U/D after CP↑	High or Low	0		0		
t _{rec}	Recovery time	PL after CP↑		5		4.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM	то	CY74FCT	191AT	CY74FCT	191CT	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX		
^t PLH	СР	0	1.5	7.8	1.5	6.2	ns	
^t PHL	CF	Q _n	1.5	7.8	1.5	6.2	115	
^t PLH	СР	TC	1.5	11.8	1.5	9.4	ns	
^t PHL	CF	TC TC	1.5	11.8	1.5	9.4	115	
^t PLH	СР	RC	1.5	8.5	1.5	6.8	ns	
^t PHL	CF	ĸu	1.5	8.5	1.5	6.8	115	
^t PLH	CE	RC	1.5	7.2	1.5	6	ns	
^t PHL		ĸċ	1.5	7.2	1.5	6	115	
^t PLH	Ū/D	RC	1.5	13	1.5	11	ns	
^t PHL	0/8	ĸu	1.5	13	1.5	11	115	
tplh	Ū/D	TC	1.5	7.2	1.5	6.1	ns	
^t PHL	0/0	10	1.5	7.2	1.5	6.1	115	
^t PLH	Р	0	1.5	9.1	1.5	7.7		
^t PHL	Pn	Q _n	1.5	9.1	1.5	7.7	ns	
^t PLH	PL	0	2	8.5	2	7.2	ns	
^t PHL	ΓL	Q _n	2	8.5	2	7.2	115	



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CY74FCT191ATSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191ATSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191ATSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191CTQCT	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT191CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT191CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT191CTSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191CTSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191CTSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191CTSOCT	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT191CTSOCTG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined. Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

11-Nov-2009

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT191CTSOCT	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT191CTSOCT	SOIC	DW	16	2000	346.0	346.0	33.0

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

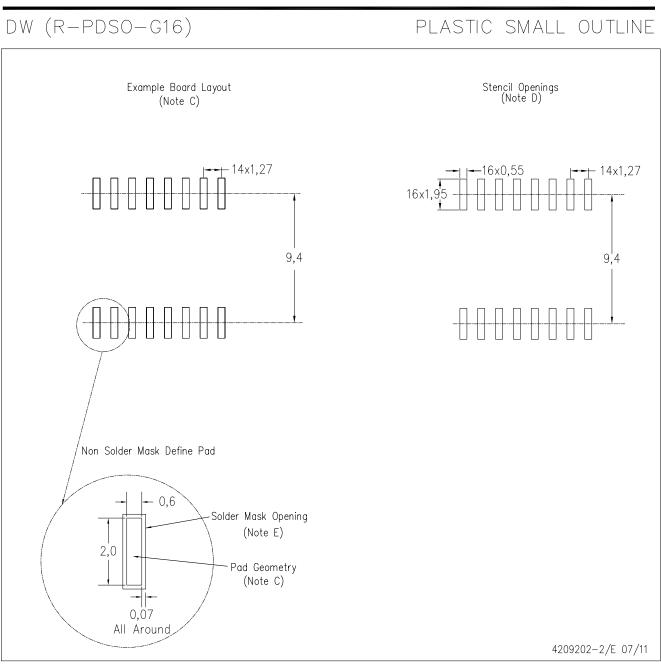
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DBQ (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



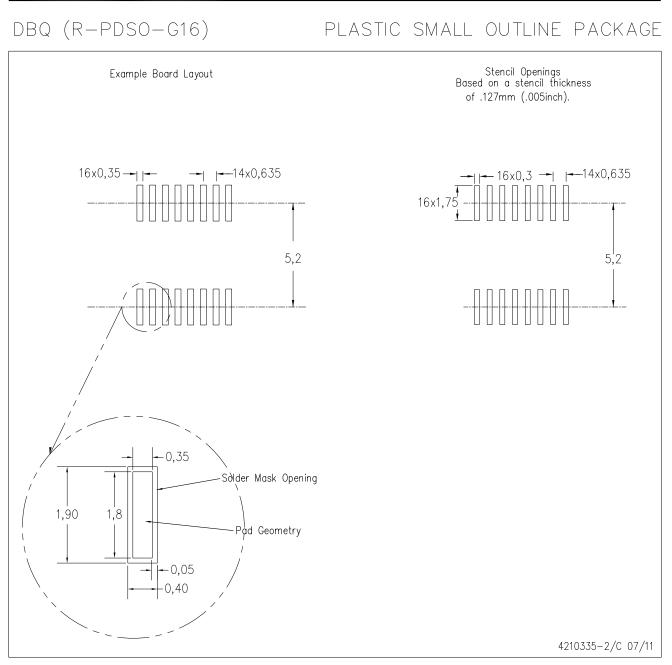
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.

D. Falls within JEDEC MO-137 variation AB.





NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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