SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Carry Look-Ahead Circuitry for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54ALS169B, SN54AS169A . . . J PACKAGE
SN74ALS169B, SN74AS169A . . . D OR N PACKAGE
(TOP VIEW)

Pin	Name		Pin	Name
1	U/$\overline{D}$		16	V_{CC}
2	CLK		15	$\overline{RCO}$
3	A		14	Q_A
4	B		13	Q_B
5	C		12	Q_C
6	D		11	Q_D
7	$\overline{ENP}$		10	$\overline{ENT}$
8	GND		9	$\overline{LOAD}$

SN54ALS169B, SN54AS169A . . . FK PACKAGE
(TOP VIEW)

Top pins: CLK (3), U/$\overline{D}$ (2), NC (1), V_{CC} (20), $\overline{RCO}$ (19)

	Pin	Name
A	4	18 Q_A
B	5	17 Q_B
NC	6	16 NC
C	7	15 Q_C
D	8	14 Q_D

Bottom pins: $\overline{ENP}$ (9), GND (10), NC (11), $\overline{LOAD}$ (12), $\overline{ENT}$ (13)

NC – No internal connection

description

These synchronous 4-bit up/down binary presettable counters feature an internal carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they may be preset to either level. The load-input circuitry allows loading with the carry-enable output of cascaded counters. Because loading is synchronous, setting up a low level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The internal carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. $\overline{ENP}$ and $\overline{ENT}$ inputs and a ripple-carry output ($\overline{RCO}$) are instrumental in accomplishing this function. Both $\overline{ENP}$ and $\overline{ENT}$ must be low to count. The direction of the count is determined by the level of the up/down (U/$\overline{D}$) input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. $\overline{ENT}$ is fed forward to enable $\overline{RCO}$. $\overline{RCO}$, thus enabled, produces a low-level pulse while the count is zero (all inputs low) counting down or maximum (15) counting up. This low-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, or U/$\overline{D}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS169B and SN54AS169A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS169B and SN74AS169A are characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
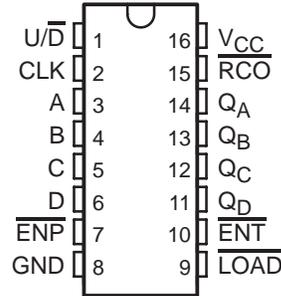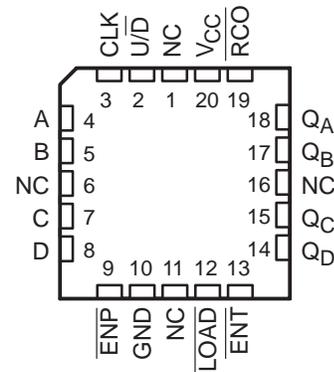
SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A
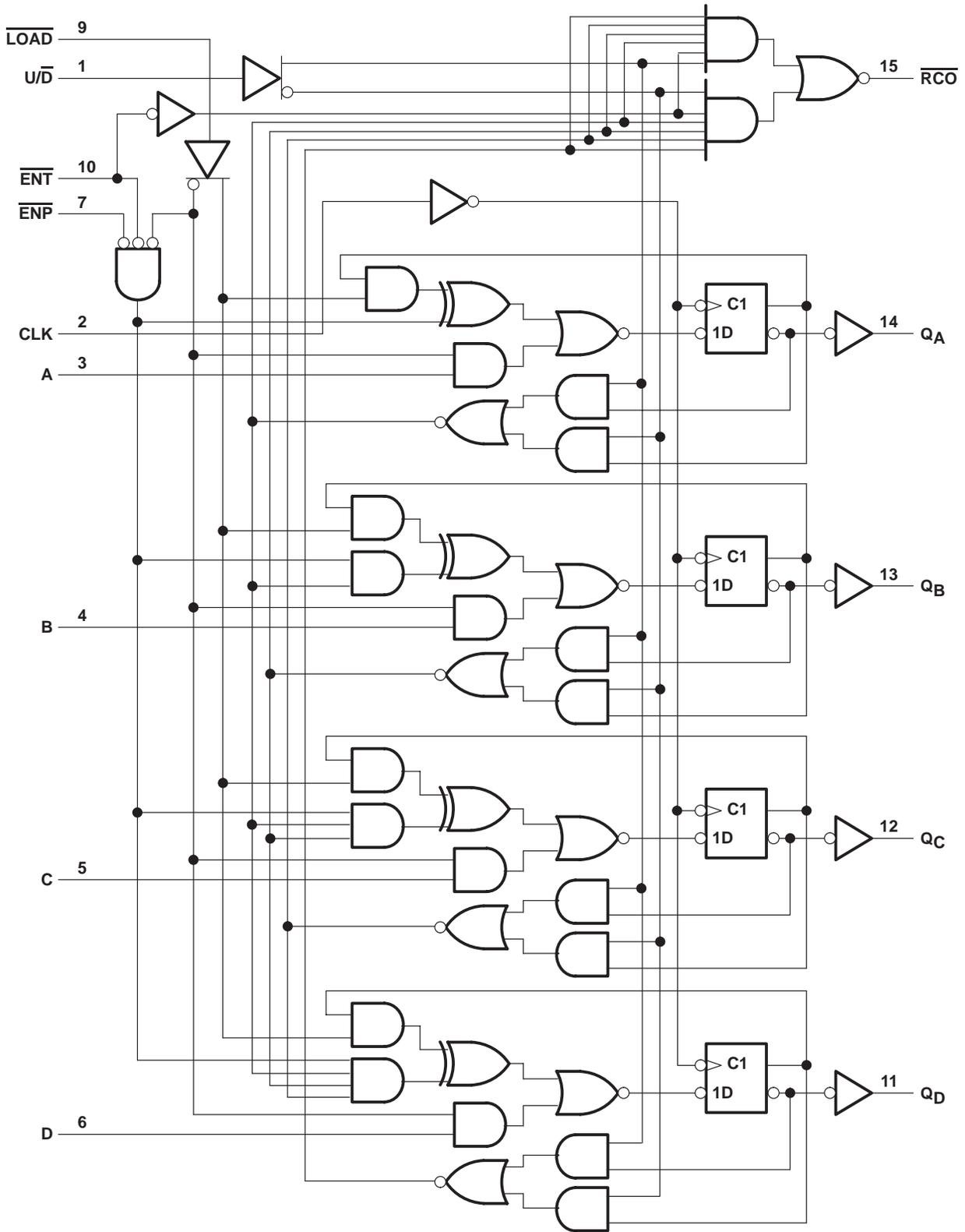# SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

logic symbol†
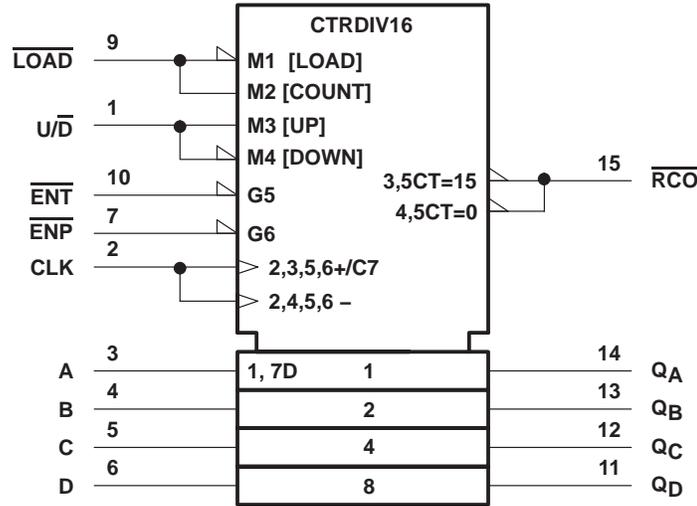
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)

Pin numbers shown are for the D, J, and N packages.

typical load, count, and inhibit sequences

The following sequence is illustrated below:

1. Load (preset) to binary 13

2. Count up to 14, 15 (maximum), 0, 1, and 2

3. Inhibit

4. Count down to 1, 0 (minimum), 15, 14, and 13
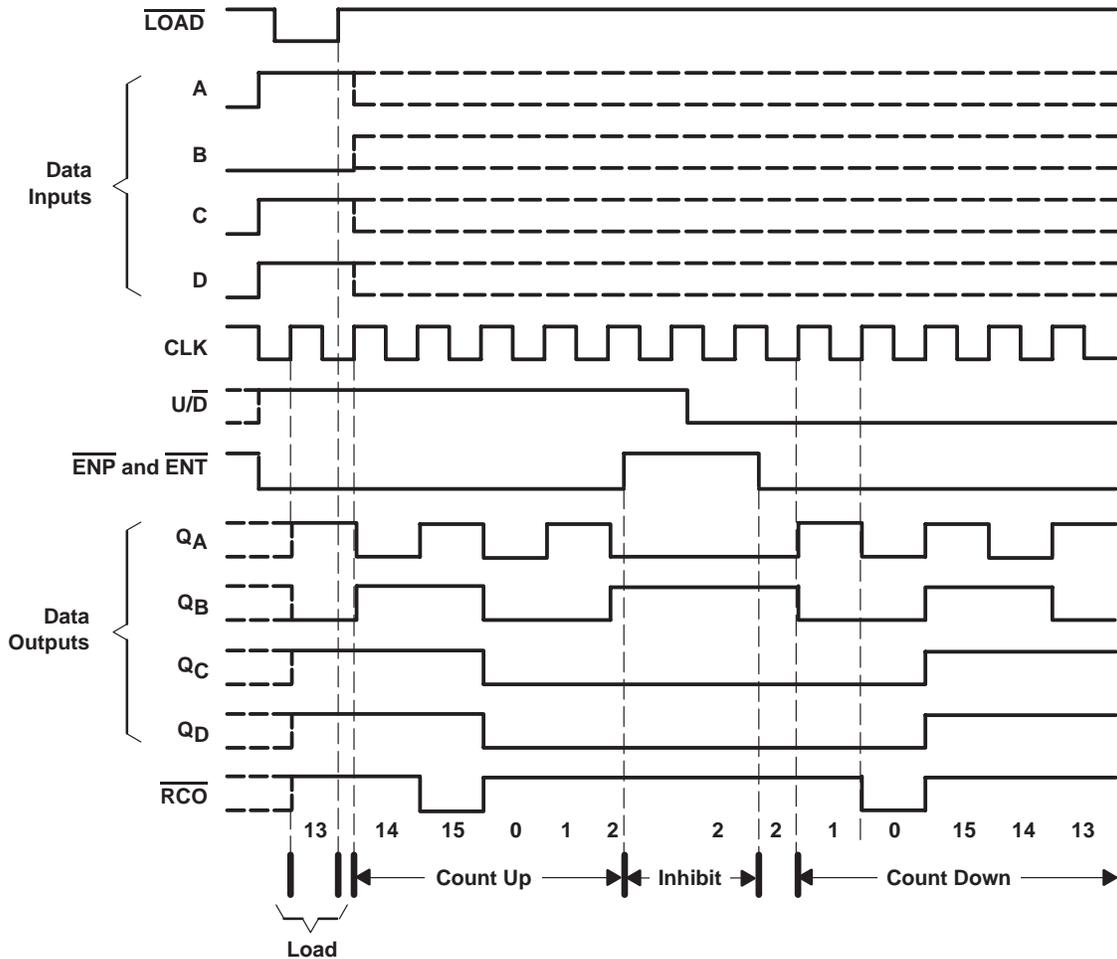
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . 7 V
Input voltage, V_I . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS169B . . . . −55°C to 125°C
　　　　　　　　　　　　　　　　　　　　　　 SN74ALS169B . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS169B			SN74ALS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		22	0		40	MHz
t_w	Pulse duration, CLK high or low		14			12.5			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			15			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	28			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS169B			SN74ALS169B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS169B		SN74ALS169B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	20	3	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	CLK	Any Q	2	20	2	15	ns
t_{PHL}			5	23	5	20	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	2	16	2	13	ns
t_{PHL}			3	24	3	16	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	4	22	5	19	ns
t_{PHL}			5	26	5	19	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Operating free-air temperature range, T_A: SN54AS169A .... −55°C to 125°C
                 SN74AS169A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS169A			SN74AS169A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}*	Clock frequency		0		60	0		75	MHz
t_w*	Pulse duration, CLK high or low		7.7			6.7			ns
t_{su}*	Setup time before CLK↑	A, B, C, or D	10			8			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			8			
		$\overline{LOAD}$	10			8			
		U/$\overline{D}$	14			11			
t_h*	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS169A			SN74AS169A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}		$V_{CC} = 4.5$ V,	$I_{OL} = 20$ mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			-1			-1	mA
	All others					-0.5			-0.5	
I_O‡		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-30		-112	-30		-112	mA
I_{CC}		$V_{CC} = 5.5$ V			41	63		41	63	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500$ Ω, $T_A =$ MIN to MAX§				UNIT
			SN54AS169A		SN74AS169A		
			MIN	MAX	MIN	MAX	
f_{max}*			60		75		MHz
t_{PLH}	CLK	$\overline{RCO}$ (LOAD high or low)	3	17.5	3	16.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.5	10	1.5	9	ns
t_{PHL}			1.5	10	1.5	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2	14	2	12	ns
t_{PHL}			2	14.5	2	13	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
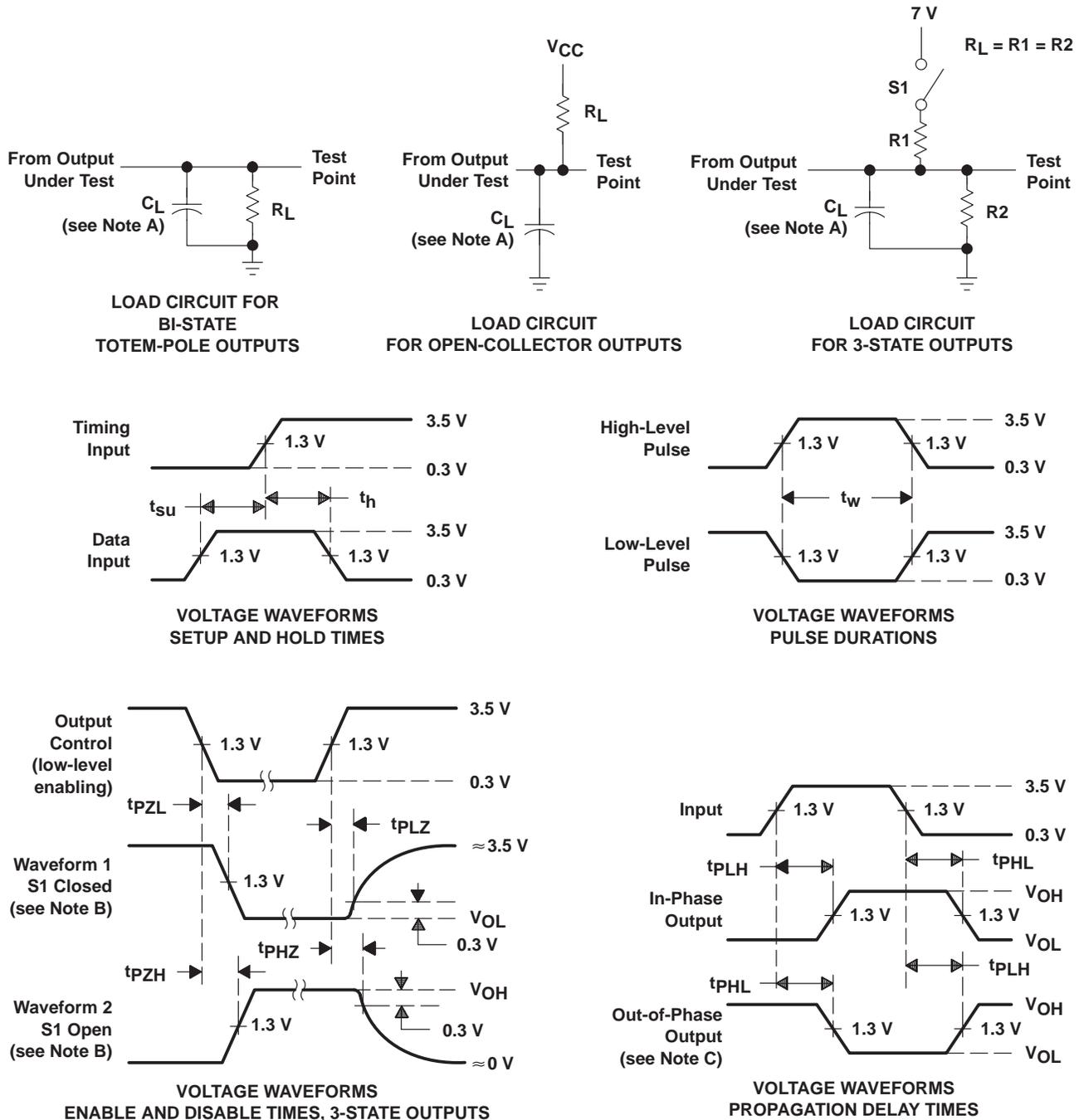
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

Figure 1. Load Circuits and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. When measuring propagation delay items of 3-state outputs, switch S1 is open.

D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

E. The outputs are measured one at a time with one transition per measurement.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
83025012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8302501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
8302501FA	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	
JM38510/38003B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/38003BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/38003B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/38003BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54ALS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54AS169AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74ALS169BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS169BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS169BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS169BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS169AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS169ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS169BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SNJ54ALS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54AS169AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ54AS169AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A :
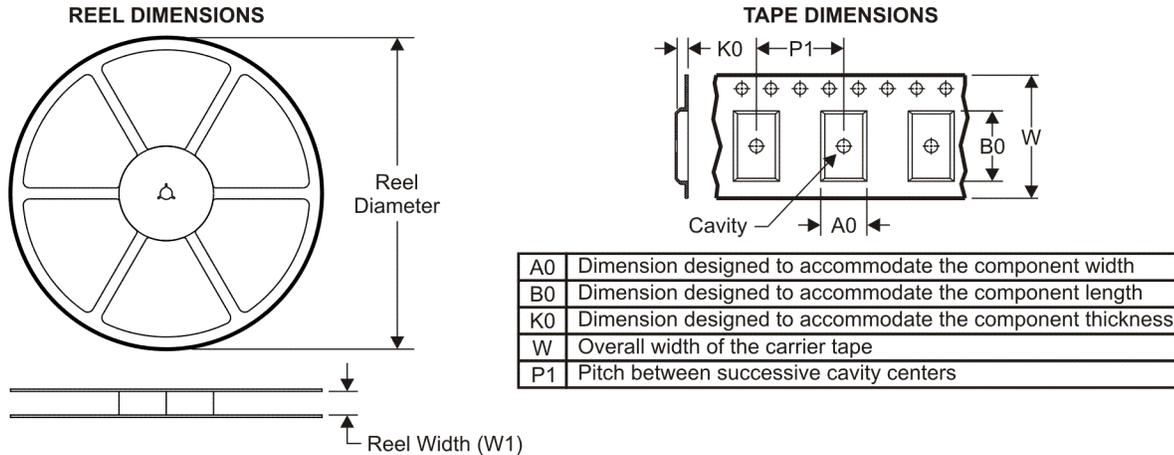
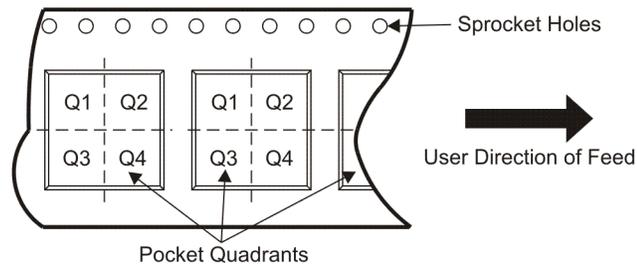- Catalog: SN74ALS169B, SN74AS169A

- Military: SN54ALS169B, SN54AS169A

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS169BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS169BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS169BDR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS169BNSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN

DIM ＼ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14　　　　　　8

1　　　　　　7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

C

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

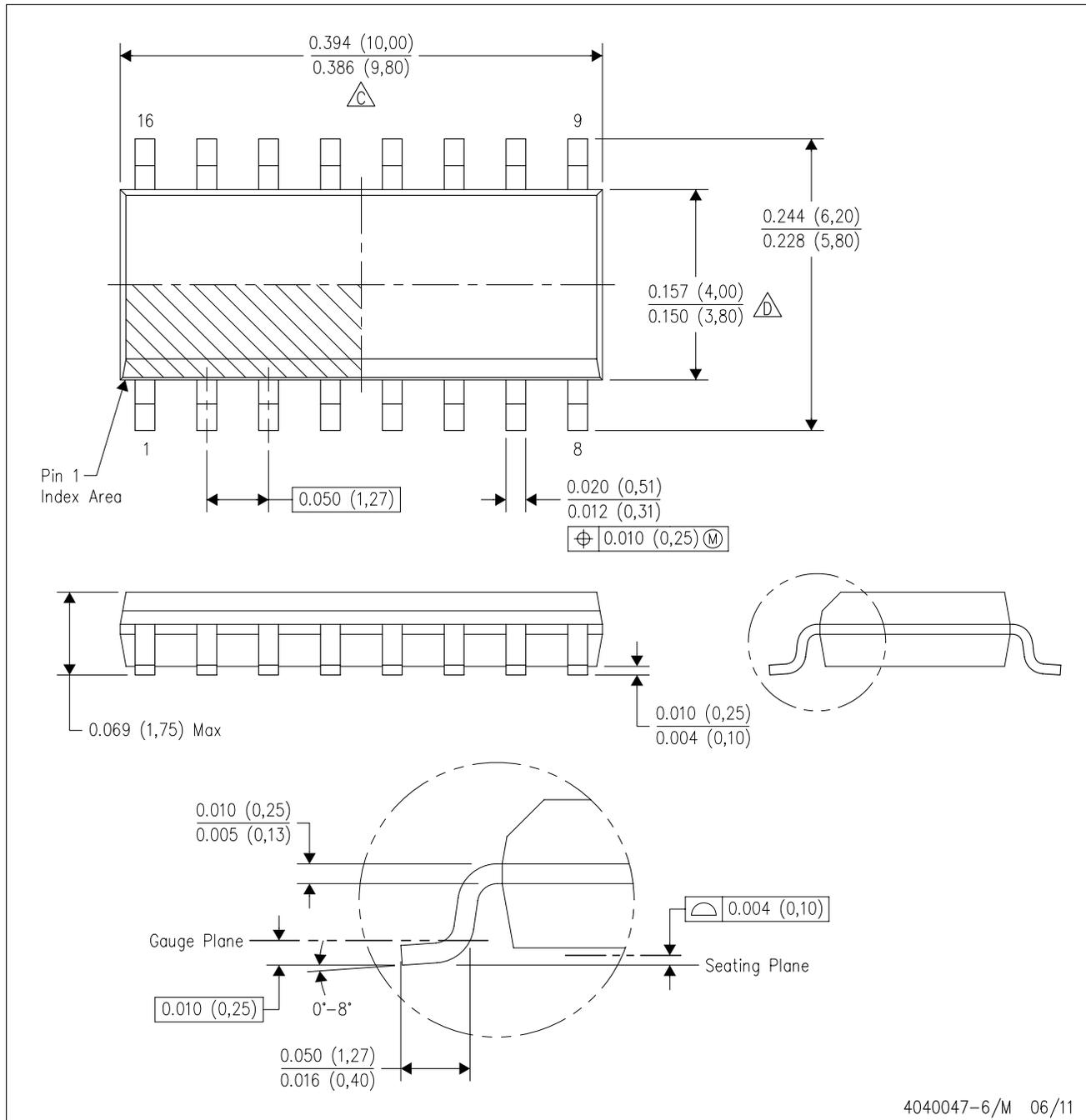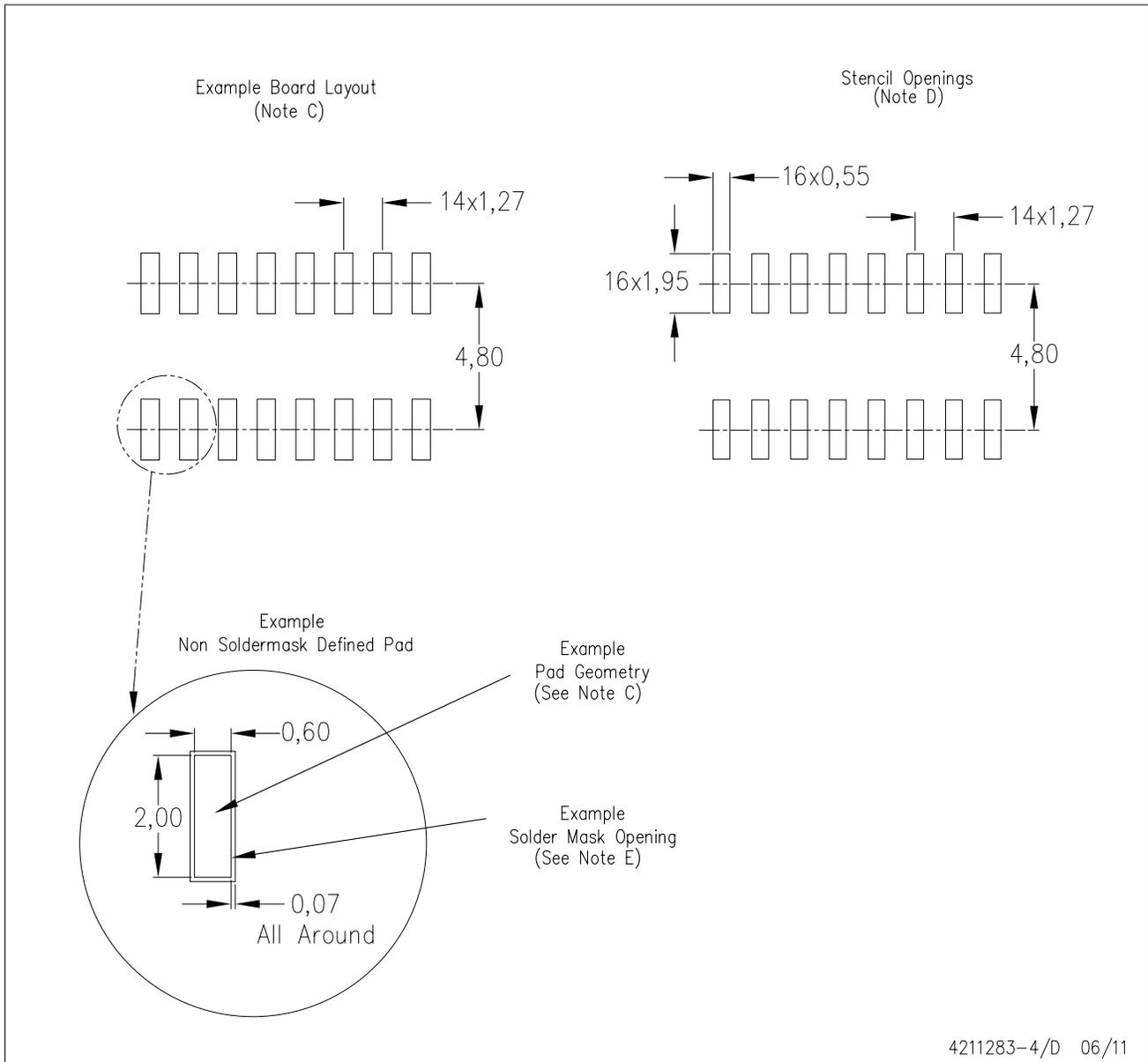0.100 (2,54)

A

0°—15°

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　B.　This drawing is subject to change without notice.
　　　　C.　This package is hermetically sealed with a ceramic lid using glass frit.
　　　　D.　Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
　　　　E.　Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R−GDFP−F16)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.285\ (7,24)}{0.245\ (6,22)}$

$\dfrac{0.080\ (2,03)}{0.055\ (1,40)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

0.305 (7,75) MAX

1   16

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

$\dfrac{0.430\ (10,92)}{0.370\ (9,40)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$
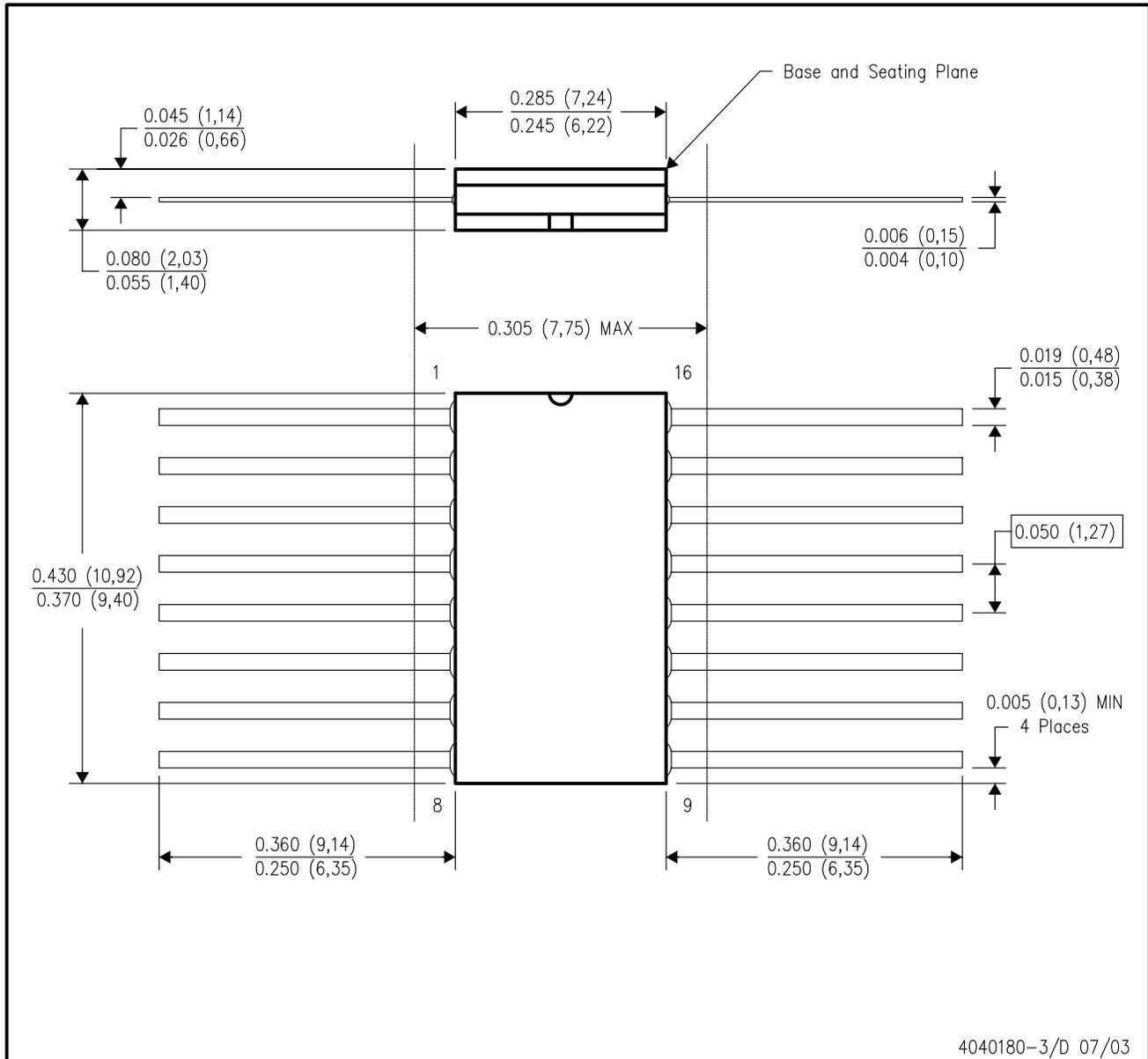
4040180−3/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only.
          E.   Falls within MIL STD 1835 GDFP1−F16 and JEDEC MO−092AC

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FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN
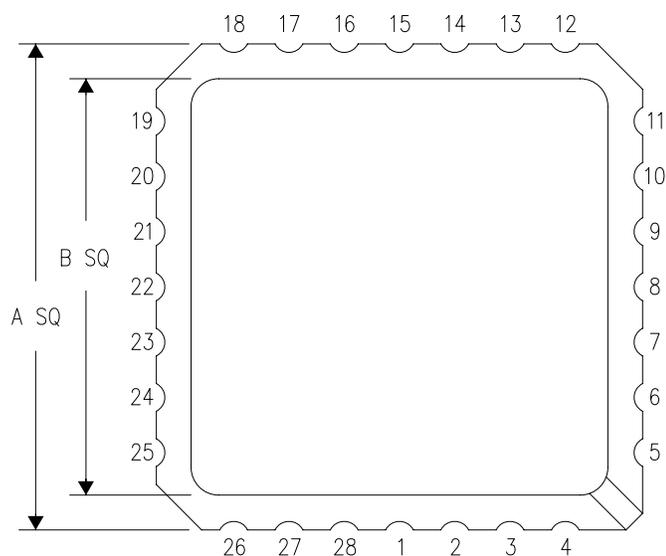
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.080\ (2,03)}{0.064\ (1,63)}$

$\dfrac{0.055\ (1,40)}{0.045\ (1,14)}$

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

$\dfrac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$
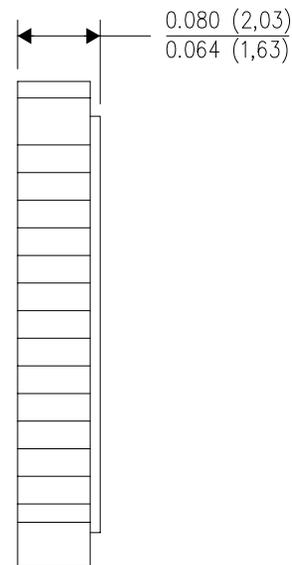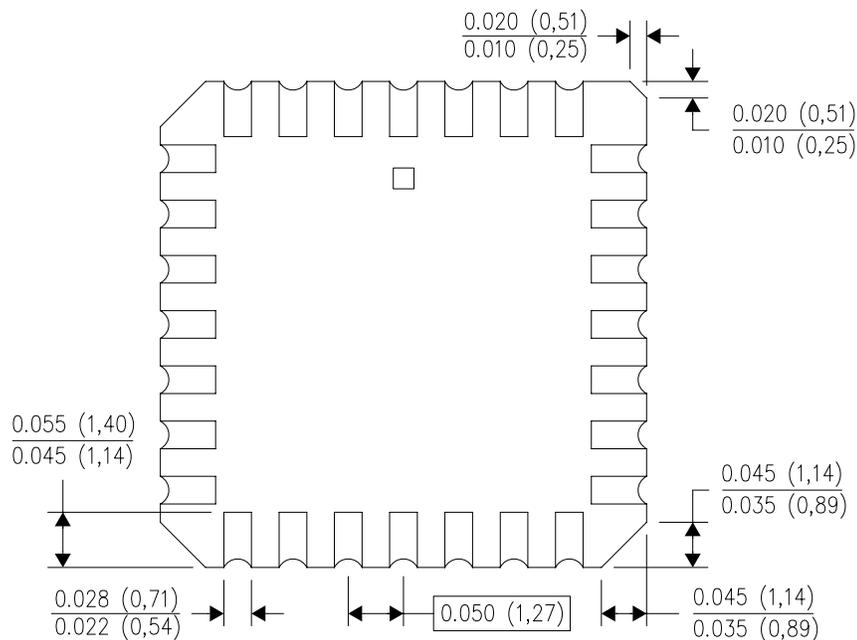
4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

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N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
          D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
       ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
       ⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←— 14x1,27

16x0,55

←— 14x1,27

16x1,95

4,80

4,80

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

2,00

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/D   06/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NS (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN
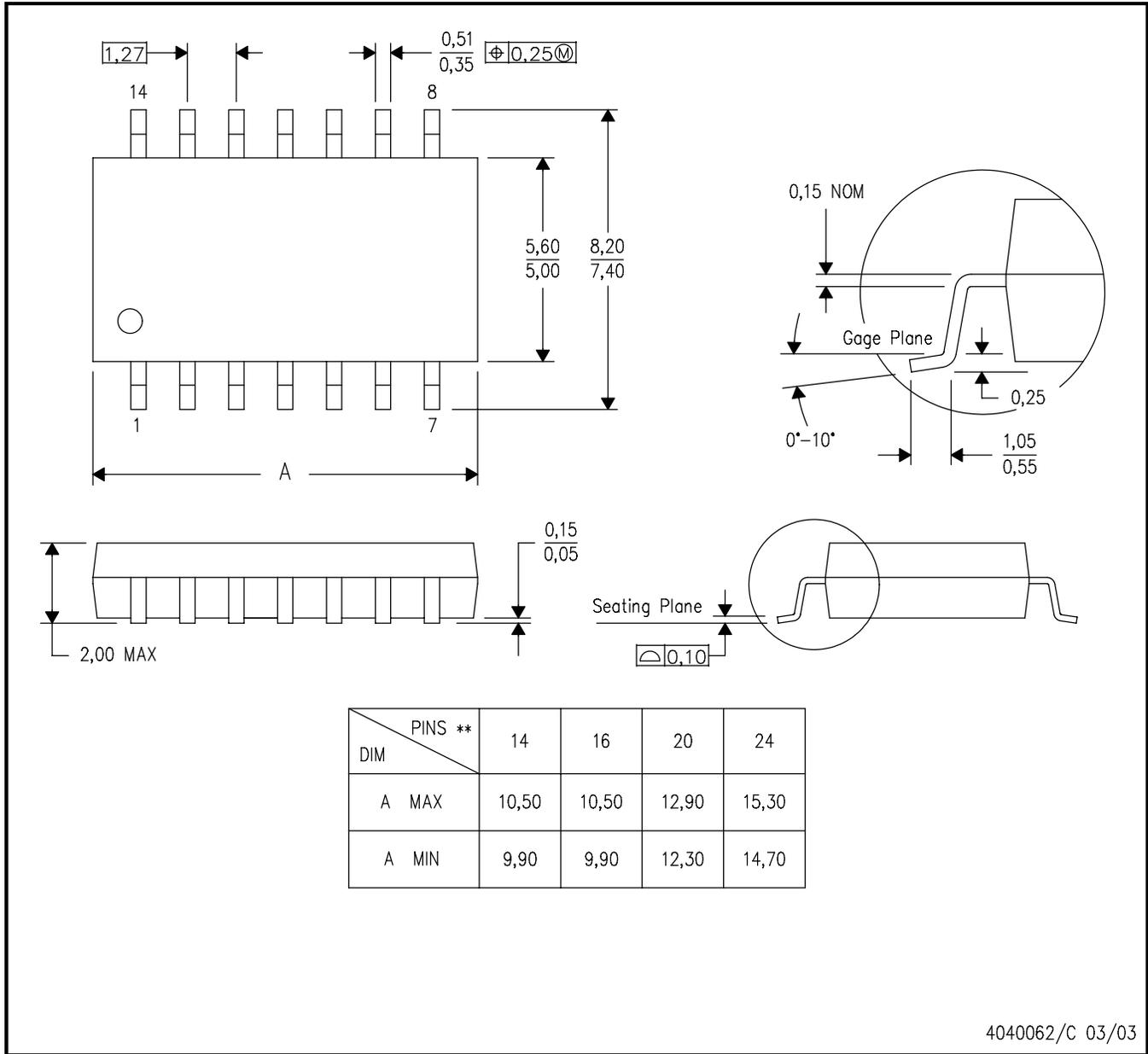
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
              B. This drawing is subject to change without notice.
              C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE