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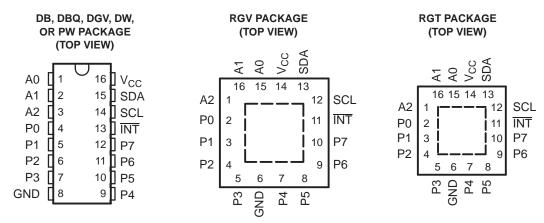
SCPS127D-SEPTEMBER 2006-REVISED AUGUST 2008

REMOTE 8-BIT I²C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

FEATURES

- I²C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/Os
- 400-kHz Fast I²C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I²C/SMBus
- Input/Output Configuration Register
- · Polarity Inversion Register
- Internal Power-On Reset

- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This 8-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface [serial clock (SCL), serial data (SDA)].

The PCA9554A consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs with a weak pullup to V_{CC} . However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9554A in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I²C/SMBus state machine.

The PCA9554A open-drain interrupt (INT) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the PCA9554A can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs and low current consumption.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I²C address and allow up to eight devices to share the same I²C bus or SMBus.

The PCA9554A is pin-to-pin and I²C address compatible with the PCF8574A. However, software changes are required, due to the enhancements in the PCA9554A over the PCF8574A.

The PCA9554A and PCA9554 are identical except for their fixed I²C address. This allows for up to 16 of these devices (8 of each) on the same I²C/SMBus.

ORDERING INFORMATION

T _A	PA	CKAGE ⁽¹⁾⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGT	Reel of 3000	PCA9554ARGTR	ZVH
	QFN – RGV	Reel of 2500	PCA9554ARGVR	PD554A
	QSOP – DBQ	Tube of 75	PCA9554ADBQ	PD554A
	QSOP - DBQ	Reel of 2500	PCA9554ADBQR	— PD554A
40°C to 95°C	SOIC DW	Tube of 40	PCA9554ADW	DCA0554A
	SOIC – DW	Reel of 2000	PCA9554ADWR	PCA9554A
-40°C to 85°C		Tube of 90	PCA9554ADB	
−40°C to 85°C	SSOP - DB	Tube of 80	PCA9554ADBG4	PD554A
		Reel of 2000	PCA9554ADBR	
	TOCOD DW	Tube of 90	PCA9554APW	DDCC4A
	TSSOP – PW	Reel of 2000	PCA9554APWR	PD554A
	TVCOD DOV	Reel of 2000	PCA9554ADGVR	DD554A
	TVSOP – DGV	Reel of 125	PCA9554ADGV	PD554A

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

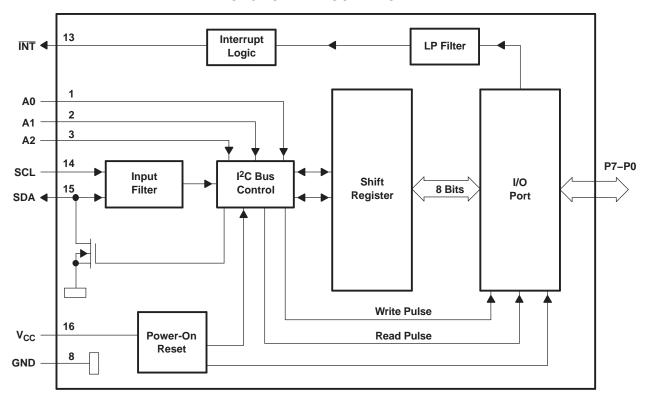
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



TERMINAL FUNCTIONS

NO.			
QSOP (DBQ) SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT AND RGV)		DESCRIPTION
1	15	A0	Address input. Connect directly to V _{CC} or ground.
2	16	A1	Address input. Connect directly to V_{CC} or ground.
3	1	A2	Address input. Connect directly to V _{CC} or ground.
4	2	P0	P-port input/output. Push-pull design structure.
5	3	P1	P-port input/output. Push-pull design structure.
6	4	P2	P-port input/output. Push-pull design structure.
7	5	P3	P-port input/output. Push-pull design structure.
8	6	GND	Ground
9	7	P4	P-port input/output. Push-pull design structure.
10	8	P5	P-port input/output. Push-pull design structure.
11	9	P6	P-port input/output. Push-pull design structure.
12	10	P7	P-port input/output. Push-pull design structure.
13	11	ĪNT	Interrupt output. Connect to V _{CC} through a pullup resistor.
14	12	SCL	Serial clock bus. Connect to V _{CC} through a pullup resistor.
15	13	SDA	Serial data bus. Connect to V _{CC} through a pullup resistor.
16	14	V _{CC}	Supply voltage

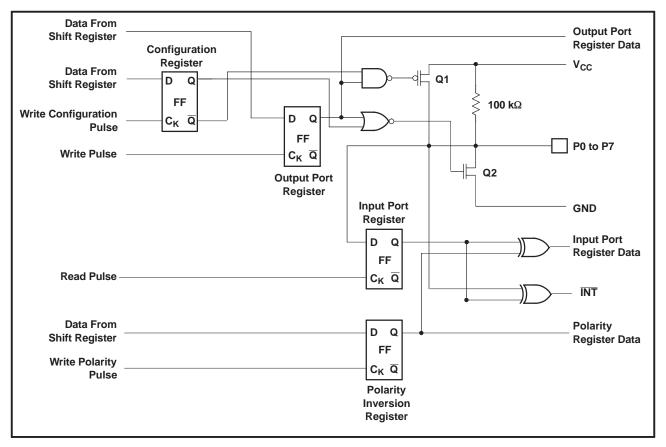
FUNCTIONAL BLOCK DIAGRAM



- A. Pin numbers shown are for the DB, DBQ, DGV, DW, or PW package.
- B. All I/Os are set to inputs at reset.



SIMPLIFIED SCHEMATIC OF P0 TO P7



A. At power-on reset, all registers return to default values.

I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high impedance input with a weak pullup (100 k Ω typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

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A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

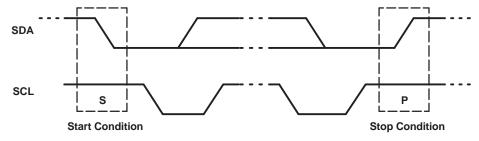


Figure 1. Definition of Start and Stop Conditions

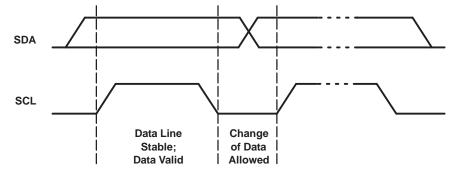


Figure 2. Bit Transfer

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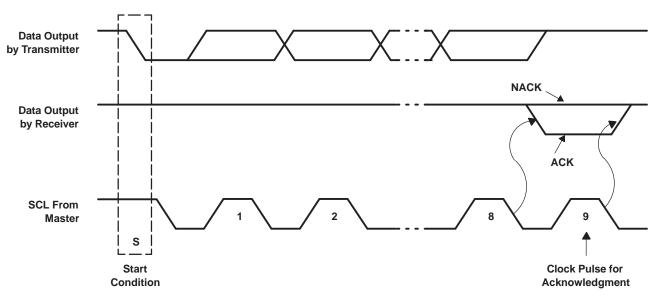


Figure 3. Acknowledgment on the I²C Bus

Interface Definition

вуте				BIT				
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C slave address	L	Н	Н	Н	A2	A1	A0	R/W
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

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Device Address

Figure 4 shows the address byte for the PCA9554A.

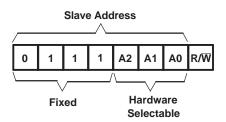


Figure 4. PCA9554A Address

Address Reference

	INPUTS		I ² C BUS SLAVE ADDRESS
A2	A1	A0	I C BUS SLAVE ADDRESS
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	Н	57 (decimal), 39 (hexadecimal)
L	Н	L	58 (decimal), 3A (hexadecimal)
L	Н	Н	59 (decimal), 3B (hexadecimal)
Н	L	L	60 (decimal), 3C (hexadecimal)
Н	L	Н	61 (decimal), 3D (hexadecimal)
Н	Н	L	62 (decimal), 3E (hexadecimal)
Н	Н	Н	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected. A low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9554A. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.



Figure 5. Control Register Bits

Command Byte

CONTROL RE	GISTER BITS	COMMAND BYTE	REGISTER	PROTOCOL	POWER-UP
B1	В0	(HEX)	REGISTER	PROTOCOL	DEFAULT
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

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Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I²C device know that the Input Port register will be accessed next.

Register 0 (Input Port Register)

BIT	17	16	15	14	13	12	I1	10
DEFAULT	X	Х	X	X	Х	Х	Χ	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Register 1 (Output Port Register)

BIT	07	O6	O5	O4	O3	O2	O1	00
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC} , an internal power-on reset holds the PCA9554A in a reset condition until V_{CC} has reached V_{POR} . At that point, the reset condition is released and the PCA9554A registers and $I^2C/SMBus$ state machine will initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

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Interrupt Output (INT)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv} , the signal \overline{INT} is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting; data is read from the port that generated the interrupt or in a Stop event. Resetting occurs in the read mode at the acknowledge (ACK) bit or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as \overline{INT} .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

INT has an open-drain structure and requires a pullup resistor to V_{CC}.

Bus Transactions

Data is exchanged between the master and PCA9554A through write and read commands.

Writes

Data is transmitted to the PCA9554A by sending the device address and setting the least-significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 6 and Figure 7). There is no limitation on the number of data bytes sent in one write transmission.

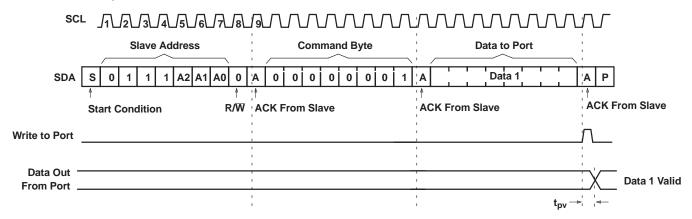


Figure 6. Write to Output Port Register

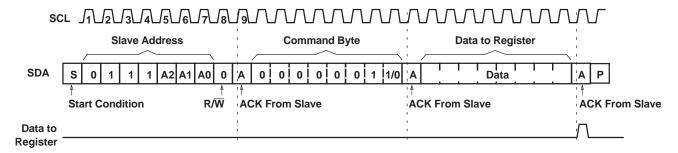


Figure 7. Write to Configuration or Polarity Inversion Registers

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Reads

The bus master first must send the PCA9554A address with the least significant bit (LSB) set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9554A (see Figure 8 and Figure 9). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

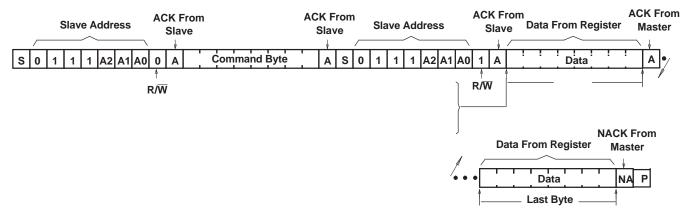
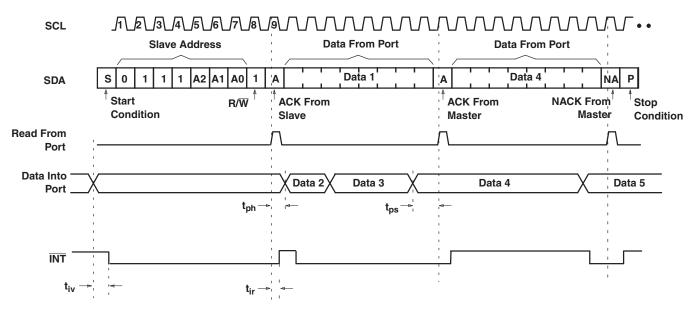


Figure 8. Read From Register



- A. This figure assumes the command byte has previously been programmed with 00h.
- B. Transfer of data can be stopped at any moment by a Stop condition.
- C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See Figure 8 for these details.

Figure 9. Read From Input Port Register

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6	V
VI	Input voltage range ⁽²⁾		-0.5	6	V
Vo	Output voltage range ⁽²⁾		-0.5	6	V
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0		-20	mA
I _{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I _{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I _{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		-50	mA
	Continuous current through GND			6 6 6 -20 -20 ±20 50	A
I _{CC}	Continuous current through V _{CC}		-250 160 82	mA	
		DB package		82	
		DBQ package		90	
	Input clamp current Output clamp current Input/output clamp current Continuous output low current Continuous output high current Continuous current through GND	DGV package		120	
θ_{JA}	Package thermal impedance (3)	DW package		57	°C/W
		PW package		108	
		RGT package		TBD	
		RGV package		6 6 -20 -20 ±20 50 -50 -250 160 82 90 120 57 108 TBD	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

				MIN	MAX	UNIT
V _{CC}	Supply voltage			2.3	5.5	V
V _{IH}	H High-level input voltage	SCL, SDA	(0.7 × V _{CC}	5.5	V
		A2-A0, P7-P0		2	5.5 5.5 5.5 0.3 × V _{CC} 0.8 -10 25	1
V	Low lovel input voltage	SCL, SDA		-0.5	5.5 5.5 2 5.5 6 0.3 × V _{CC} 6 0.8 -10 25	V
V_{IL}	Low-level input voltage	A2-A0, P7-P0		-0.5		
I _{OH}	High-level output current	P7–P0			-10	mA
I _{OL}	Low-level output current	P7–P0			25	mA
T _A	Operating free-air temperature			-40	85	°C

Product Folder Link(s): PCA9554A

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input diode clamp voltage	$I_1 = -18 \text{ mA}$	2.3 V to 5.5 V	-1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V _{POR}		1.5	1.65	V
			2.3 V	1.8		8 8 10 14 17 35 13 19 24 45 10 ±1 ±1 1 -100 04 175 50 90 20 65 60 150 15 40 8 20 50 700	
		1 - 9 mA	3 V	2.6			
		$I_{OH} = -8 \text{ mA}$	4.5 V	3.1			
,	P-port high-level output voltage (2)		4.75 V	4.1		±1 ±1 1 -100 175 90 65 150 40 20	V
/ _{OH}	P-port nign-level output voltage		2.3 V	1.7			V
		L = 10 mA	3 V	2.5			
		$I_{OH} = -10 \text{ mA}$	4.5 V	3			
			4.75 V	4			
	SDA	V _{OL} = 0.4 V	2.3 V to 5.5 V	3	8		
			2.3 V	8	10		
		V -05V	3 V	8	14		
		$V_{OL} = 0.5 \text{ V}$	4.5 V	8	17	±1 ±1 1 1 -100 65 150 40 20 700 600 500 1 0.9 0.8 1.5 5 6.5	
	P port ⁽³⁾		4.75 V	8	35		A
OL	P porto,		2.3 V	10	13		mA
		V 0.7.V	3 V	10	19		
		$V_{OL} = 0.7 \text{ V}$	4.5 V	10	24		
			4.75 V	10	45		
	ĪNT	V _{OL} = 0.4 V	2.3 V to 5.5 V	3	10		
	SCL, SDA	V V at CND	227/4- 5.57/			±1	^
ı	A2-A0	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	μΑ
IH	P port	$V_{I} = V_{CC}$	2.3 V to 5.5 V			1	μΑ
L	P port	V _I = GND	2.3 V to 5.5 V			-100	μΑ
		., .,	5.5 V		104	175	
		$V_I = V_{CC}$, $I_O = 0$, $I/O = inputs$, $f_{scl} = 400 \text{ kHz}$, No load	3.6 V		50	±1 ±1 1 -100 175 90 65 150 40 20 700 600 500 1 0.9 0.8 1.5 1 5 6.5	
	Operating mode	rsci recitalization	2.7 V		20	65	
	Operating mode		5.5 V		60	150	
		$V_I = V_{CC}$, $I_O = 0$, $I/O = inputs$, $f_{scl} = 100 \text{ kHz}$, No load	3.6 V		15	40	
		Isci = 100 M Iz, 110 Ioad	2.7 V		8	20	^
CC		., ., ., ., ., ., ., ., ., ., ., ., ., .	5.5 V		450	700	μΑ
		$V_I = GND$, $I_O = 0$, $I/O = inputs$, $f_{scl} = 0$ kHz, No load	3.6 V		300	600	
	Standby mode	-Su - Su	2.7 V		225	500	
	Standby mode		5.5 V		0.25	1	
		$V_I = V_{CC}$, $I_O = 0$, $I/O = inputs$, $f_{scl} = 0$ kHz, No load	3.6 V		0.2	0.9	
		15G 15 Ki 12, 115 15GG	2.7 V		0.1	8.0	
VI.	Additional current in standby	One input at V _{CC} = 0.6 V, Other inputs at V _{CC} or GND	2.3 V to 5.5 V			1.5	, A
ΛI _{CC}	mode	Every LED I/O at $V_I = 4.3 \text{ V}$; $f_{SCI} = 0 \text{ kHz}$	5.5 V			1	mA
ો	SCL	V _I = V _{CC} or GND	2.3 V to 5.5 V		4	5	pF
	SDA	V V or CND	221/4-551		5.5	6.5	
C_{io}	P port	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		8	9.5	pF

All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.

The total current sourced by all I/Os must be limited to 85 mA.

Each I/O must be externally limited to a maximum of 25 mA, and the P port (P0 to P7) must be limited to a maximum current of 200 mA.

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I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 10)

				STANDARD MODE I ² C BUS		E	UNIT
			MIN	MAX	MIN	MAX	
f _{scl}	I ² C clock frequency		0	100	0	400	kHz
t _{sch}	I ² C clock high time		4		0.6		μs
t _{scl}	I ² C clock low time		4.7		1.3		μs
t _{sp}	I ² C spike time			50		50	ns
t _{sds}	I ² C serial-data setup time	250		100		ns	
t _{sdh}	I ² C serial-data hold time	0		0		ns	
t _{icr}	I ² C input rise time		1000	20 + 0.1C _b ⁽¹⁾	300	ns	
t _{icf}	I ² C input fall time			300	20 + 0.1C _b ⁽¹⁾	300	ns
t _{ocf}	I ² C output fall time	10-pF to 400-pF bus		300	20 + 0.1C _b ⁽¹⁾	300	ns
t _{buf}	I ² C bus free time between Stop and	d Start	4.7		1.3		μs
t _{sts}	I ² C Start or repeated Start condition	n setup	4.7		0.6		μs
t _{sth}	I ² C Start or repeated Start condition	n hold	4		0.6		μs
t _{sps}	I ² C Stop condition setup	4		0.6		μs	
t _{vd(data)}	Valid data time	SCL low to SDA output valid	300		50		ns
t _{vd(ack)}	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	μs
C _b	I ² C bus capacitive load			400		400	ns

⁽¹⁾ C_b = Total capacitive load of one bus in pF

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 11 and Figure 12)

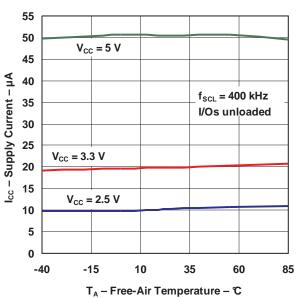
	PARAMETER	FROM (INPUT)	TO (OUTBUT)	STANDARD MO I ² C BUS	FAST MODE I ² C BUS		UNIT	
		(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t _{iv}	Interrupt valid time	P port	ĪNT		4		4	μs
t _{ir}	Interrupt reset delay time	SCL	ĪNT		4		4	μs
t _{pv}	Output data valid	SCL	P7-P0		200		200	ns
t _{ps}	Input data setup time	P port	SCL	100		100		ns
t _{ph}	Input data hold time	P port	SCL	1		1		μs

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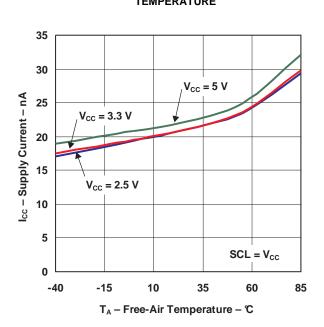


TYPICAL CHARACTERISTICS

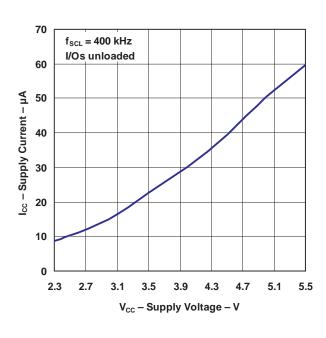




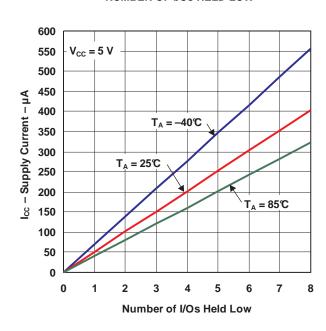
QUIESCENT SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



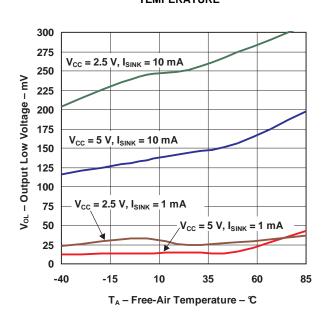
SUPPLY CURRENT vs NUMBER OF I/Os HELD LOW



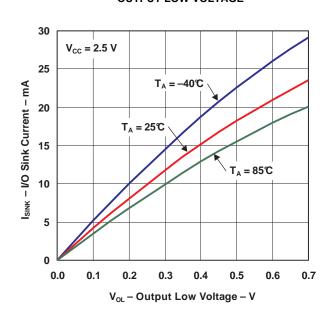


TYPICAL CHARACTERISTICS (continued)

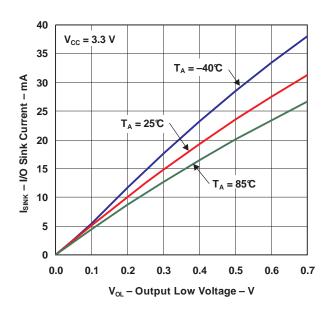
I/O OUTPUT LOW VOLTAGE vs TEMPERATURE



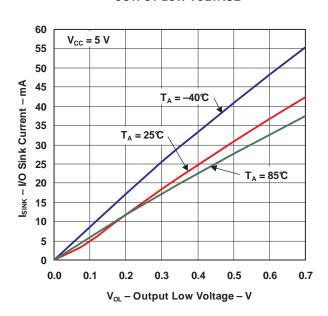
I/O SINK CURRENT vs OUTPUT LOW VOLTAGE



I/O SINK CURRENT vs OUTPUT LOW VOLTAGE



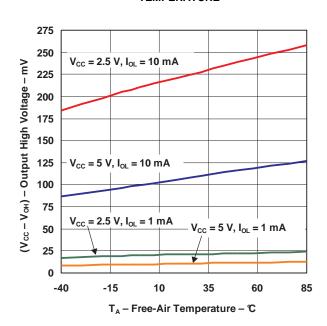
I/O SINK CURRENT vs OUTPUT LOW VOLTAGE



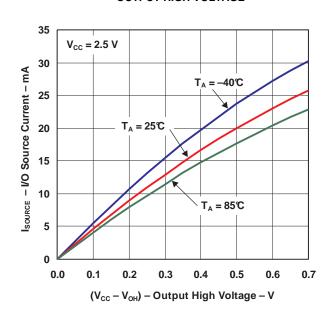


TYPICAL CHARACTERISTICS (continued)

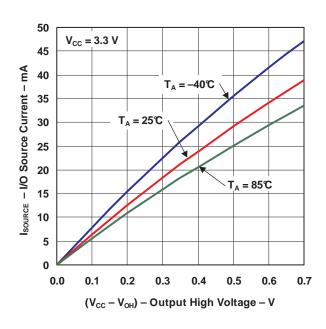
I/O OUTPUT HIGH VOLTAGE VS TEMPERATURE



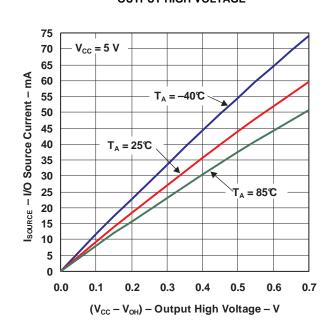
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



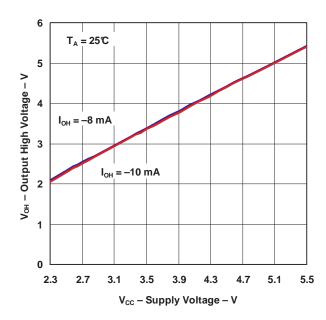
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE





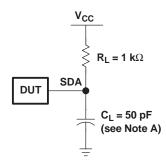
TYPICAL CHARACTERISTICS (continued)

OUTPUT HIGH VOLTAGE VS SUPPLY VOLTAGE

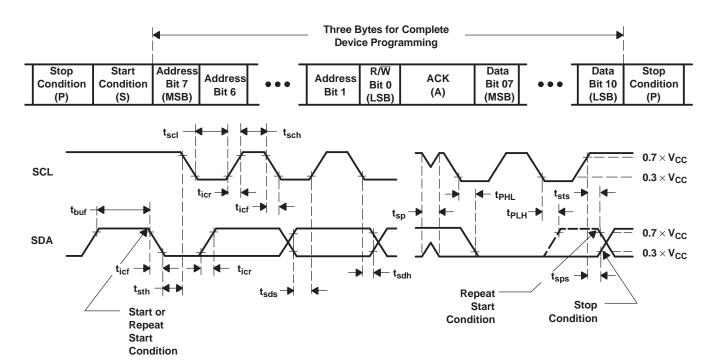




PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

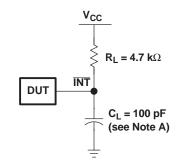
BYTE	DESCRIPTION
1	I ² C address
2, 3	P-port data

- A. C_I includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_r/t_f \leq$ 30 ns.
- C. All parameters and waveforms are not applicable to all devices.

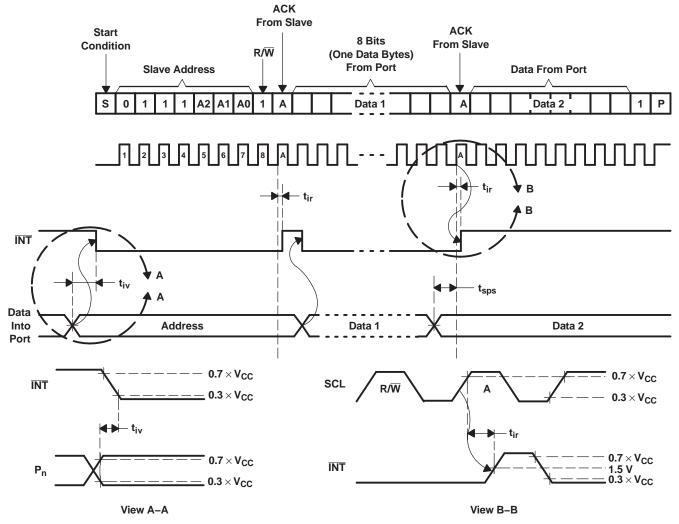
Figure 10. I²C Interface Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)



INTERRUPT LOAD CONFIGURATION

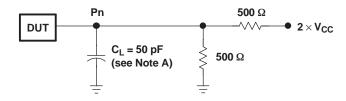


- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
- C. All parameters and waveforms are not applicable to all devices.

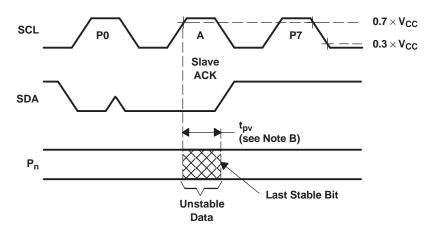
Figure 11. Interrupt Load Circuit and Voltage Waveforms



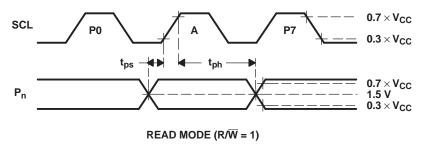
PARAMETER MEASUREMENT INFORMATION (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE $(R/\overline{W} = 0)$

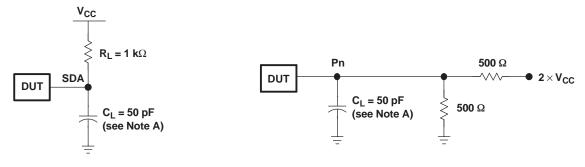


- A. C_L includes probe and jig capacitance.
- B. t_{pv} is measured from 0.7 x V_{CC} on SCL to 50% I/O pin output.
- C. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_r/t_f \leq$ 30 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 12. P-Port Load Circuit and Voltage Waveforms

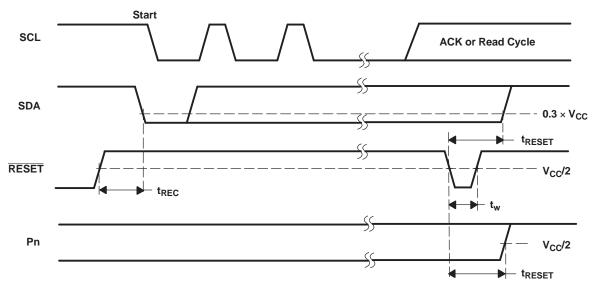


PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION



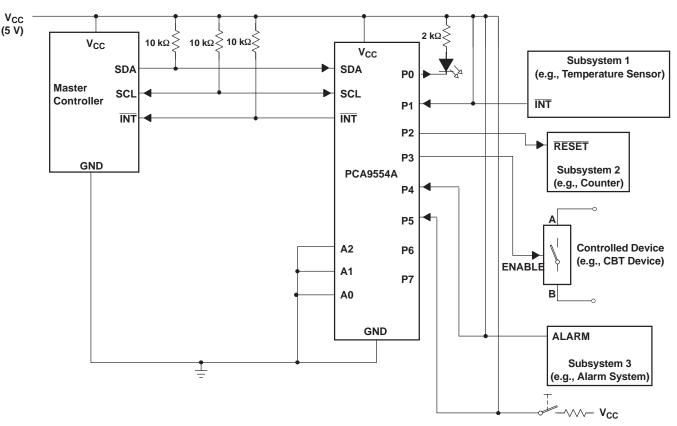
- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f/t_f \leq$ 30 ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 13. Reset Load Circuits and Voltage Waveforms



APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9554A can be used.



- A. Device address is configured as 0111000 for this example.
- B. P0, P2, and P3 are configured as outputs.
- C. P1, P4, and P5 are configured as inputs.
- D. P6 and P7 are not used and have internal 100- $k\Omega$ pullup resistors to protect them from floating.

Figure 14. Typical Application

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Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Figure 14. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC} . The supply current, I_{CC} , increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.

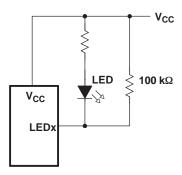


Figure 15. High-Value Resistor in Parallel With the LED

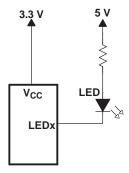


Figure 16. Device Supplied by a Lower Voltage

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PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCA9554ADB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9554ARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9554ARGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9554ARGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9554ARGVRG4	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

 $^{^{(1)}}$ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

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package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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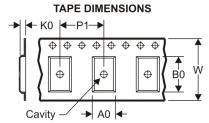
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9554ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
PCA9554ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9554ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9554APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9554ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PCA9554ARGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9554ADBR	SSOP	DB	16	2000	346.0	346.0	33.0
PCA9554ADGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
PCA9554ADWR	SOIC	DW	16	2000	346.0	346.0	33.0
PCA9554APWR	TSSOP	PW	16	2000	346.0	346.0	29.0
PCA9554ARGTR	QFN	RGT	16	3000	346.0	346.0	29.0
PCA9554ARGVR	VQFN	RGV	16	2500	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD 3,15 2,85 - A В 3,15 2,85 PIN 1 INDEX AREA TOP AND BOTTOM 0,20 REF. SEATING PLANE 0,08 0,05 0,00 Ċ 16 THERMAL PAD SIZE AND SHAPE SHOWN ON SEPARATE SHEET

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

12

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.

13

- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

16X $\frac{0,30}{0,18}$

0,50

0,10 M C A B 0,05 M C

4203495/H 10/11

F. Falls within JEDEC MO-220.



RGT (S-PVQFN-N16)

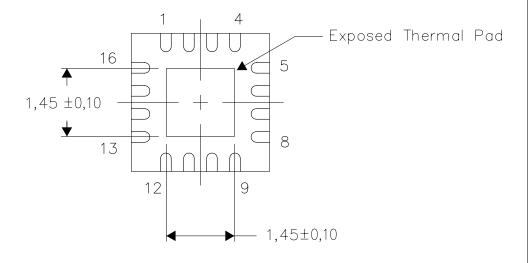
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

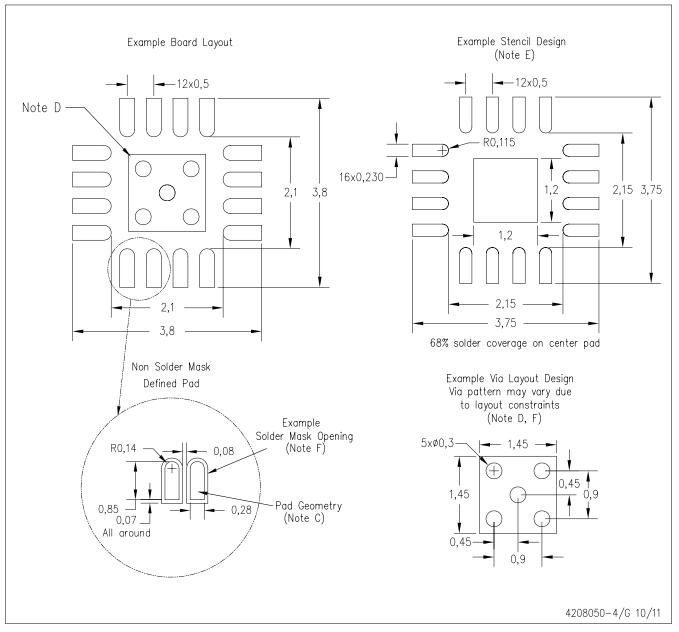
4206349-2/Q 10/11

NOTE: All linear dimensions are in millimeters



RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.





- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.



RGV (S-PVQFN-N16)

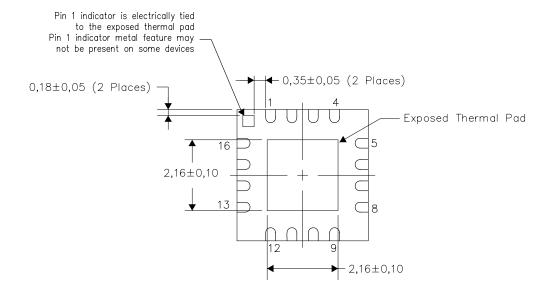
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

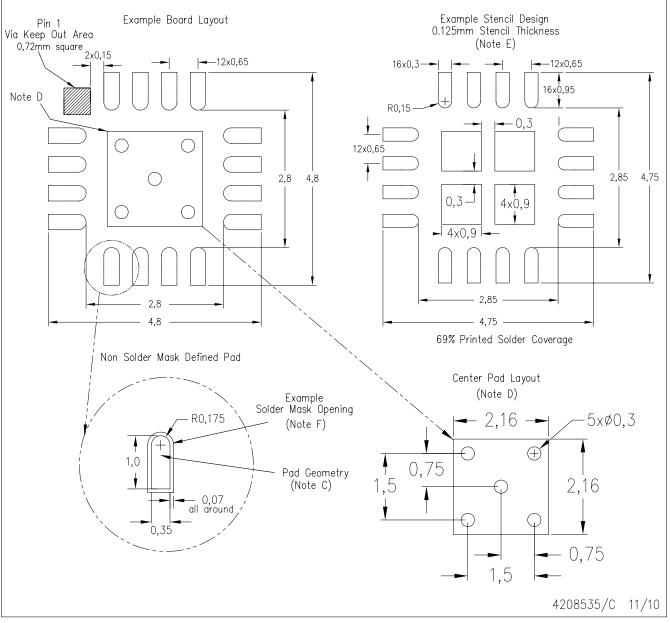
4206351-2/J 06/11

NOTE: All linear dimensions are in millimeters



RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com https://www.ti.com.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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