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SLLS723B - APRIL 2006-REVISED NOVEMBER 2009

DUAL RS-232 DRIVER/RECEIVER WITH IEC61000-4-2 PROTECTION

Check for Samples: MAX232E

FEATURES

- Meets or Exceeds TIA/RS-232-F and ITU Recommendation V.28
- **Operates From a Single 5-V Power Supply** With 1.0-µF Charge-Pump Capacitors
- Operates up to 250 kbit/s
- **Two Drivers and Two Receivers**
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- **ESD Protection for RS-232 Bus Pins**
 - ±15-kV Human-Body Model (HBM)
 - ±8-kV IEC61000-4-2, Contact Discharge
 - ±15-kV IEC61000-4-2, Air-Gap Discharge

APPLICATIONS

- **TIA/RS-232-F**
- **Battery-Powered Systems**
- **Terminals**
- **Modems**
- Computers

D. DW, N, NS, OR PW PACKAGE (TOP VIEW) C1+ **∏** 1 16 V_{CC} 🛮 GND V_{S+} [] 2 15 14 DOUT1 C1− **П** 3 C2+ [4 13 RIN1 C2- 1 5 12 ROUT1 11 DIN1 V_{S-} 6 DOUT2 7 10 DIN2 RIN2 [ROUT2

DESCRIPTION/ORDERING INFORMATION

The MAX232E is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/RS-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/RS-232-F inputs to 5-V TTL/CMOS levels. This receiver has a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/RS-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Table 1. ORDERING INFORMATION⁽¹⁾

T _A	P.A	ACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	MAX232ECN	MAX232ECN
	SOIC - D	Tube of 40	MAX232ECD	MAYOOFO
	201C – D	Reel of 2500	MAX232ECDR	MAX232EC
0°C to 70°C	COIC DW	Tube of 40	MAX232ECDW	MAYOOFO
	SOIC – DW	Reel of 2000	MAX232ECDWR	MAX232EC
	TCCOD DW	Tube of 25	MAX232ECPW	MAGGGEO
	TSSOP – PW	Reel of 2000	MAX232ECPWR	MA232EC
	PDIP – N	Tube of 25	MAX232EIN	MAX232EIN
	COIC D	Tube of 40	MAX232EID	MAYOOFI
	SOIC – D	Reel of 2500	MAX232EIDR	MAX232EI
-40°C to 85°C	COIC DW	Tube of 40	MAX232EIDW	MAYOOFI
	SOIC – DW	Reel of 2000	MAX232EIDWR	MAX232EI
	TCCOD DW	Tube of 25	MAX232EIPW	MDOOOEL
	TSSOP – PW	Reel of 2000	MAX232EIPWR	MB232EI

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 2. FUNCTION TABLES

Each Driver⁽¹⁾

INPUT DIN	OUTPUT DOUT
L	Н
Н	L

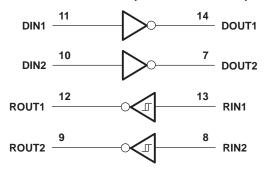
(1) H = high level, L = low level

Table 3. Each Receiver⁽¹⁾

INPUT RIN	OUTPUT ROUT
L	Н
Н	L

(1) H = high level, L = low level

LOGIC DIAGRAM (POSITIVE LOGIC)



⁽²⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Input supply voltage range (2)		-0.3	6	V
V _{S+}	Positive output supply voltage range		V _{CC} - 0.3	15	V
V _S _	Negative output supply voltage range		-0.3	-15	V
V	land to talk and an area	Driver	-0.3	V _{CC} + 0.3	\/
VI	Input voltage range	Receiver		±30	V
W	Outrot valtage reserv	DOUT	V _{S-} - 0.3	V _{S+} + 0.3	\ /
Vo	Output voltage range	ROUT	-0.3	V _{CC} + 0.3	V
	Short-circuit duration	DOUT		Unlimited	
		D package		73	
0	Declines the world in a dame (3) (4)	DW package		57	00/11/
θ_{JA}	Package thermal impedance (3) (4)	N package		67	°C/W
		PW package		108	
TJ	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltages are with respect to network GND.

The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

	-		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage (DIN1, DIN2)		2			V
V_{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)				±30	V
_	On a set in a face of the second set up	MAX232EC	0		70	90
¹A	Operating free-air temperature	MAX232EI	-40		85	°C

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

	PARAMETER	TEST CONDITIONS			TYP ⁽²⁾	MAX	UNIT
I_{CC}	Supply current	$V_{CC} = 5.5 V,$	All outputs open, T _A = 25°C		8	10	mA

Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V ± 0.5 V. All typical values are at V_{CC} = 5 V and T_A = 25°C.

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Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.



DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature range

	PARAMETER	TEST CON	MIN	TYP ⁽²⁾	MAX	UNIT		
V_{OH}	High-level output voltage	DOUT	$R_L = 3 \text{ k}\Omega \text{ to GND}$		5	7		V
V_{OL}	Low-level output voltage (3)	DOUT	$R_L = 3 \text{ k}\Omega \text{ to GND}$			-7	– 5	V
ro	Output resistance	DOUT	$V_{S+} = V_{S-} = 0,$	V _O = ±2 V	300			Ω
l _{OS}	Short-circuit output current	DOUT	V _{CC} = 5.5 V,	V _O = 0		±10		mA
I _{IS}	Short-circuit input current	DIN	V _I = 0				200	μΑ

- (1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.
 (2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
 (3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
- (4) Not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

 V_{CC} = 5 V, T_A = 25°C (see Note 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One DOUT switching		250		kbit/s

⁽¹⁾ Test conditions are C1-C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

ESD protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
	НВМ	±15	kV
DOUT, RIN	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

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RECEIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature range

	PARAMETER		TEST COI	MIN	TYP ⁽²⁾	MAX	UNIT	
V _{OH}	High-level output voltage	ROUT	$I_{OH} = -1 \text{ mA}$		3.5			V
V _{OL}	Low-level output voltage (3)	ROUT	$I_{OL} = 3.2 \text{ mA}$				0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	RIN	V _{CC} = 5 V,	T _A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	RIN	V _{CC} = 5 V,	T _A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	RIN	V _{CC} = 5 V		0.2	0.5	1	V
ri	Receiver input resistance	RIN	V _{CC} = 5 V,	T _A = 25°C	3	5	7	kΩ

Switching Characteristics(1)

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C} \text{ (see Figure 1)}$

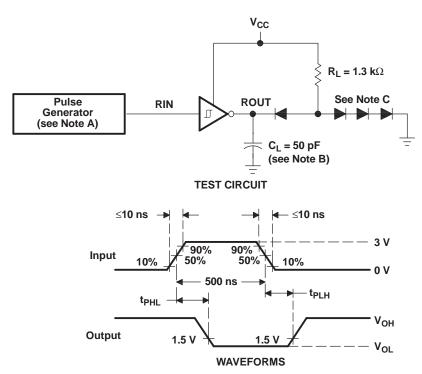
	PARAMETER	TYP	UNIT
t _{PLH(R)}	Receiver propagation delay time, low- to high-level output	500	ns
t _{PHL(R)}	Receiver propagation delay time, high- to low-level output	500	ns

(1) Test conditions are C1-C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

 ⁽¹⁾ Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
 (2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
 (3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.



PARAMETER MEASUREMENT INFORMATION

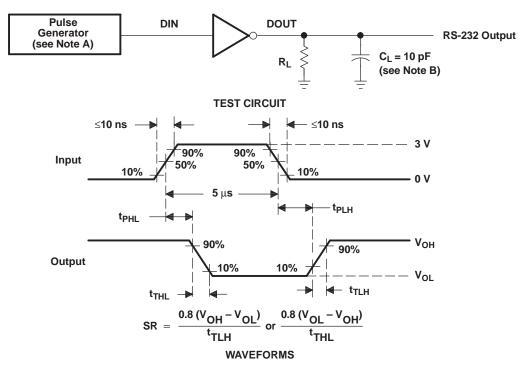


- A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

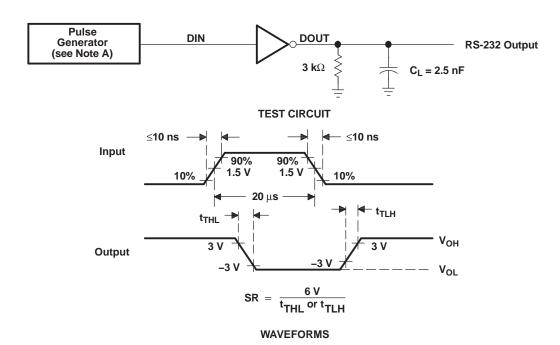


PARAMETER MEASUREMENT INFORMATION (continued)



- A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-μs Input)

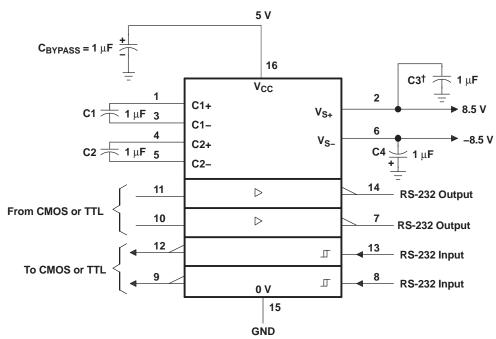


A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)



APPLICATION INFORMATION



 $^{^\}dagger$ C3 can be connected to V_{CC} or GND.

- A. Resistor values shown are nominal.
- B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-μF capacitors shown, the MAX202E can operate with 0.1-μF capacitors.

Figure 4. Typical Operating Circuit

23-Jan-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
MAX232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
MAX232ECNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
MAX232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





www.ti.com 23-Jan-2012

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
MAX232EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
MAX232EINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
MAX232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MAX232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

23-Jan-2012

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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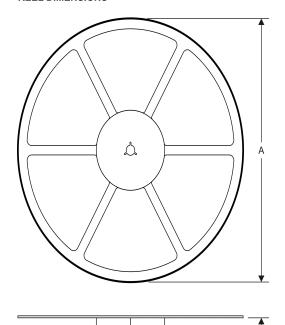
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



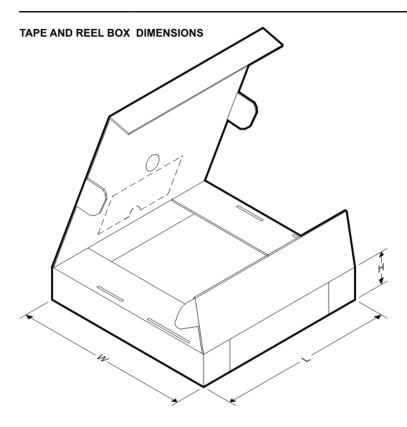
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232ECDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232ECDR	SOIC	D	16	2500	346.0	346.0	33.0
MAX232ECDWR	SOIC	DW	16	2000	366.0	364.0	50.0
MAX232ECDWRG4	SOIC	DW	16	2000	346.0	346.0	33.0
MAX232ECPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
MAX232EIDR	SOIC	D	16	2500	346.0	346.0	33.0
MAX232EIDWR	SOIC	DW	16	2000	346.0	346.0	33.0
MAX232EIPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



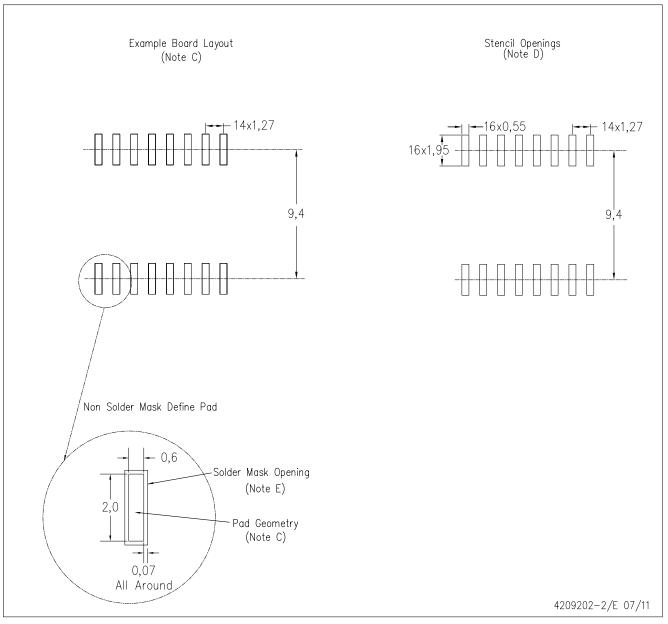
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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