

FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.5 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C

DESCRIPTION/ORDERING INFORMATION

D OR PW PACKAGE (TOP VIEW) 14 Vcc 1A 1Y [2 13 🛛 6A 2A 🛛 3 12 6Y 2Y 4 11 **1** 5A 10 5Y 3A 5 3Y 6 9[] 4A GND 8 4Y

The SN74LVC04A hex inverter contains six independent inverters designed for 2.7-V to 3.6-V V_{CC} operation.

The device performs the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION⁽¹⁾

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC04AQDRQ1	LVC04AQ
-40 C 10 125 C	TSSOP – PW	Reel of 2000	SN74LVC04AQPWRQ1	LVC04AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
Н	L
L	н

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC04A-Q1 HEX INVERTER

SCAS704B-SEPTEMBER 2003-REVISED FEBRUARY 2008



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V _{CC}	Supply voltage range			-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V	
Vo	Output voltage range ⁽²⁾⁽³⁾			-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0			-50	mA
I _{OK}	Output clamp current	V _O < 0			-50	mA
I _O	Continuous output current				±50	mA
	Continuous current through V_{CC} or GN	D			±100	mA
0	Package thermal impedance ⁽⁴⁾	D package			86	°C/W
θ_{JA}	Fackage mermai impedance ?	PW package			113	C/W
T _{stg}	Storage temperature range			-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V	Supply voltage Operating Data retention only		2	3.6	V
V _{CC}			1.5		v
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V_{CC}	V
	High lovel output ourrent	$V_{CC} = 2.7 V$		-12	mA
IOH	High-level output current V _{CC} = 3 V			-24	ША
	Low lovel output ourrept	$V_{CC} = 2.7 V$		12	mA
IOL	Low-level output current $V_{CC} = 3 V$			24	ША
T _A	Operating free-air temperature		-40	125	°C

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

2



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾	MAX	UNIT	
	I _{OH} = -100 μA	2.7 V to 3.6 V	V _{CC} – 0.2			
N/	1. 10 m/	2.7 V	2.2		V	
V _{OH}	$I_{OH} = -12 \text{ mA}$	3 V	2.4			
	I _{OH} = -24 mA	3 V	2.2		1	
	I _{OL} = 100 μA	2.7 V to 3.6 V		0.2		
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
I _I	$V_{I} = 5.5 \text{ V or GND}$	3.6 V		±5	μA	
I _{CC}	$V_{I} = V_{CC} \text{ or } \text{GND}, I_{O} = 0$	3.6 V		10	μA	
ΔI _{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V		500	μA	
Ci	$V_{I} = V_{CC} \text{ or } GND$	3.3 V	5		pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX	
t _{pd}	А	Y		5.5	0.5	4.5	ns

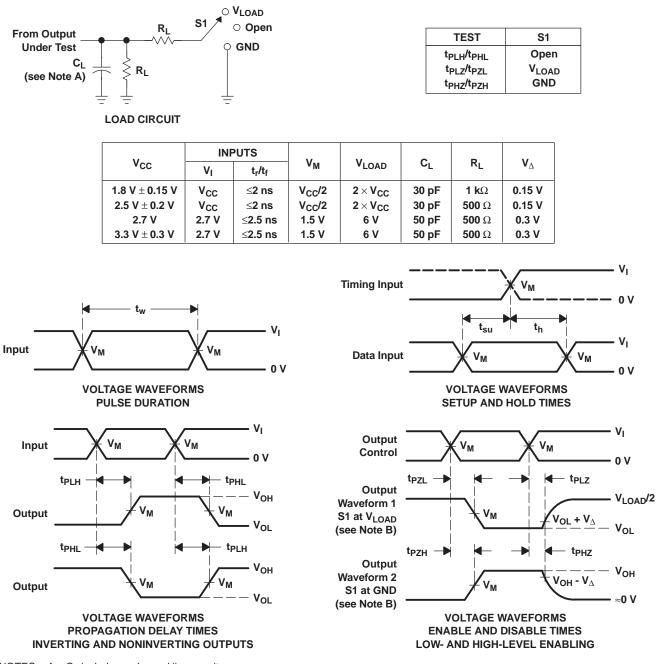
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C _{pd}	Power dissipation capacitance per inverter	f = 10 MHz	7	8	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

4



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC04AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC04AQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC04AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC04AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC04A-Q1 :





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12-Oct-2011

• Catalog: SN74LVC04A

Enhanced Product: SN74LVC04A-EP

Military: SN54LVC04A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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