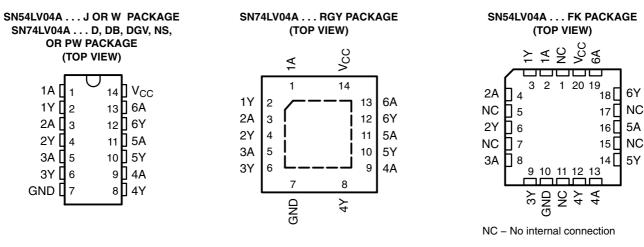
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- 2-V to 5.5-V V<sub>CC</sub> Operation
- Max t<sub>pd</sub> of 6.5 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V,  $T_A = 25^{\circ}C$
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot) >2.3 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C

- Support Mixed-Mode Voltage Operation on All Ports
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22

   2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description/ordering information

These hex inverters are designed for 2-V to 5.5-V V<sub>CC</sub> operation. The 'LV04A devices contain six independent inverters. These devices perform the Boolean function  $Y = \overline{A}$ .

These devices are fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

T <sub>A</sub>	PACK	AGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Reel of 1000	SN74LV04ARGYR	LV04A
		Tube of 50	SN74LV04AD	11/044
	SOIC – D	Reel of 2500	SN74LV04ADR	LV04A
	SOP – NS	Reel of 2000	SN74LV04ANSR	74LV04A
–40°C to 85°C	SSOP – DB	Reel of 2000	SN74LV04ADBR	LV04A
		Tube of 90	SN74LV04APW	
	TSSOP – PW	Reel of 2000	SN74LV04APWR	LV04A
		Reel of 250	SN74LV04APWT	
	TVSOP – DGV	Reel of 2000	SN74LV04ADGVR	LV04A
	CDIP – J	Tube of 25	SNJ54LV04AJ	SNJ54LV04AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54LV04AW	SNJ54LV04AW
	LCCC – FK	Tube of 55	SNJ54LV04AFK	SNJ54LV04AFK

#### ORDERING INFORMATION

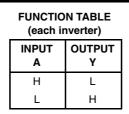
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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logic diagram, each inverter (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V <sub>O</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	
(see Note 3): DB package	
(see Note 3): DGV package	127°C/W
(see Note 3): NS package	
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 5.5 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

4. The package thermal impedance is calculated in accordance with JESD 51-5.



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			SN54L	V04A	SN74L	.V04A	
			MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
		$V_{CC} = 2 V$	1.5		1.5		
		$V_{CC}$ = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC}  imes 0.7$		
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		V
		$V_{CC}$ = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 2 V$		0.5		0.5	
.,		$V_{CC}$ = 2.3 V to 2.7 V		$V_{CC}  imes 0.3$		$V_{CC}  imes 0.3$	.,
V <sub>IL</sub>	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		$V_{CC}  imes 0.3$		$V_{CC}  imes 0.3$	v
		$V_{CC}$ = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC}  imes 0.3$	
VI	Input voltage		0	5.5	0	5.5	V
Vo	Output voltage		0	v <sub>cc</sub>	0	V <sub>CC</sub>	V
		$V_{CC} = 2 V$	20	-50		-50	μA
	I Bala Jacob Landari Alammani	$V_{CC}$ = 2.3 V to 2.7 V	20	-2		-2	
I <sub>OH</sub>	High-level output current	$V_{CC} = 3 V \text{ to } 3.6 V$	44	-6		-6	mA
		$V_{CC}$ = 4.5 V to 5.5 V		-12		-12	
		V <sub>CC</sub> = 2 V		50		50	μA
		$V_{CC}$ = 2.3 V to 2.7 V		2		2	
I <sub>OL</sub>	Low-level output current	$V_{CC} = 3 V \text{ to } 3.6 V$		6		6	mA
		$V_{CC}$ = 4.5 V to 5.5 V		12		12	
		$V_{CC}$ = 2.3 V to 2.7 V		200		200	
Δt/Δv	$t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 3 V \text{ to } 3.6 V$		100		100	ns/V
		$V_{CC}$ = 4.5 V to 5.5 V		20		20	
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

#### recommended operating conditions (see Note 5)

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER			SN54L	V04A	SN74LV	04A		
PARAMETER	TEST CONDITIONS	v <sub>cc</sub>	MIN	TYP MAX	MIN T	YP MAX	UNIT	
	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1			
N/	$I_{OH} = -2 \text{ mA}$	2.3 V	2		2		v	
V <sub>OH</sub>	$I_{OH} = -6 \text{ mA}$	3 V	2.48		2.48		v	
	I <sub>OH</sub> = -12 mA	4.5 V	3.8	W	3.8			
	I <sub>OL</sub> = 50 μA	2 V to 5.5 V		0.1		0.1		
	I <sub>OL</sub> = 2 mA	2.3 V	ć	0.4		0.4	- V	
V <sub>OL</sub>	I <sub>OL</sub> = 6 mA	3 V	5	0.44		0.44		
	I <sub>OL</sub> = 12 mA	4.5 V	nc	0.55		0.55		
l	$V_{I} = 5.5 V \text{ or GND}$	0 to 5.5 V	04	±1		±1	μA	
I <sub>CC</sub>	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	5.5 V	Q	20		20	μA	
l <sub>off</sub>	$V_1 \text{ or } V_0 = 0 \text{ to } 5.5 \text{ V}$	0		5		5	μA	
-		3.3 V		2.3	:	2.3	ъĘ	
Ci	$V_{I} = V_{CC}$ or GND	5 V		2.3		2.3	pF	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V  $\pm$  0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	Т	₄ = 25°C	;	SN54LV04A	SN74L	V04A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	ТҮР	MAX	MIN MAX	MIN	MAX	UNIT
t .	٨	v	C <sub>L</sub> = 15 pF		7.1*	11.7*	14*	1	14	
۲pd	A	T	C <sub>L</sub> = 50 pF		10	15.5	18	1	18	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

ĺ		FROM	то	LOAD	T,	<sub>A</sub> = 25°C		SN54LV04	4 <b>A</b>	SN74L	V04A	
	PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	МАХ	MINS	IAX	MIN	MAX	UNIT
	<b>t</b> .	~	v	C <sub>L</sub> = 15 pF		5.1*	7.1*	D* IFE	8.5*	1	8.5	20
	<sup>l</sup> pd	A	T	C <sub>L</sub> = 50 pF		7.3	10.6	\$`\$A`	12	1	12	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	₄ = 25°C	;	SN54LV04A	SN74L	V04A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
ter	٨	v	C <sub>L</sub> = 15 pF		3.6*	5.5*	① <sup>*</sup> 6.5*	1	6.5	
tpd	~	1	C <sub>L</sub> = 50 pF		5.1	7.5	8.5	1	8.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

### noise characteristics, $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 6)

		SN	Α		
	PARAMETER	MIN	ТҮР	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.3	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.1	-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		3.1		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.31			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V

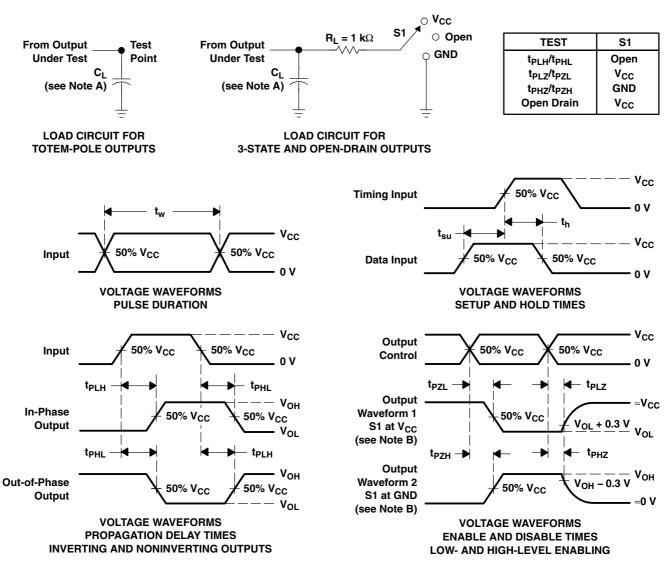
NOTE 6: Characteristics are for surface-mount packages only.

#### operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CO	V <sub>CC</sub>	TYP	UNIT	
<u> </u>	Power dissinction conscitutes	C = 50  pc	f = 10 MHz	3.3 V	9.6	рF
Upd	Power dissipation capacitance	C <sub>L</sub> = 50 pF,		5 V	11.4	μr



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#### PARAMETER MEASUREMENT INFORMATION

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{P7I}$  and  $t_{P7H}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

#### Figure 1. Load Circuit and Voltage Waveforms



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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV04AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LV04ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LV04APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV04APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

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RUMENTS

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	ackage Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74LV04ARGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LV04ARGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LV04A :

Automotive: SN74LV04A-Q1

Enhanced Product: SN74LV04A-EP

NOTE: Qualified Version Definitions:

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications

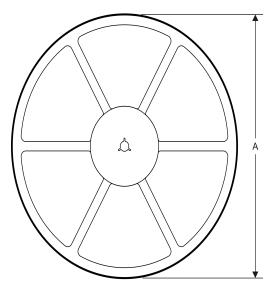
## PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION

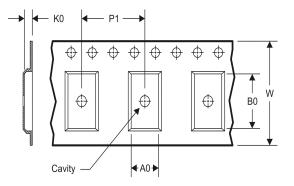
#### REEL DIMENSIONS

TEXAS INSTRUMENTS





#### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## TAPE AND REEL INFORMATION

\*All dimensions are nominal

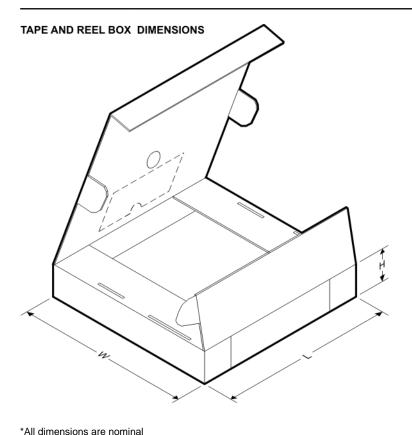
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV04ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV04ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV04ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV04APWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LV04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV04APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV04ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

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## PACKAGE MATERIALS INFORMATION

16-Dec-2011



All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV04ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LV04ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74LV04ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LV04ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LV04APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV04APWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74LV04APWT	TSSOP	PW	14	250	346.0	346.0	29.0
SN74LV04ARGYR	VQFN	RGY	14	3000	346.0	346.0	29.0

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

#### DGV (R-PDSO-G\*\*)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



## LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- earrow Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
- The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



## RGY (S-PVQFN-N14)

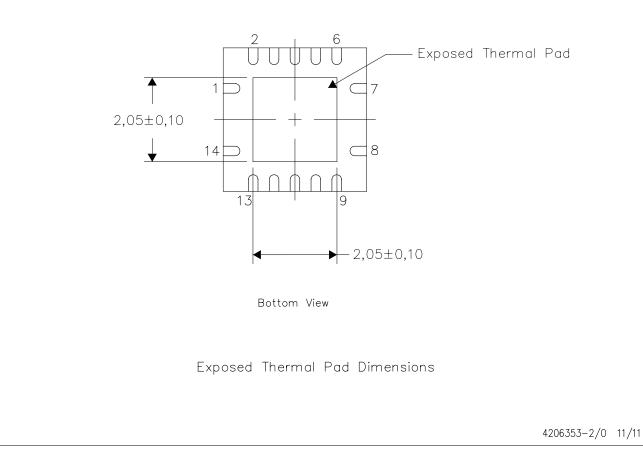
## PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

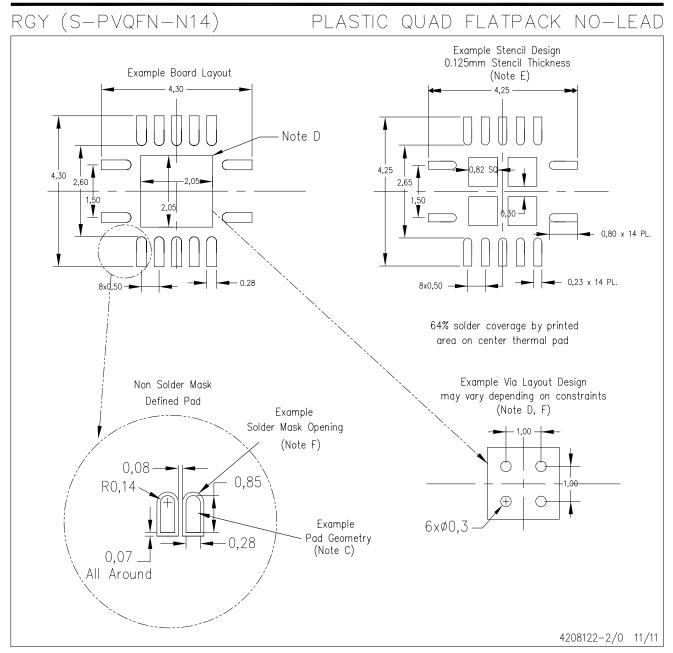
For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



#### NOTE: All linear dimensions are in millimeters





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="http://www.ti.com">http://www.ti.com</a>.

- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



#### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

## DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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