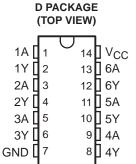
- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Low Power Consumption, 20-μA Max I_{CC}
- Typical t_{pd} = 13 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Inputs Are TTL-Voltage Compatible



description/ordering information

This device contains six independent inverters. It performs the Boolean function $Y = \overline{A}$ in positive logic.

ORDERING INFORMATION

TA	PACKAC	3E‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC - D	Reel of 2500	SN74HCT04IDREP	SHCT04IEP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SCLS561 - JANUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5	\mbox{V} to 7 \mbox{V}
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$ (see Note 1)		±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)		$\pm 20~\text{mA}$
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$		$\pm 25~\text{mA}$
Continuous current through V _{CC} or GND		$\pm 50~\text{mA}$
Package thermal impedance, θ_{JA} (see Note 2)		86°C/W
Storage temperature range, T _{stq}	–65°C t	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2			V
V _{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			0.8	V
VI	Input voltage		0		VCC	V
Vo	Output voltage		0		VCC	V
Δt/Δν	Input transition rise/fall time				500	ns
TA	Operating free-air temperature		-40		85	°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETO		T _A = 25°C			MIN	MAY		
PARAMETER	TEST CONDITION	VCC	MIN	TYP	MAX	IVIIN	MAX	UNIT	
V	Mr. Mr. andr.	$I_{OH} = -20 \mu A$	451/	4.4	4.499		4.4		
VOH	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.84		V
V	VI = VIH or VIL	I _{OL} = 20 μA	451/		0.001	0.1		0.1	V
VOL		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.33	
lį	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000	nA
ICC	$V_I = V_{CC}$ or 0,	IO = 0	5.5 V			2		20	μΑ
Δl _{CC} ‡	One input at 0.5 V or 2.4 V, Other in	puts at 0 or V _{CC}	5.5 V		1.4	2.4		2.9	mA
Ci			4.5 V to 5.5 V		3	10		10	pF

 $[\]ddagger$ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

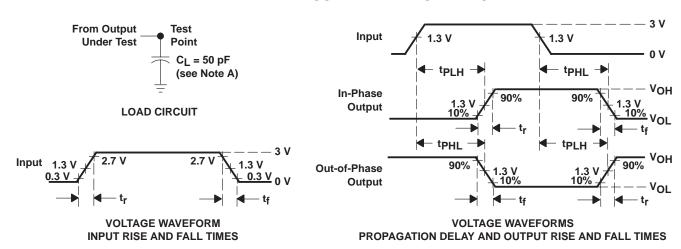
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	.,	T _A = 25°C				MAX	LINUT
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	WAX	UNIT
			4.5 V		14	20		25	
^t pd	А	Y	5.5 V		13	18		23	ns
		V	4.5 V		9	15		19	no
чt		ī	5.5 V		8	14		17	ns

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





ti.com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HCT04IDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04697-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74HCT04-EP:

Catalog: SN74HCT04

Automotive: SN74HCT04-Q1

• Military: SN54HCT04

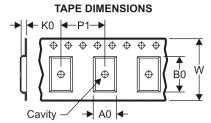
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





_		
	A0	Dimension designed to accommodate the component width
Γ	B0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

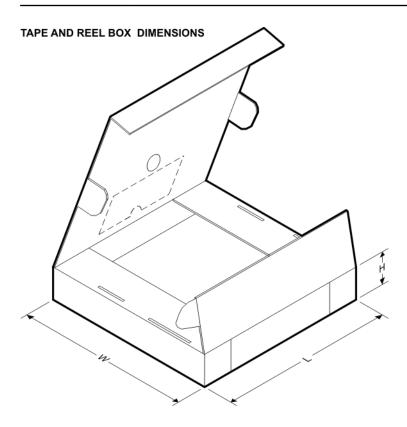
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT04IDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT04IDREP	SOIC	D	14	2500	333.2	345.9	28.6

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



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