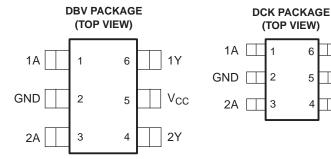
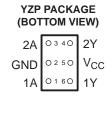


#### **FEATURES**

- Available in the Texas Instruments
  NanoFree™ Package
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Max t<sub>nd</sub> of 5.4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
  <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C

- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
  2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Feature Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)





See mechanical drawings for dimensions.

### **DESCRIPTION/ORDERING INFORMATION**

This dual Schmitt-trigger inverter is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The SN74LVC2G14 contains two inverters and performs the Boolean function  $Y = \overline{A}$ . The device functions as two independent inverters, but because of Schmitt action, it may have different input threshold levels for positive-going  $(V_{T+})$  and negative-going  $(V_{T-})$  signals.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC2G14YZPR	CF_	
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC2G14DBVR	C14	
–40°C to 85°C	SOT (SOT-23)	Reel of 250	SN74LVC2G14DBVT	C14_	
	COT (CC 70) DOV	Reel of 3000	SN74LVC2G14DCKR	OF.	
	SOT (SC-70) – DCK	Reel of 250	SN74LVC2G14DCKT	CF_	

<sup>(1)</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

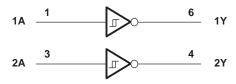
<sup>(2)</sup> DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



# FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
Н	L
L	Н

#### **LOGIC DIAGRAM (POSITIVE LOGIC)**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
$V_{CC}$	Supply voltage range		-0.5	6.5	V	
$V_{I}$	Input voltage range <sup>(2)</sup>	Input voltage range (2)				
Vo	Voltage range applied to any output in t	-0.5	6.5	V		
Vo	Voltage range applied to any output in t	he high or low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50		
Io	Continuous output current			±50	mA	
	Continuous current through V <sub>CC</sub> or GNE	)		±100	mA	
		DBV package		165		
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCK package		259	°C/W	
		YZP package		123		
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



### SN74LVC2G14 DUAL SCHMITT-TRIGGER INVERTER

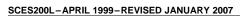
SCES200L-APRIL 1999-REVISED JANUARY 2007

## Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V	Cupply voltage	Operating	1.65	5.5	V
$V_{CC}$	Supply voltage	Data retention only	1.5		V
$V_{I}$	Input voltage		0	5.5	V
Vo	Output voltage		0	$V_{CC}$	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	mA
$I_{OH}$	High-level output current	V 2V		-16	
		$V_{CC} = 3 V$		-24	
		$V_{CC} = 4.5 \text{ V}$		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

### SN74LVC2G14 DUAL SCHMITT-TRIGGER INVERTER





### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup> MAX	UNIT		
		1.65 V	0.7	1.4			
V <sub>T+</sub>		2.3 V	1	1.7			
Positive-going input		3 V	1.3	2.2	V		
threshold voltage		4.5 V	1.9	3.1			
		5.5 V	2.2	3.7			
		1.65 V	0.3	0.7			
$V_{T-}$		2.3 V	0.4	1			
Negative-going input		3 V	0.6	1.3	V		
threshold voltage		4.5 V	1.1	2			
		5.5 V	1.4	2.5			
		1.65 V	0.3	0.8			
$\Delta V_T$		2.3 V	0.4	0.9			
Hysteresis		3 V	0.4	1.1	V		
$(\dot{V}_{T+} - V_{T-})$		4.5 V	0.6	1.3			
		5.5 V	0.7	1.4			
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 4.5 V	V <sub>CC</sub> - 0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
.,	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V		
V <sub>OH</sub>	I <sub>OH</sub> = -16 mA	3 V	2.4		V		
	I <sub>OH</sub> = -24 mA	3 V	2.3				
	I <sub>OH</sub> = -32 mA	4.5 V	3.8				
	I <sub>OL</sub> = 100 μA	1.65 V to 4.5 V		0.1			
	I <sub>OL</sub> = 4 mA	1.65 V		0.45			
.,	I <sub>OL</sub> = 8 mA	2.3 V		0.3	.,		
V <sub>OL</sub>	I <sub>OL</sub> = 16 mA	3 V		0.4	V		
	I <sub>OL</sub> = 24 mA	3 V		0.55			
	I <sub>OL</sub> = 32 mA	4.5 V		0.55			
I <sub>I</sub> A input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±5	μΑ		
I <sub>off</sub>	$V_1$ or $V_0 = 5.5 \text{ V}$	0		±10	μΑ		
I <sub>CC</sub>	$V_1 = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10	<u>.</u> μΑ		
$\Delta I_{CC}$	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V		500	<u>.</u> μΑ		
C <sub>I</sub>	$V_1 = V_{CC}$ or GND	3.3 V		4	pF		

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

### **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	3.9	9.5	1.9	5.7	2	5.4	1.5	4.3	ns



### SN74LVC2G14 DUAL SCHMITT-TRIGGER INVERTER

SCES200L-APRIL 1999-REVISED JANUARY 2007

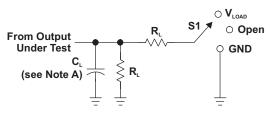
### **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 2.5 \text{ V} \qquad V_{CC} = 3.3 \text{ V}$		UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	16	17	18	21	pF	



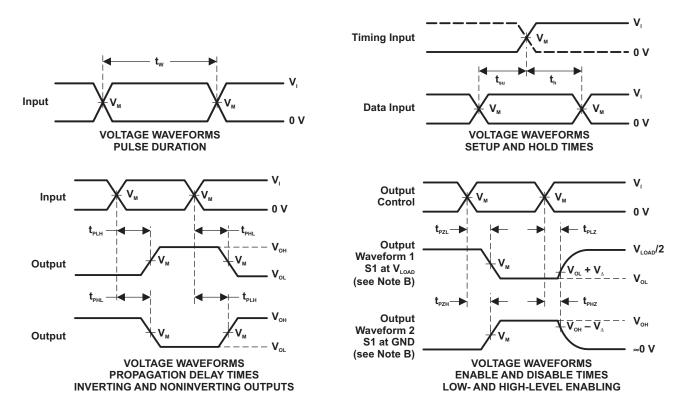
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

.,	INF	PUTS	V	V		Б	
V <sub>cc</sub>	V,	V <sub>I</sub> t <sub>r</sub> /t <sub>r</sub>		V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>o</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC2G14DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G14YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### **PACKAGE OPTION ADDENDUM**

5-Dec-2008

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVC2G14:

Automotive: SN74LVC2G14-Q1

NOTE: Qualified Version Definitions:

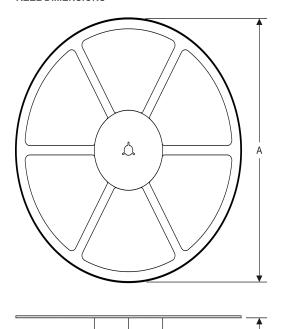
• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

### PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

#### \*All dimensions are nominal

^All dimensions are nominal	T	I	I		T	I						
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G14DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC2G14DBVR	SOT-23	DBV	6	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC2G14DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2G14DBVT	SOT-23	DBV	6	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC2G14DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC2G14DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC2G14DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2G14DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC2G14DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2G14DCKT	SC70	DCK	6	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC2G14YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G14DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2G14DBVR	SOT-23	DBV	6	3000	205.0	200.0	33.0
SN74LVC2G14DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2G14DBVT	SOT-23	DBV	6	250	205.0	200.0	33.0
SN74LVC2G14DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC2G14DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC2G14DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC2G14DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC2G14DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC2G14DCKT	SC70	DCK	6	250	205.0	200.0	33.0
SN74LVC2G14YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

## DBV (R-PDSO-G6)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



## DBV (R-PDSO-G6)

### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



## DCK (R-PDSO-G6)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



## DCK (R-PDSO-G6)

### PLASTIC SMALL OUTLINE



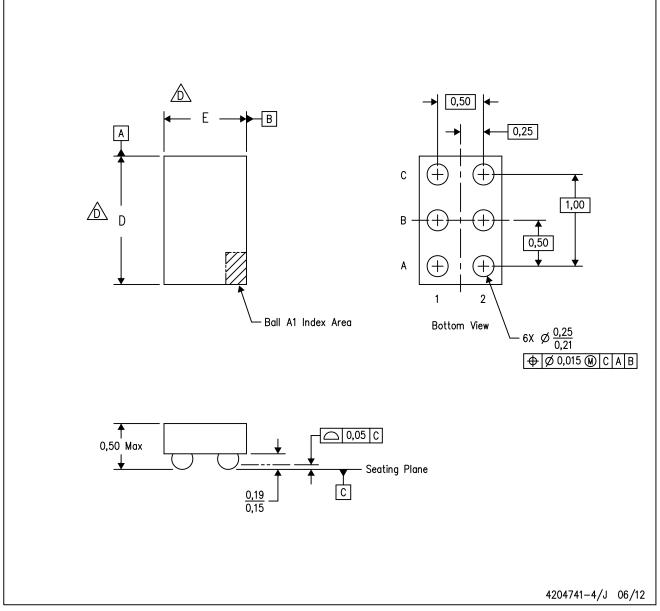
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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