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RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

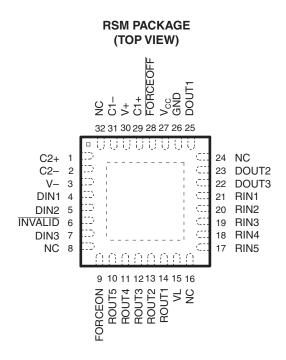
Check for Samples: TRS3253E

FEATURES

- V_L Pin for Compatibility With Mixed-Voltage Systems Down to 1.8 V on Logic Side
- Enhanced ESD Protection on RIN Inputs and DOUT Outputs
 - ±8 kV IEC 61000-4-2 Air-Gap Discharge
 - ±8 kV IEC 61000-4-2 Contact Discharge
 - ±15 kV Human-Body Model
- Low 300-µA Supply Current
- Specified 1000-kbps Data Rate
- Auto Powerdown Plus Feature

APPLICATIONS

- Hand-Held Equipment
- PDAs
- Cell Phones
- Battery-Powered Equipment
- Data Cables



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The TRS3253E is a three-driver and five-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ±8 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human-Body Model.

The charge pump requires only four small 0.1-µF capacitors for operation from a 3.3-V supply. The TRS3253E is capable of running at data rates up to 1000 kbps, while maintaining RS-232-compliant output levels.

The TRS3253E has a unique V_L pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the V_L pin. This eliminates the need for additional voltage level shifter while interfacing with low-voltage microcontroller or UARTs. The TRS3253E is available in a space-saving QFN package (4 mm × 4 mm RSM).

Auto-powerdown plus can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown plus enabled, the device activates automatically when a valid signal is applied to any receiver or driver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 5 for receiver input levels.

ORDERING INFORMATION

0.152.11.10.11.01.11.01.1								
T _A	PACKAGE ⁽¹⁾ (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING					
-40°C to 85°C	QFN - RSM	TRS3253EIRSMR	RS53EI					

⁽¹⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

⁽²⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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FUNCTION TABLES

Each Driver⁽¹⁾

		INPUTS		OUTPUT							
DIN	FORCEON	FORCEOFF	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	DOUT	DRIVER STATUS						
Х	Х	L	X	Z	Powered off						
L	Н	Н	X	Н	Normal operation with						
Н	Н	Н	X	L	auto-powerdown plus disabled						
L	L	Н	<30 s	Н	Normal operation with						
Н	L	Н	<30 s	L	auto-powerdown plus enabled						
L	L	Н	>30 s	Z	Powered off by						
Н	L	Н	>30 s	Z	auto-powerdown plus feature						

⁽¹⁾ H = high level, L = low level, X = irrelevant, Z = high impedance

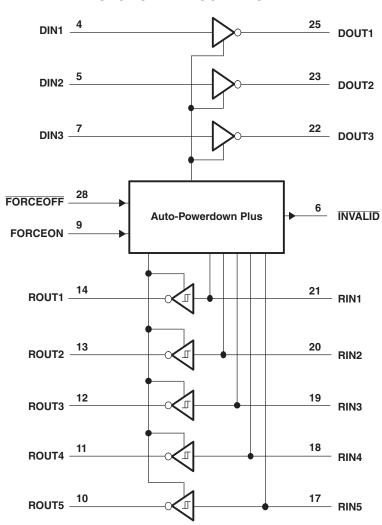
Each Receiver⁽¹⁾

	INPUTS			INPUTS OUTPUTS			
RIN1-RIN5	FORCEOFF	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1-ROUT5	RECEIVER STATUS			
X	L	X	Z	Powered off			
L	Н	<30 s	Н	Normal operation with			
Н	Н	<30 s	L	auto-powerdown plus			
Open	Н	<30 s	Н	disabled/enabled			

⁽¹⁾ H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off



FUNCTIONAL BLOCK DIAGRAM





TERMINAL FUNCTIONS

TERMI	INAL	DESCRIPTION			
NAME	RSM	DESCRIPTION			
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge-pump capacitor			
V+	30	5.5-V supply generated by the charge pump			
C1-, C2-	31, 2	Negative terminal of the voltage-doubler charge-pump capacitor			
INVALID	6	Invalid Output Pin			
V-	3	-5.5-V supply generated by the charge pump			
DIN1 DIN2 DIN3	4 5 7	Driver inputs			
ROUT5 - ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and V _L .			
V_L	15	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.			
RIN5-RIN1	17, 18, 19, 20, 21	RS-232 receiver inputs			
DOUT3 DOUT2 DOUT1	22 23 25	RS-232 driver outputs			
GND	26	Ground			
V _{CC}	27	3-V to 5.5-V supply voltage			
FORCEOFF	28	Powerdown Control input (Refer to Truth Table)			
FORCEON	9	Powerdown Control input (Refer to Truth Table)			

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	V _{CC} to GND		-0.3	6	V
	V _L to GND		-0.3	V _{CC} + 0.3	V
	V+ to GND		-0.3	7	V
	V- to GND		0.3	-7	V
	V+ + V- ⁽²⁾			13	V
·	Land and the ma	DIN, FORCEOFF to GND, FORCEON to GND	-0.3	6	V
VI	Input voltage	RIN to GND		±25	V
V	Output valtage	DOUT to GND		±13.2	V
Vo	Output voltage	ROUT	-0.3	$V_{L} + 0.3$	V
	Continuous power dissipation	T _A = 70°C, 32-pin RSM (derate 7 mW/°C above 70°C)		TBD	mW
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V+ and V- can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

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RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V _{CC}	Supply voltage			3	5.5	V
VL	Supply voltage			1.65	V _{CC}	V
	Input logic threshold low		$V_L = 3 \text{ V or } 5.5 \text{ V}$		8.0	
		DIN, FORCEOFF, FORCEON	V _L = 2.3 V		0.6	V
			V _L = 1.65 V		0.5	
			$V_{L} = 5.5 \text{ V}$	2.4		
	lanut lagia throobald high	DIN, FORCEOFF, FORCEON	$V_L = 3 V$	2.0		V
	Input logic threshold high	DIN, FORCEOFF, FORCEON	$V_{L} = 2.7 \text{ V}$	1.4		V
			V _L = 1.95 V	1.25		
	Operating temperature	TRS3253EIRSMR	-40	85	°C	
	Receiver input voltage			-25	25	V

ELECTRICAL CHARACTERISTICS(1)

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V \pm 10%), C1 = 0.047 μF , $C2-C4 = 0.33 \mu F$ (tested at 5 V ± 10%) (unless otherwise noted)

	PARAI	METER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I	Input leakage current	FORCEOFF, FORCEON			±0.01	±1	μΑ
		Auto-powerdown plus disabled	No load, FORCEOFF and FORCEON at V _{CC}		0.5	1	mA
loo	Supply current	Powered off	No load, FORCEOFF at GND		1	10	
I _{CC}	$(T_A = 25^{\circ}C)$ Auto	Auto-powerdown plus enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded		1	10	μΑ

Testing supply conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.15 V; C1–C4 = 0.22 μ F at V_{CC} = 3.3 V \pm 0.3 V; and C1 = 0.047 μ F and C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
	Human-Body Model	±15	
RIN, DOUT	IEC 61000-4-2 Air-Gap Discharge	±8	kV
	IEC 61000-4-2 Contact Discharge	±8	

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RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range, $V_{CC} = V_L = 3 \text{ V}$ to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V \pm 10%), C1 = 0.047 μF , C2–C4 = 0.33 μF (tested at 5 V \pm 10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST (CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{off}	Output leakage current	ROUT, receivers disab	oled		±0.05	±10	μΑ
V _{OL}	Output voltage low	I _{OUT} = 1.6 mA				0.4	V
V_{OH}	Output voltage high	$I_{OUT} = -1 \text{ mA}$		V _L - 0.6	$V_{L} - 0.1$		V
V	Input threshold low	Input threshold low T = 25°C	V _L = 5 V	0.8	1.2		V
V _{IT}		T _A = 25°C	$V_{L} = 3.3 \text{ V}$	0.6	1.5		V
V	Input throubold high	T 250C	V _L = 5 V		1.8	2.4	V
V _{IT+}	Input threshold high	1A = 25 C	$T_A = 25^{\circ}C$ $V_L = 3.3 \text{ V}$		1.5	2.4	V
V_{hys}	Input hysteresis				0.5		V
	Input resistance	T _A = 25°C		3	5	7	kΩ

⁽¹⁾ Typical values are at $V_{CC} = V_L = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

Switching Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μ F (tested at 3.3 V ± 10%), C1 = 0.047 μ F, C2–C4 = 0.33 μ F (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t _{PHL}	Receiver propagation delay	Receiver input to receiver output, C _L = 150 pF		ПС
t _{PLH}	Receiver propagation delay			μs
t _{PHL} – t _{PLH}	Receiver skew		50	ns
t _{en}	Receiver output enable time	From FORCEOFF	200	ns
t _{dis}	Receiver output disable time	From FORCEOFF	200	ns

⁽¹⁾ Typical values are at $V_{CC} = V_L = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



DRIVER SECTION

Electrical Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μ F (tested at 3.3 V \pm 10%), C1 = 0.047 μ F, C2–C4 = 0.33 μ F (tested at 5 V \pm 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	Output voltage swing	All driver outputs loaded with 3 k Ω to ground, V _{CC} = 3.1V to 5.5V	±5	±5.4		V
r _O	Output resistance	$V_{CC} = V + = V - = 0$, Driver output = ±2 V	300	10M		Ω
Ios	Output short-circuit current	$V_{T_OUT} = 0$			±60	mA
	Output leakage augrapt	$V_{T_OUT} = \pm 12 \text{ V}, \overline{\text{FORCEOFF}} = \text{GND},$ $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$			±60 ±25	
I _{OZ}	Output leakage current	$V_{T_OUT} = \pm 12 \text{ V}, \overline{\text{FORCEOFF}} = \text{GND},$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			±23	μΑ
	Driver input hysteresis				0.5	V
	Input leakage current	DIN, FORCEOFF, FORCEON		±0.01	±1	μΑ

⁽¹⁾ Typical values are at $V_{CC} = V_L = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

Timing Requirements

over operating free-air temperature range, $V_{CC} = V_L = 3 \text{ V}$ to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V \pm 10%), C1 = 0.047 μF , C2–C4 = 0.33 μF (tested at 5 V \pm 10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

	PARAMETER			MIN	TYP ⁽¹⁾	MAX	UNIT
	Maximum data rate	$R_L = 3 \text{ k}\Omega$, $C_L = 200 \text{ pF}$, Or	$R_L = 3 \text{ k}\Omega$, $C_L = 200 \text{ pF}$, One driver switching				kbps
	Time-to-exit powerdown	V _{T_OUT} > 3.7 V			100		μs
t _{PHL} - t _{PLH}	Driver skew ⁽²⁾						ns
	Transition-region slew rate	$\begin{split} &V_{CC}=3.3~\text{V},\\ &T_{A}=25^{\circ}\text{C},\\ &R_{L}=3~\text{k}\Omega~\text{to 7 k}\Omega,\\ &\text{Measured from 3 V}\\ &\text{to } -3~\text{V or } -3~\text{V to 3 V} \end{split}$	C _L = 150 pF to 1000 pF	15		150	V/µs

⁽¹⁾ Typical values are at $V_{CC} = V_L = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

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⁽²⁾ Driver skew is measured at the driver zero crosspoint.



AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{IT+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _L		2.7	V
V _{IT-(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _L	-2.7		V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _L	-0.3	0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _L	V _L - 0.6		V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _L		0.4	V

Switching Characteristics

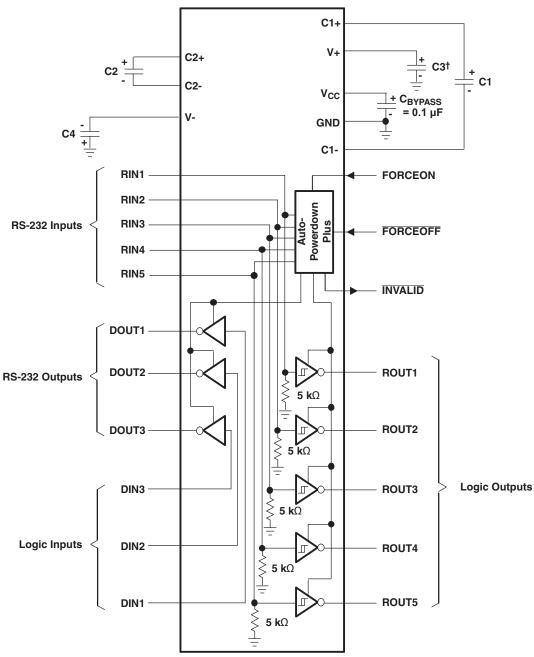
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{valid}	Propagation delay time, low- to high-level output		0.1		μs
t _{invalid}	Propagation delay time, high- to low-level output		50		μs
t _{en}	Supply enable time		25		μs
t _{dis}	Receiver or driver edge to auto-powerdown plus	15	30	60	S

⁽¹⁾ All typical values are at V_{CC} = V_L = 3.3 V and TA = 25°C.



APPLICATION INFORMATION



 $^{^{\}dagger}$ C3 can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4			
3.3 V \pm 0.3 V 5 V \pm 0.5 V 3 V to 5.5 V	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF			

Figure 1. Typical Operating Circuit and Capacitor Values



PARAMETER MEASUREMENT INFORMATION

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

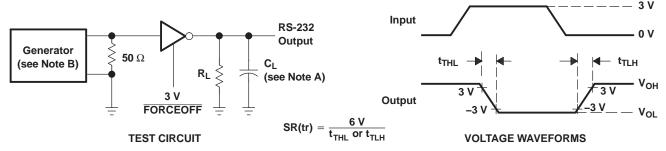


Figure 2. Driver Slew Rate

- C. C_L includes probe and jig capacitance.
- D. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω , 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

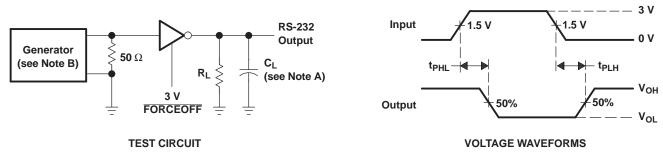


Figure 3. Driver Pulse Skew

- E. C_L includes probe and jig capacitance.
- F. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns. $t_f \le 10$ ns.

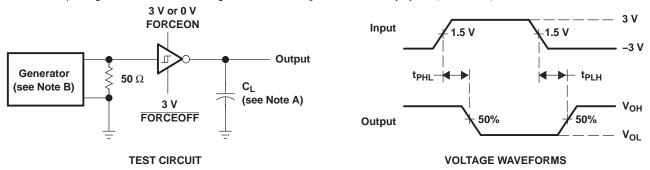


Figure 4. Receiver Propagation Delay Times

- G. C_L includes probe and jig capacitance.
- H. The pulse generator has the following characteristics: $Z_O = 50 \ \Omega$, 50% duty cycle, $t_r \le 10 \ ns$, $t_f \le 10 \ ns$.
- I. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- J. t_{PZL} and t_{PZH} are the same as t_{en} .



PARAMETER MEASUREMENT INFORMATION (continued)

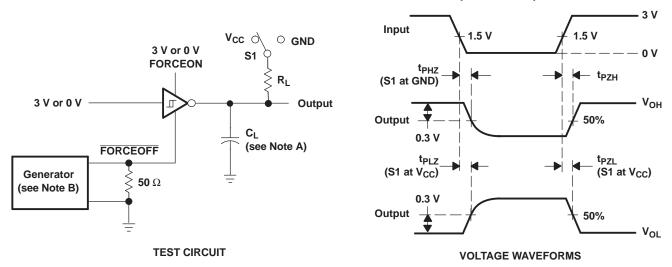
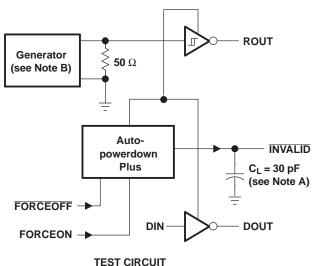


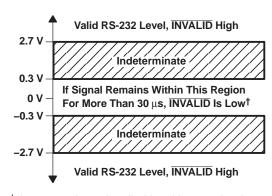
Figure 5. Receiver Enable and Disable Times

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PARAMETER MEASUREMENT INFORMATION (continued)





 † Auto-powerdown plus disables drivers and reduces supply current to 1 $\mu A.$

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω , 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

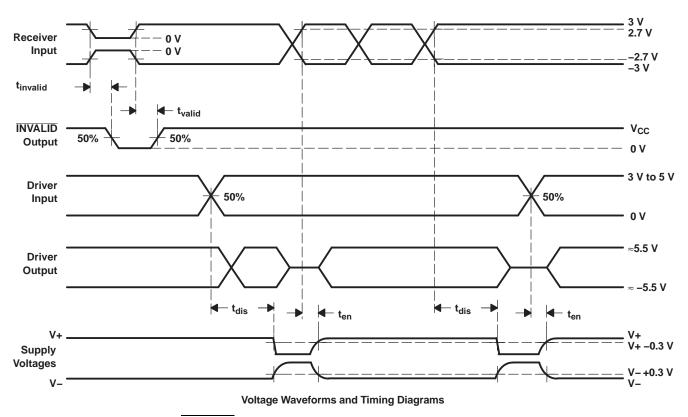


Figure 6. INVALID Propagation-Delay Times and Supply-Enabling Time



PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins P	ackage Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TRS3253EIRSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

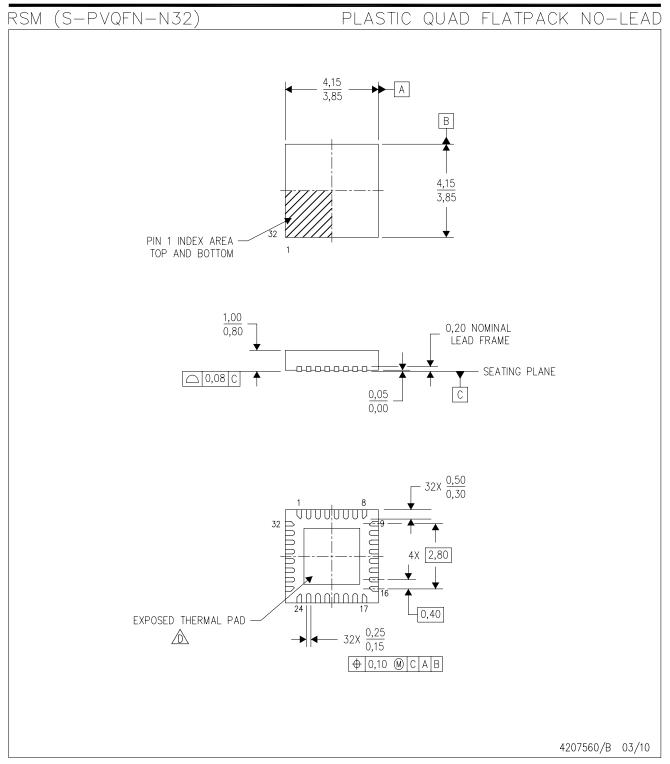
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

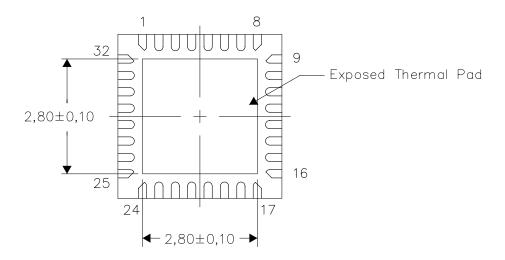


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



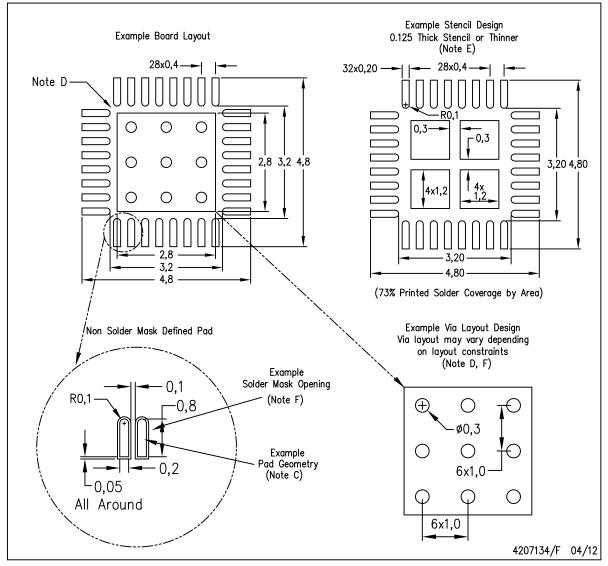
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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