CD4504B Types

TERMINAL ASSIGNMENT

```
         TOP VIEW
   Vcc   1      16  VDD
   AOUT   2      15  FOUT
   AIN    3      14  FIN
   BOUT   4      13  SELECT
   BIN    5      12  EOUT
   COUT   6      11  EIN
   CIN    7      10  DOUT
   VSS    8       9  DIN
```

92CS-39308

CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

High-Voltage Types (20-Volt Rating)

Features:
- Independence of power-supply sequence considerations–V_{CC} can exceed V_{DD}; input signals can exceed both V_{CC} and V_{DD}
- Up and down level-shifting capability
- Shiftable input threshold for either CMOS or TTL compatibility
- Standardized symmetrical output characteristics
- 100% tested for quiescent current @ 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the V_{CC} logic level to the V_{DD} logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the V_{CC} HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and MT suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).


*ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

V_{CC} = PIN 1
V_{DD} = PIN 16
V_{SS} = PIN 8

92CS-39309
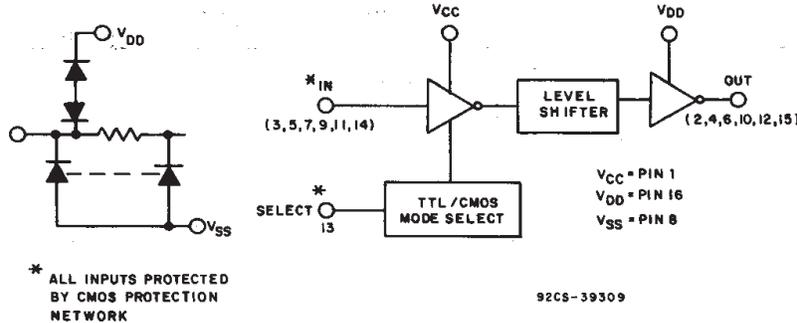
Fig. 1 - Functional diagram for CD4504B.

MAXIMUM RATINGS, *Absolute–Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR -
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING–TEMPERATURE RANGE (T_A) .... –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

V_{GEN}

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
		V_O (V)	V_{IN} (V)	V_{CC} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 MIN	+25 TYP	+25 MAX	
Quiescent Device Current, I_{DD} Max and I_{CC} in CMOS-CMOS Mode		—	0, 5	5	5	1.5	1.5	1.5	1.5	—	0.02	1.5	mA
		—	0, 10	5	10	2	2	2	2	—	0.02	2	
		—	0, 15	5	15	4	4	120	120	—	0.02	4	μA
		—	0, 20	5	20	20	20	600	600	—	0.04	20	
Quiescent Device Current, I_{CC} Max TTL-CMOS Mode		—	0, 5	5	5	5	5	6	6	—	2.5	5	
		—	0, 10	5	10	5	5	6	6	—	2.5	5	mA
		—	0, 15	5	15	5	5	6	6	—	2.5	5	
Output Low (Sink) Current, I_{OL} Min		0.4	0.5	—	5	0.64	0.61	0.42	0.36	0.51	1	—	
		0.5	0, 10	—	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
		1.5	0, 15	—	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min		4.6	0, 5	—	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	mA
		2.5	0, 5	—	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
		9.5	0, 10	—	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
		13.5	0, 15	—	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max		—	0, 5	—	5	0.05				—	0	0.05	
		—	0, 10	—	10	0.05				—	0	0.05	
		—	0, 15	—	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min		—	0, 5	—	5	4.95				4.95	5	—	
		—	0, 10	—	10	9.95				9.95	10	—	
		—	0, 15	—	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max Note 1	TTL-CMOS	1	—	5	10	0.8				—	—	0.8	
	TTL-CMOS	1	—	5	15	0.8				—	—	0.8	V
	CMOS-CMOS	1	—	5	10	1.5				—	—	1.5	
	CMOS-CMOS	1.5	—	5	15	1.5				—	—	1.5	
	CMOS-CMOS	1.5	—	10	15	3				—	—	3	
Input High Voltage, V_{IH} Min Note 1	TTL-CMOS	9	—	5	10	2				2	—	—	
	TTL-CMOS	13.5	—	5	15	2				2	—	—	
	CMOS-CMOS	9	—	5	10	3.5				3.5	—	—	
	CMOS-CMOS	13.5	—	5	15	3.5				3.5	—	—	
	CMOS-CMOS	13.5	—	10	15	7				7	—	—	
Input Current, I_{IN} Max		—	0, 18	—	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

Note 1: Applies to the 6 input signals. For mode control (P13), only the CMOS-CMOS ratings apply.
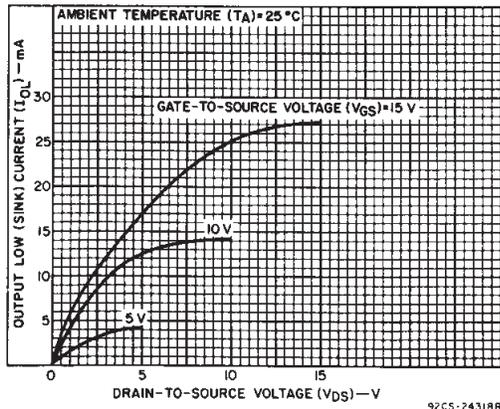

Fig. 2 - Typical output low (sink) current characteristics.
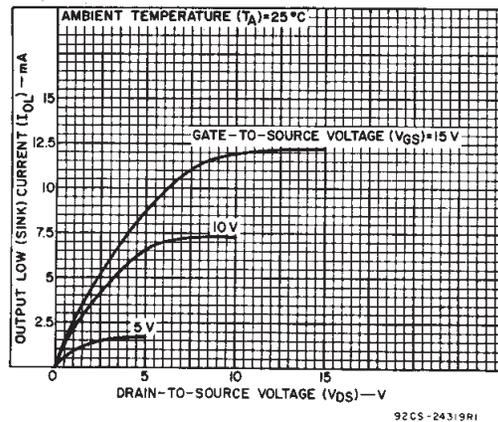
Fig. 3 - Minimum output low (sink) current characteristics.
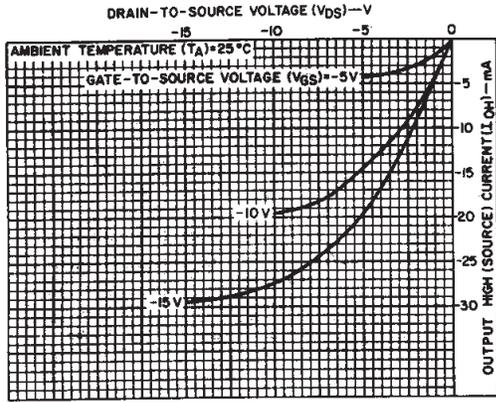
Fig. 4 - Typical output high (source) current characteristics.
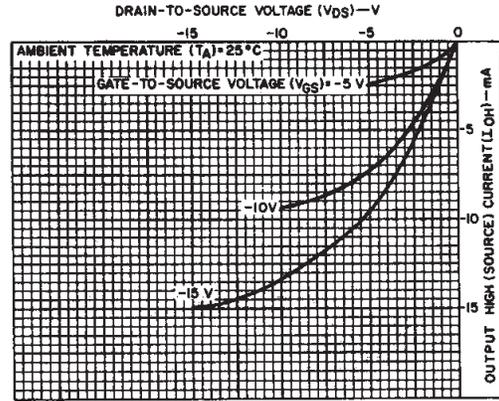
Fig. 5 - Minimum output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	5	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 Ω

CHARACTERISTIC		SHIFTING MODE	VCC (V)	VDD (V)	LIMITS		UNITS
					TYP.	MAX.	
Propagation Delay: High-to Low,	t_{PHL}	TTL to CMOS $V_{DD} > V_{CC}$	5	10	140	280	ns
			5	15	140	280	
		CMOS to CMOS $V_{DD} > V_{CC}$	5	10	120	240	
			5	15	120	240	
			10	15	70	140	
		CMOS to CMOS $V_{CC} > V_{DD}$	10	5	275	550	
			15	5	275	550	
			15	10	70	140	
Low-to-High,	t_{PLH}	TTL to CMOS $V_{DD} > V_{CC}$	5	10	140	280	
			5	15	140	280	
		CMOS to CMOS $V_{DD} > V_{CC}$	5	10	120	240	
			5	15	120	240	
			10	15	70	140	
		CMOS to CMOS $V_{CC} > V_{DD}$	10	5	200	400	
			15	5	200	400	
			15	10	60	120	
Transition Time,	t_{THL}, t_{TLH}	All Modes		5	100	200	
				10	50	100	
				15	40	80	
Input Capacitance,	C_{IN}	Any Input			5	7.5	pF

Fig. 6 - Quiescent device current.

NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{CC} OR V_{SS}.
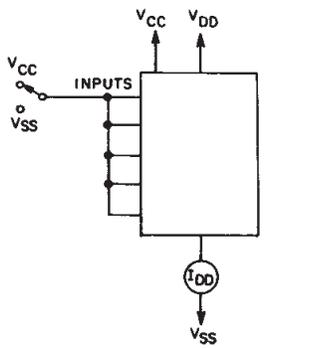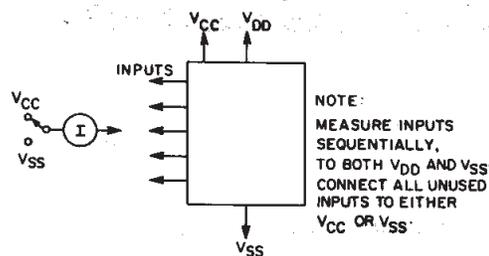
Fig. 7 - Input current.

NOTE:
TEST ANY COMBINATION OF INPUTS

Fig. 8 - Input voltage.
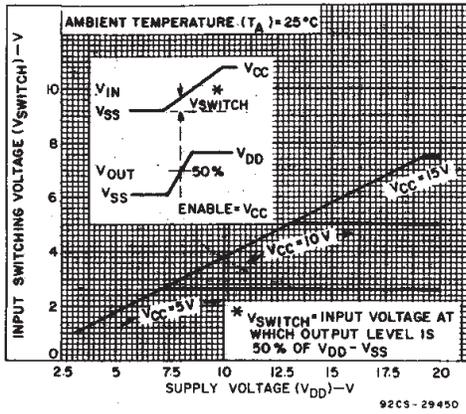
Fig. 9 - Typical input switching as a function of high-level supply voltage. (SELECT at V_{CC}-CMOS mode).
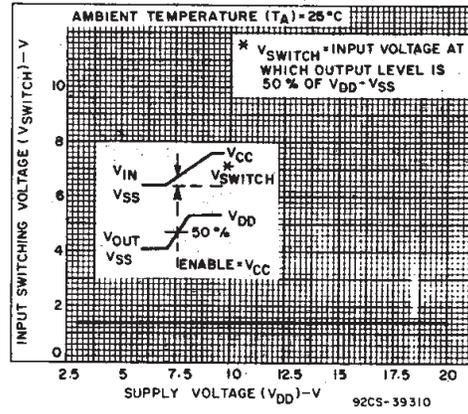

Fig. 10 - Typical input switching as a function of high-level supply voltage (SELECT at V_{SS}-TTL mode).
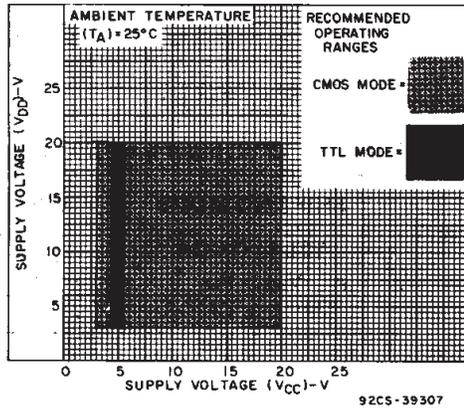

Fig. 11 - High-level supply voltage vs. low-level supply voltage.
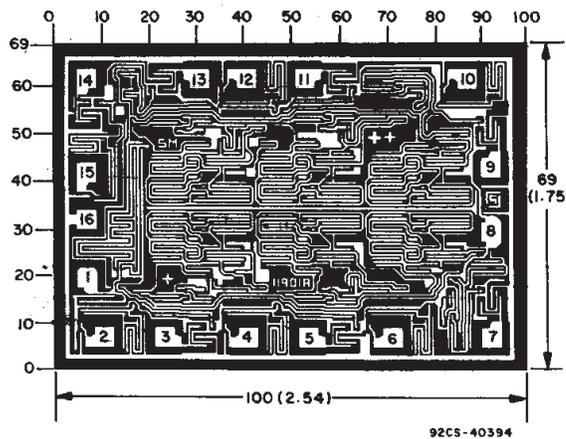
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4504BH.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
CD4504BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD4504BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD4504BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD4504BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4504BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD4504B, CD4504B-MIL :

● Catalog: CD4504B

● Enhanced Product: CD4504B-EP, CD4504B-EP

● Military: CD4504B-MIL

NOTE: Qualified Version Definitions:

 ● Catalog - TI's standard catalog product

 ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
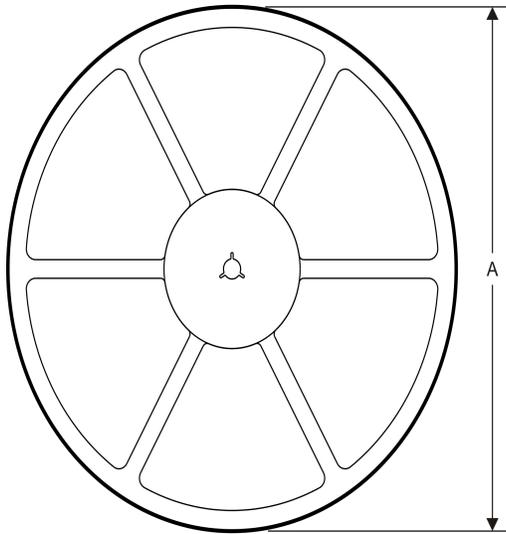
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Cavity

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4504BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4504BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
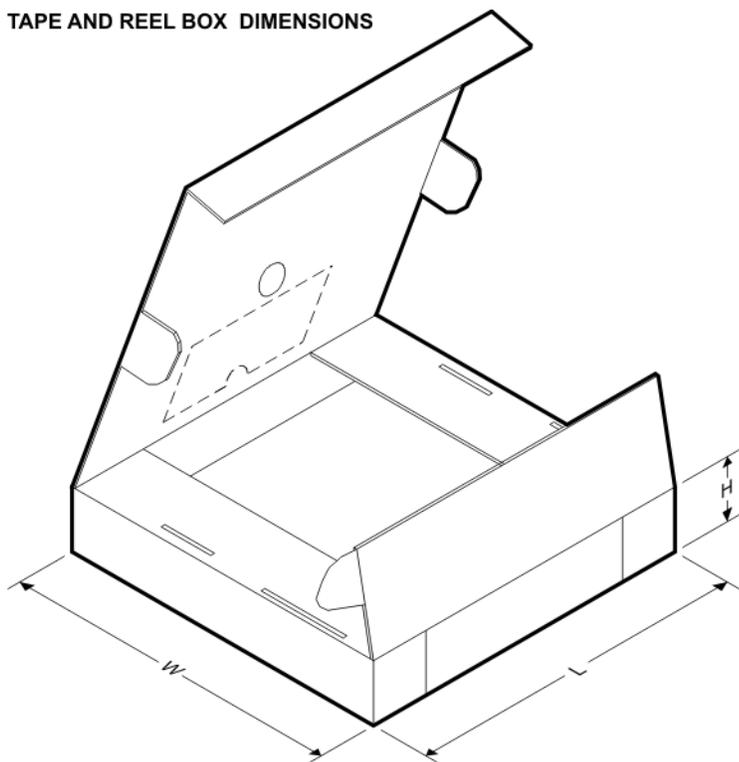
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4504BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4504BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
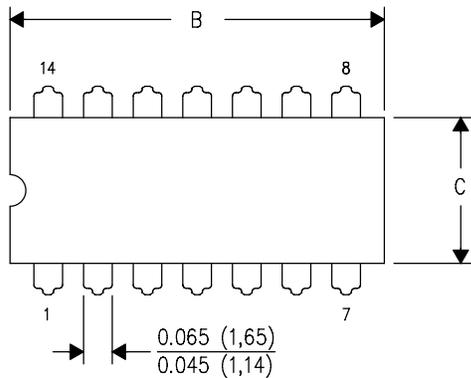
	PINS **	14	16	18	20
DIM					
A		0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX		0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN		—	—	—	—
C MAX		0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN		0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

C

1   7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package is hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
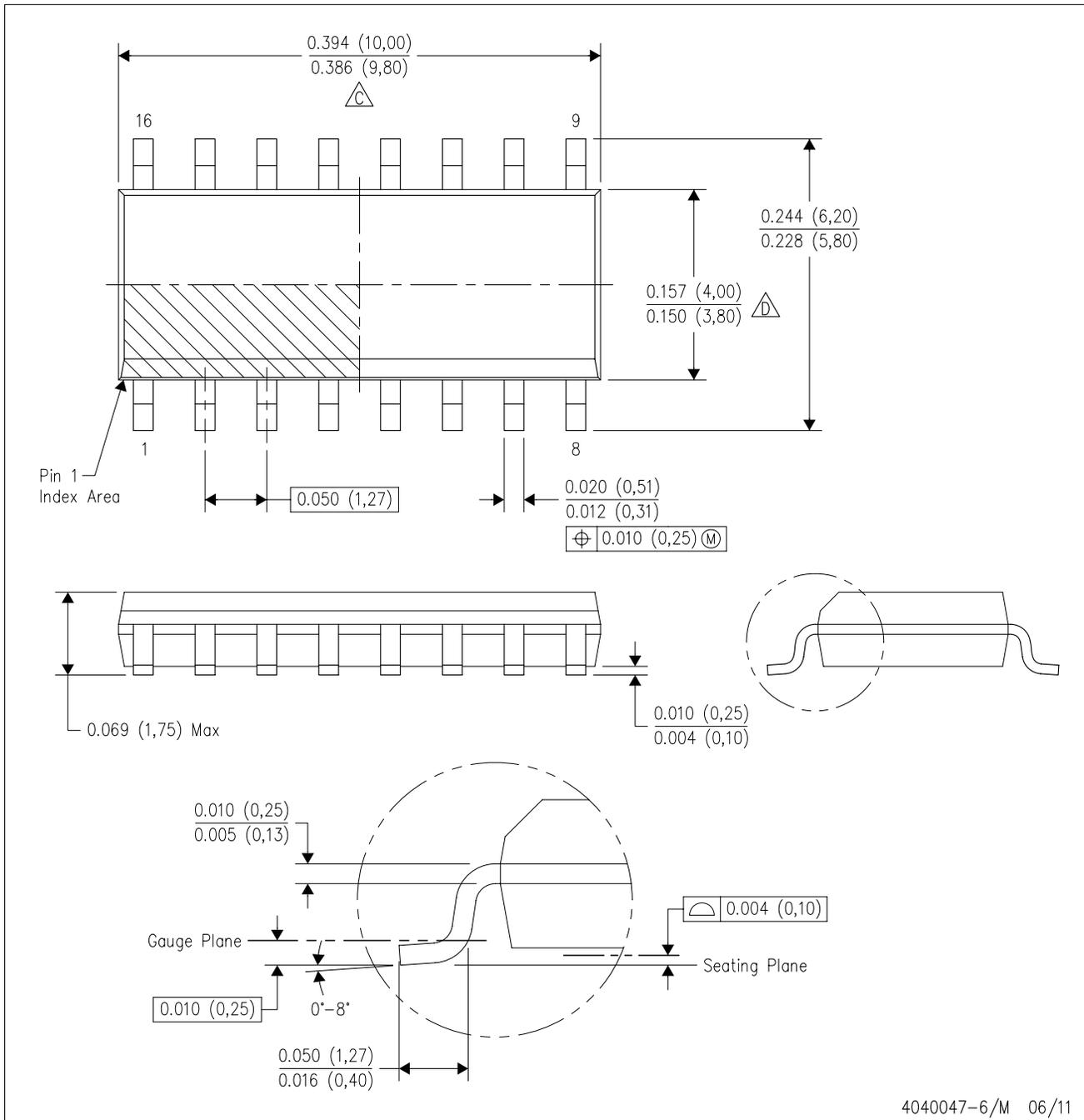
0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          ⚠C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
          ⚠D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AC.
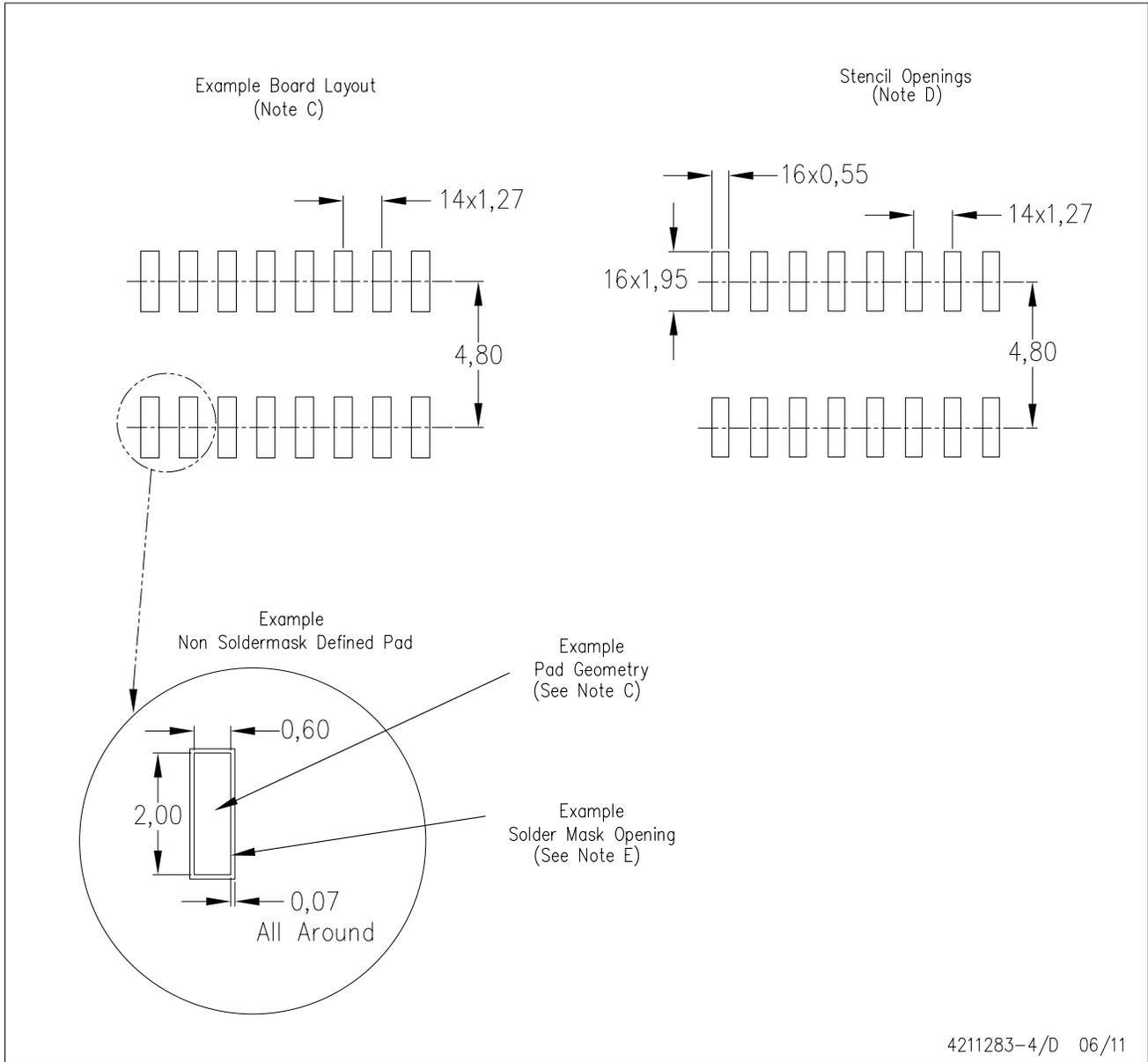
TEXAS
INSTRUMENTS
www.ti.com

D (R–PDSO–G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←─ 14x1,27

16x0,55

←─ 14x1,27

16x1,95

4,80

4,80

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

2,00

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211283–4/D   06/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC–7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

△D 4,50
    4,30

6,60
6,20

1   8

5,10
4,90

△C

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10
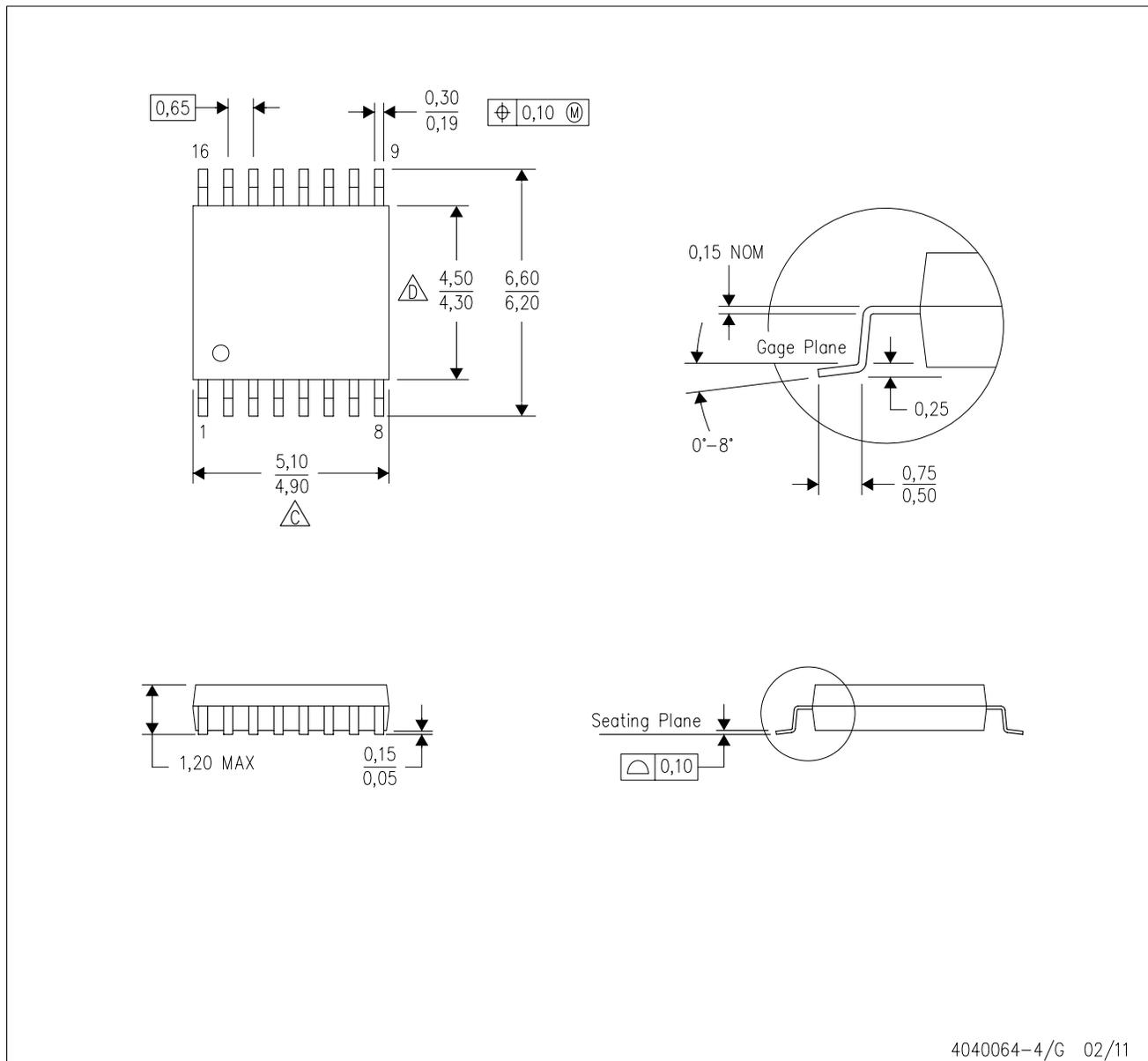
4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
          △D   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←14x0,65→

5,60

Stencil Openings
(Note D)

←16x0,30→

←14x0,65→

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284−3/D   05/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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