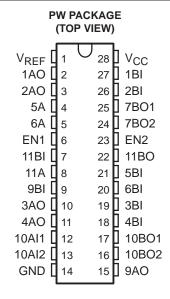
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- Operates as a GTL-/GTL/GTL+ to LVTTL or LVTTL to GTL-/GTL/GTL+ Translator
- Series Termination on TTL Outputs of 30 Ω
- Latch-Up Testing Done to JEDEC Standard JESD 78
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

The SN74GTL2007 is a 12-bit translator to interface between the 3.3-V LVTTL chip set I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The device is designed for platform health management in dual-processor applications.



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	VREF	GTL reference voltage
2-6, 8, 10-13, 15, 23	ENn nAn	Data and enable inputs/outputs (LVTTL)
7, 9, 16, 17–22, 24–27	nBn	Data inputs/outputs (GTL-/GTL/GTL+)
14	GND	Ground (0 V)
28	VCC	Positive supply voltage

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – PW	Tube	SN74GTL2007PW	GK2007
-40 C 10 65 C	1330F - FW	Tape and reel	SN74GTL2007PWR	GNZ007

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Function Tables

INF	PUTS	OUTPUT
EN1	1BI/2BI	1AO/2AO
Н	L	L
Н	Н	Н
L	X	Н

INF	PUTS	OUTPUT
EN2	3BI/4BI	3AO/4AO
Н	L	L
Н	Н	Н
L	X	Н

INPUT 9BI	OUTPUT 9AO
L	L
Н	Н

INPUTS	OUTPUT	
10AI1/10AI2	9BI	10BO1/10BO2
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

		INIDIJE/GUEDUE	
INPUTS		INPUT/OUTPUT 5A/6A	OUTPUT
EN2	5BI/6BI	(OPEN DRAIN)	7BO1/7BO2
Н	L	L	H [†]
Н	Н	L‡	L
Н	Н	Н	Н
L	Н	L‡	L
L	Н	Н	Н
L	L	Н	Н
L	L	L‡	Н

INPUT 11BI	INPUT/OUTPUT 11A (OPEN DRAIN)	OUTPUT 11BO
L	Н	L
L	L‡	Н
Н	L	Н

H = High voltage level

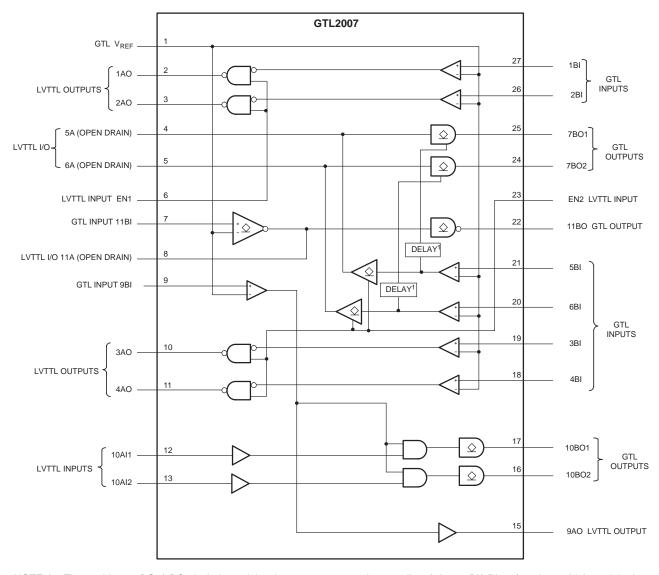
L = Low voltage level

[‡] Open-drain input/output terminal is driven to a logic-low state by an external driver.



[†]The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (where 5BI/6BI goes from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

logic symbol



NOTE A: The enable on 7BO1/7BO2 includes a delay that prevents a transient conditon (where 5BI/6BI go from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

–0.5 to 4.6 V
–0.5 to 4.6 V
–50 mA
–50 mA
32 mA
30 mA
–32 mA
62°C/W
–60 to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The performance capability of a high-performance integrated circuit, in conjunction with its thermal environment, can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		3	3.3	3.6	٧
		GTL-	0.85	0.9	0.95	
VTT	Termination voltage	GTL	1.14	1.2	1.26	V
	-	GTL+	1.35	1.5	1.65	1
		Overall	0.5	2/3 V _{TT}	1.8	
V _{REF}	Reference voltage	GTL-	0.5	0.6	0.63] ,
		GTL	0.76	0.8	0.84	٧
		GTL+	0.87	1	1.1	1
	Input voltage	A port	0	3.3	3.6	.,
VI		B port	0	V _{TT}	3.6	V
		A port	2			V
VIH	HIGH-level input voltage	B port	V _{REF} + 50 m	V _{REF} + 50 mV		
.,	1000	A port			0.8	.,
V_{IL}	LOW-level input voltage	B port			V _{REF} -50 mV	٧
loh	HIGH-level output current	A port			-16	mA
lOL	1000	A port			16	
	LOW-level output current	B port	15		15	mA
TA	Operating free-air temperature range	•	-40		85	°C



[‡] Voltages are referenced to GND (ground = 0 V).

^{2.} The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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electrical characteristics over recommended operating conditions

	DADAMETED	TEST CONDITIONS	–40°C	LINUT		
	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
\ \ +	Anad	$V_{CC} = 3 \text{ V to } 3.6 \text{ V, } I_{OH} = -100 \mu\text{A}$	V _{CC} - 0.2			.,
V _{OH} ‡	A port	$V_{CC} = 3 \text{ V, } I_{OH} = -16 \text{ mA}$	2.1			V
+	A port	V _{CC} = 3 V, I _{OL} = 16 mA			8.0	.,
V _{OL} ‡	B port	V _{CC} = 3 V, I _{OL} = 15 mA			0.4	V
	A port	$V_{CC} = 3.6 \text{ V}, V_I = V_{CC}$			±1	
Ц		V _{CC} = 3.6, V _I = 0 V			±1	μΑ
	B port	$V_{CC} = 3.6 \text{ V}, V_I = V_{TT} \text{ or GND}$			±1	
ICC	A or B port	$V_{CC} = 3.6 \text{ V}, V_{I} = V_{CC} \text{ or GND, } I_{O} = 0$			12	mA
Δlcc§	A port or control inputs	$V_{CC} = 3.6 \text{ V}, V_{I} = V_{CC} - 0.6 \text{ V}$			500	μΑ
Con	A port	V _O = 3 V or 0		5		
CIO	B port	$V_O = V_{TT}$ or 0		4		pF

 $[\]overline{\dagger}$ All typical values are measured at $V_{CC} = 3.3 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range

PARAMETER				GTL-			GTL			GTL+		
		WAVEFORM	V _{CC} = 3.3 V ± 0.3 V V _{REF} = 0.6 V		V _{CC} = 3.3 V ± 0.3 V V _{REF} = 0.8 V		V _{CC} = 3.3 V ± 0.3 V V _{REF} = 1 V		UNIT			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
^t PLH	An to Bn	1	2	4	8	2	4	8	2	4	8	20
^t PHL	An to bn	I	2	5.5	10	2	5.5	10	2	5.5	10	ns
^t PLH	Bn to An		2	5.5	10	2	5.5	10	2	5.5	10	20
^t PHL	DII IO AII	2	2	5.5	10	2	5.5	10	2	5.5	10	ns
^t PLH	0PI to 10POn		2	6	11	2	6	11	2	6	11	20
^t PHL	9BI to 10BOn	3	2	6	11	2	6	11	2	6	11	ns
^t PLH	440145 4400		2	8	13	2	8	13	2	8	13	
$t_{PHL}\P$	11BI to 11BO	3	2	14	21	2	14	21	2	14	21	ns
^t PLH	Do to Do		4	7	11	4	7	11	4	7	11	
tPHL	Bn to Bn	3	120	205	350	120	205	350	120	205	350	ns
tPLH	ENIO 40 Am	4	1	3	7	1	3	7	1	3	7	
^t PHL	ENn to An	4	1	3	7	1	3	7	1	3	7	ns
t _{PLZ}	Do to Ap (1/0)	_	2	5	10	2	5	10	2	5	10	
t _{PZL}	Bn to An (I/O)	5	2	5	10	2	5	10	2	5	10	ns
tPLZ	EN2 to An (I/O)	6	1	3	7	1	3	7	1	3	7	20
t _{PZL}	EINZ IO ATT (I/O)	0	1	3	7	1	3	7	1	3	7	ns

 $^{^{\}dagger}$ All typical values are measured at $V_{CC} = 3.3 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

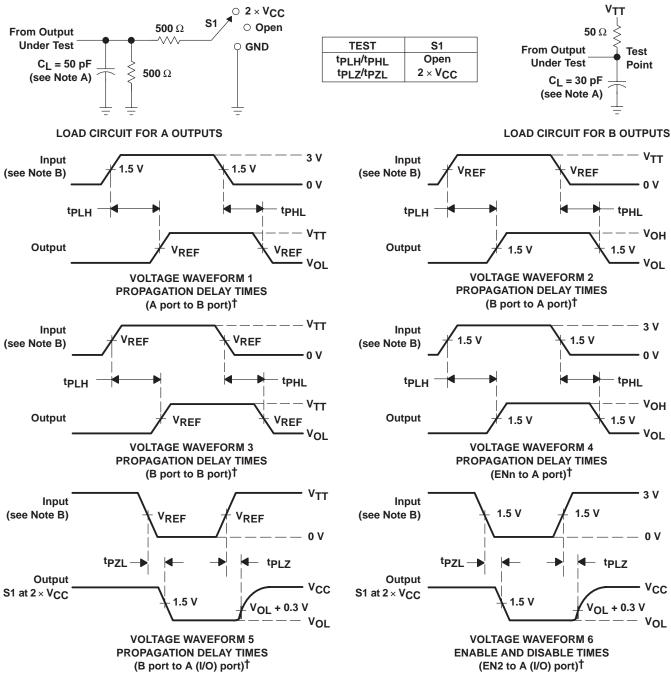


[‡] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[§] This is the increase in supply current for each input that is at the specified LVTTL voltage, rather than V_{CC} or GND.

[¶] Includes ~7.6-ns RC rise time of test-load pullup on 11-A, 1.5-kΩ pullup, and 21-pF load on 11 A has approximately 23-ns RC rise time.

PARAMETER MEASUREMENT INFORMATION V_{TT} = 1.2 V, V_{REF} = 0.8 V FOR GTL AND V_{TT} = 1.5 V, V_{REF} = 1 V FOR GTL+



† All control inputs are LVTTL levels.

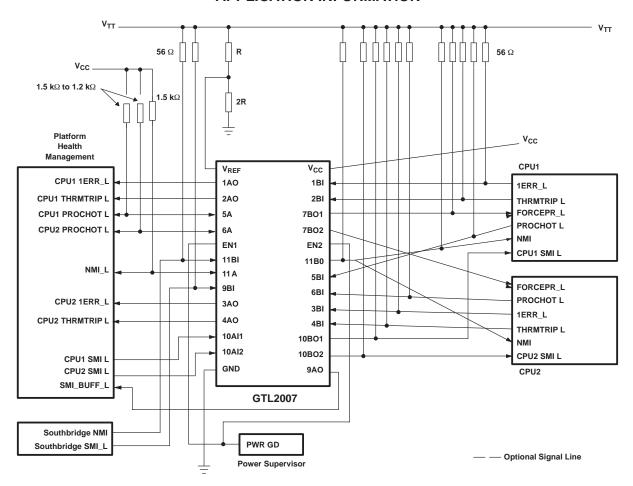
NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



APPLICATION INFORMATION



Frequently Asked Questions

Question 1: On the GTL2007 LVTTL input, specifically 10Al1 and 10Al2, when the GTL2007 is powered down, these inputs may be pulled up to 3.3 V, and we want to ensure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs high impedance when the device is powered down, and will there be any leakage?

Answer 1: When the device is powered down, the LVTTL inputs are in a high-impedance state and do not leak to V_{DD} if they are pulled high while the device is powered down.

Question 2: Do all the LVTTL inputs have the same powered-down characteristic?

Answer 2: Yes

Question 3: What is the condition of the other GTL I/O and LVTTL output pins when the device is powered down?

Answer 3: The open-drain outputs, both GTL and LVTTL, do not leak to the power supply if they are pulled high while the device is powered down. The GTL inputs also do not leak to the power supply under the same conditions. The LVTTL totem-pole outputs, however, are not open-drain type outputs, and there is no current flow on these pins if they are pulled high when V_{DD} is at ground.







.com 24-May-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74GTL2007PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2007PWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2007PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2007PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2007PWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2007PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

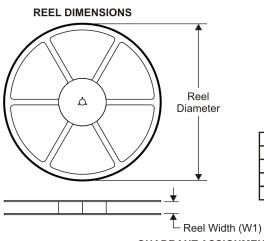
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

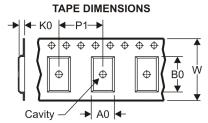
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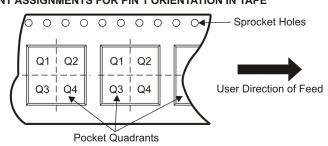
TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2007PWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1



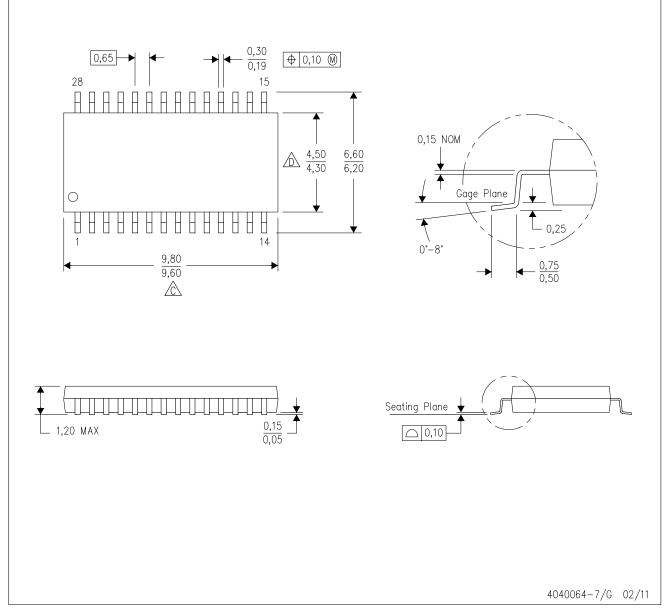


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2007PWR	TSSOP	PW	28	2000	346.0	346.0	33.0

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



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