

3.3 V Dual LVTTL/LVCMOS to Differential LVPECL Buffer

Check for Samples: SN65EPT22

FEATURES

- Dual 3.3V LVTTL to LVPECL Buffer
- Operating Range
 - LVPECL V_{CC} = 3.0 V to 3.6 V With GND = 0 V
- Support for Clock Frequencies to 2.0 GHz (typ)
- 420 ps Typical Propagation Delay
- Deterministic HIGH Output Value for Open Input Conditions
- Built-in Temperature Compensation
- Drop in Compatible to MC100ELT23
- PNP Single Ended Inputs for Minimal Loading

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

DESCRIPTION

The SN65EPT22 is a low power dual LVTTL to LVPECL translator device. The device includes circuitry to maintain known logic HIGH level when inputs are in open condition. The SN65EPT22 is housed in an industry standard SOIC-8 package and is also available in TSSOP-8 package option.

PINOUT ASSIGNMENT

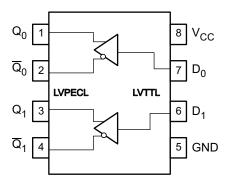


Table 1. Pin Description

| PIN | FUNCTION |
|--|-------------------|
| D ₀ , D ₁ | LVTTL data inputs |
| $Q_0, \overline{Q}_0, Q_1, \overline{Q}_1$ | LVPECL outputs |
| V _{CC} | Positive supply |
| GND | Ground |

ORDERING INFORMATION(1)

| PART NUMBER | PART MARKING | PACKAGE | LEAD FINISH |
|--------------|--------------|------------|-------------|
| SN65EPT22D | EPT22 | SOIC | NiPdAu |
| SN65EPT22DGK | EPT22 | SOIC-TSSOP | NiPdAu |

(1) Leaded device options not initially available. Contact sales representative for further details.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

| PARAMETER | CONDITION | VALUE | UNIT |
|--|--|------------|------|
| Absolute supply voltage, V _{CC} | | 6 | V |
| Absolute input voltage, VI | GND = 0 and VI ≤ V _{CC} | 0 to 6 | V |
| Supply voltage LVPEL | | 3.3 | V |
| Outrot suggest | Continuous | 50 | ^ |
| Output current | 6 GND = 0 and VI ≤ V _{CC} 0 to 6 3.3 Continuous 50 Surge 100 -40 to 85 | mA | |
| Operating temperature range | | -40 to 85 | °C |
| Storage temperature range | | -65 to 150 | °C |

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | POWER RATING T _A < 25°C (mW) | THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW | DERATING FACTOR T _A > 25°C (mW/°C) | POWER RATING T _A = 85°C (mW) |
|------------|------------------------|---|--|---|---|
| SOIC | Low-K | 719 | 139 | 7 | 288 |
| | High-K | 840 | 119 | 8 | 336 |
| SOIC-TSSOP | Low-K | 469 | 213 | 5 | 188 |
| | High-K | 527 | 189 | 5 | 211 |

THERMAL CHARACTERISTICS

| | PARAMETER | PACKAGE | VALUE | UNIT |
|-----------------|--------------------------------------|------------|-------|------|
| θ_{JB} | Junction-to Board Thermal Resistance | SOIC | 79 | °C/W |
| | | SOIC-TSSOP | 120 | |
| θ _{JC} | Junction-to Case Thermal Resistance | SOIC | 98 | °C/W |
| | | SOIC-TSSOP | 74 | |

KEY ATTRIBUTES

| CHARACTERISTICS | | VALUE |
|---|---------|-----------------------|
| Moisture sensitivity level | | Lead free package |
| | SOIC-8 | Level 1 |
| | TSSOP-8 | Level 3 |
| Flammability rating (Oxygen Index: 28 to 34) | | UL 94 V-0 at 0.125 in |
| ESD-HBM | | 4 kV |
| ESD-machine model | | 200 V |
| ESD-charge device model | | 2 kV |
| Meets or exceeds JEDEC Spec EIA/JESD78 latchup test | | |

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TTL INPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3 \text{ V}$, GND = 0, $T_A = -40 ^{\circ}\text{C}$ to 85°C)

| | CHARACTERISTIC | CONDITION | MIN | TYP | MAX | UNIT |
|------------------|------------------------|---------------------------|-----|-----|------|------|
| I _{IH} | Input HIGH current | $V_{IN} = 2.7 \text{ V}$ | | | 20 | μΑ |
| I _{IHH} | Input HIGH current max | $V_{IN} = V_{CC}$ | | | 100 | μΑ |
| I _{IL} | Input LOW current | V _{IN} = 0.5 V | | | -0.6 | mA |
| V_{IK} | Input clamp voltage | $I_{IN} = -18 \text{ mA}$ | | | -1 | V |
| V_{IH} | Input high voltage | | 2.0 | | | V |
| V _{IL} | Input low voltage | | | | 0.8 | V |

⁽¹⁾ Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

PECL OUTPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3 \text{ V}$; GND = 0.0V) (2)

| CHARACTERISTIC | | | –40°C | | | 25°C | | | 85°C | | |
|-----------------|-----------------------------------|------|-------|------|------|------|------|------|------|------|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| I _{CC} | Power supply current | | 39 | 45 | | 42 | 47 | | 45 | 50 | mA |
| V _{OH} | Output HIGH voltage (3) | 2155 | 2224 | 2405 | 2155 | 2224 | 2405 | 2155 | 2224 | 2405 | mV |
| V _{OL} | Output LOW voltage ⁽³⁾ | 1355 | 1441 | 1605 | 1355 | 1438 | 1605 | 1355 | 1435 | 1605 | mV |

⁽¹⁾ Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- (2) Output parameters vary 1:1 with V_{CC}
- (3) All loading with 50Ω to V_{CC} –2.0V

AC CHARACTERISTICS $^{(1)}(V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; \text{ GND} = 0 \text{ V})^{(2)}$

| | , 00 | | | | , | | | | | | |
|-------------------------------------|---|-------|-----|-----|------|-----|-----|------|-----|------|------|
| | | –40°C | | | 25°C | | | 85°C | | UNIT | |
| | CHARACTERISTIC | | | MAX | MIN | TYP | MAX | MIN | TYP | MAX | UNII |
| f _{MAX} | Max switching frequency (3), see Figure 5 | | 2.1 | | | 2.0 | | | 2.0 | | GHz |
| t _{PLH} / t _{PHL} | Propagation delay to differential output | 230 | | 550 | 230 | | 550 | 230 | | 550 | ps |
| | Within device skew ⁽⁴⁾ | | 25 | 50 | | 25 | 50 | | 25 | 50 | ps |
| t _{SKEW} | Device to device skew ⁽⁵⁾ | | 100 | 200 | | 100 | 200 | | 100 | 200 | ps |
| t _{JITTER} | Random clock jitter (RMS) | | 0.2 | 8.0 | | 0.2 | 8.0 | | 0.2 | 8.0 | ps |
| t _r / t _f | Output rise/fall times (20%–80%) | 150 | | 300 | 150 | | 300 | 150 | | 300 | ps |

⁽¹⁾ Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- (2) Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to VCC 2.0 V.
- (3) Maximum switching frequency measured at output amplitude of 300 mV_{pp}.
- (4) Skew is measured between outputs under identical transitions and conditions on any one device.
- (5) Device-to-Device Skew for identical transitions at identical VCC levels.

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Typical Termination for Output Driver

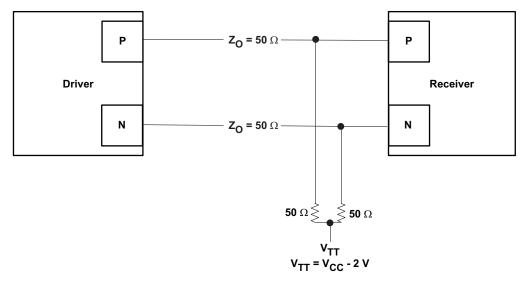


Figure 1. Termination for Output Driver

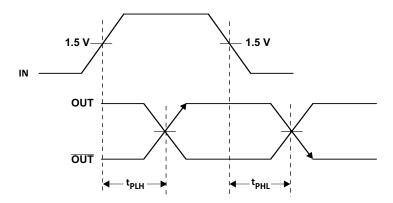


Figure 2. Output Propagation Delay

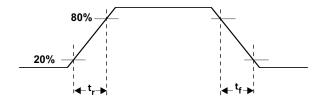


Figure 3. Output Rise and Fall Times



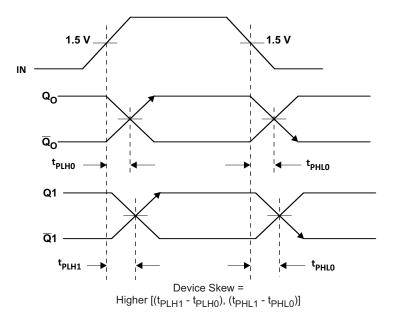


Figure 4. Device Skew

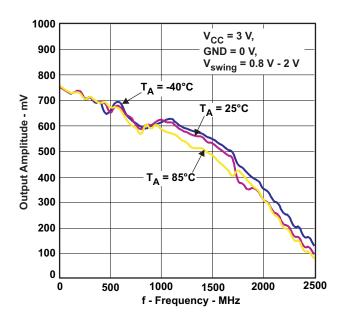


Figure 5. Output Amplitude versus Frequency



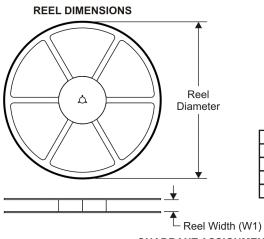
REVISION HISTORY

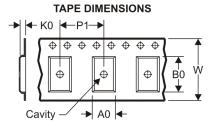
| Cł | hanges from Original (November 2010) to Revision A | Page |
|----|---|------|
| • | Changed SN65EPT22 to EPT22 (2 places) in Ordering Information Table under Part Marking column | 1 |

PACKAGE MATERIALS INFORMATION

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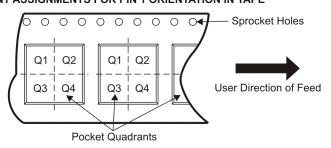
TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|-----------------|--------------------|---|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN65EPT22DGKR | MSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65EPT22DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65EPT22DGKR | MSOP | DGK | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| SN65EPT22DR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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