

# SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

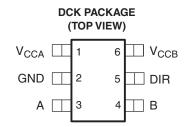
#### **FEATURES**

- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- V<sub>CC</sub> Isolation Feature If Either V<sub>CC</sub> Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V<sub>CCA</sub>
- Low Power Consumption, 4-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Max Data Rates
  - 420 Mbps (3.3-V to 5-V Translation)
  - 210 Mbps (Translate to 3.3 V)
  - 140 Mbps (Translate to 2.5 V)
  - 75 Mbps (Translate to 1.8 V)

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C)
   Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- (1) Additional temperature ranges are available contact factory



See mechanical drawings for dimensions.

### **DESCRIPTION/ORDERING INFORMATION**

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

### ORDERING INFORMATION(1)

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
-55°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	SN74LVC1T45MDCKREP	NXG

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (3) The actual top-side marking has one additional character that designates the assembly/test site.



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### **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The SN74LVC1T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74LVC1T45 is designed so that the DIR input is powered by V<sub>CCA</sub>.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

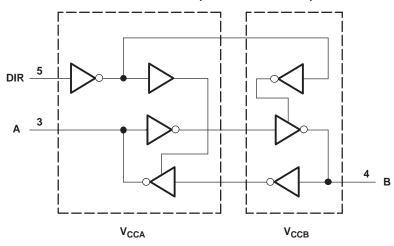
The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then both ports are in the high-impedance state.

### **FUNCTION TABLE**(1)

INPUT DIR	OPERATION
L	B data to A bus
Н	A data to B bus

 Input circuits of the data I/Os always are active.

### **LOGIC DIAGRAM (POSITIVE LOGIC)**





### Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CCA}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power	er-off state (2)	-0.5	6.5	V
V	Voltage range applied to any output in the high or low state (2)(3)	A port	-0.5	$V_{CCA} + 0.5$	V
Vo	voltage range applied to any output in the high or low state.	B port	-0.5	$V_{CCB} + 0.5$	V
$I_{IK}$	Input clamp current	V <sub>I</sub> < 0		-50	mA
$I_{OK}$	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		259	°C/W	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. The value of  $V_{CC}$  is provided in the recommended operating conditions table. The package thermal impedance is calculated in accordance with JESD 51-7.

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### Recommended Operating Conditions (1)(2)(3)

			V <sub>CCI</sub>	V <sub>cco</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.65	5.5	V
V <sub>CCB</sub>	Supply voltage				1.65	5.5	V
			1.65 V to 1.95 V		V <sub>CCI</sub> × 0.65		
.,	High-level	Data inputs (4)	2.3 V to 2.7 V		1.7		V
$V_{IH}$	input voltage	Data inputs (7	3 V to 3.6 V		2		V
			4.5 V to 5.5 V		$V_{CCI} \times 0.7$		
			1.65 V to 1.95 V			$V_{\rm CCI} \times 0.35$	
.,	Low-level	Data inputs (4)	2.3 V to 2.7 V			0.7	V
$V_{IL}$	input voltage	Data Inputs**	3 V to 3.6 V			0.8	V
			4.5 V to 5.5 V			$V_{\rm CCI} \times 0.3$	
			1.65 V to 1.95 V		V <sub>CCA</sub> × 0.65		
. ,	High-level	DIR	2.3 V to 2.7 V		1.7		.,
$V_{IH}$	input voltage	(referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	3 V to 3.6 V		2		V
			4.5 V to 5.5 V		$V_{CCA} \times 0.7$		
			1.65 V to 1.95 V			$V_{CCA} \times 0.35$	
. ,	Low-level	DIR	2.3 V to 2.7 V			0.7	.,
$V_{IL}$	input voltage	(referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	3 V to 3.6 V			0.8	V
			4.5 V to 5.5 V			$V_{CCA} \times 0.3$	
VI	Input voltage	1			0	5.5	V
Vo	Output voltage				0	V <sub>cco</sub>	V
				1.65 V to 1.95 V		-4	
	I Pade Javas Laudavid a			2.3 V to 2.7 V		-8	A
l <sub>OH</sub>	High-level output c	urrent		3 V to 3.6 V		-24	mA
				4.5 V to 5.5 V		-32	
				1.65 V to 1.95 V		4	
	Landard and and			2.3 V to 2.7 V		8	A
l <sub>OL</sub>	Low-level output co	urrent		3 V to 3.6 V		24	mA
				4.5 V to 5.5 V		32	
			1.65 V to 1.95 V			20	
		Data Sanata	2.3 V to 2.7 V			20	
Δt/Δν	Input transition rise or fall rate	3 V to 3.6 V			10	ns/V	
		4.5 V to 5.5 V			5		
		Control inputs	1.65 V to 5.5 V			5	
T <sub>A</sub>	Operating free-air	temperature			<b>–</b> 55	125	°C

 $<sup>\</sup>begin{array}{ll} \text{(1)} & \text{$V_{\text{CCI}}$ is the $V_{\text{CC}}$ associated with the input port.} \\ \text{(2)} & \text{$V_{\text{CCO}}$ is the $V_{\text{CC}}$ associated with the output port.} \\ \end{array}$ 

All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004. For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCI} \times 0.7 \text{ V}$ ,  $V_{IL}$  max =  $V_{CCI} \times 0.3 \text{ V}$ . For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCA} \times 0.7 \text{ V}$ ,  $V_{IL}$  max =  $V_{CCA} \times 0.3 \text{ V}$ .



### Electrical Characteristics (1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	IONE	V	v	T,	4 = 25°C		−55°C to	125°C	UNIT
PARA	AIVIETER	TEST CONDIT	IONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNII
		$I_{OH} = -100 \ \mu A$		1.65 V to 4.5 V	1.65 V to 4.5 V				V <sub>CCO</sub> - 0.1		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.65 V				1.2		
$V_{OH}$		$I_{OH} = -8 \text{ mA}$	$V_I = V_{IH}$	2.3 V	2.3 V				1.9		V
		I <sub>OH</sub> = -24 mA		3 V	3 V				2.4		
		$I_{OH} = -32 \text{ mA}$		4.5 V	4.5 V				3.8		
		$I_{OL} = 100  \mu A$		1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	
		I <sub>OL</sub> = 4 mA		1.65 V	1.65 V					0.45	
$V_{OL}$		$I_{OL} = 8 \text{ mA}$	$V_{I} = V_{IL}$	2.3 V	2.3 V					0.3	V
		I <sub>OL</sub> = 24 mA		3 V	3 V					0.55	
		$I_{OL} = 32 \text{ mA}$		4.5 V	4.5 V					0.55	
lı	DIR	$V_I = V_{CCA}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	μΑ
	A port	\\ -=\\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	.,	0 V	0 to 5.5 V			±1		±6	^
l <sub>off</sub>	B port	$V_{\rm I}$ or $V_{\rm O} = 0$ to 5.5	V	0 to 5.5 V	0 V			±1		±6	μΑ
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±6	μΑ
	•			1.65 V to 5.5 V	1.65 V to 5.5 V					4	
$I_{CCA}$		$V_I = V_{CCI}$ or GND,	$I_O = 0$	5.5 V	0 V					2	μΑ
				0 V	5.5 V					-4	
				1.65 V to 5.5 V	1.65 V to 5.5 V					4	
I <sub>CCB</sub>		$V_I = V_{CCI}$ or GND,	$I_O = 0$	5.5 V	0 V					-4	μΑ
				0 V	5.5 V					2	
I <sub>CCA</sub> + I (see Ta	I <sub>CCB</sub> able 1)	$V_I = V_{CCI}$ or GND,	I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					4	μΑ
	A port	A port at V <sub>CCA</sub> – 0.6 DIR at V <sub>CCA</sub> , B port	SV, t = open							50	
ΔI <sub>CCA</sub>	DIR	DIR at V <sub>CCA</sub> – 0.6 V B port = open, A port at V <sub>CCA</sub> or G	/,	3 V to 5.5 V	3 V to 5.5 V					50	μΑ
ΔI <sub>CCB</sub>	B port	B port at V <sub>CCB</sub> – 0.6 DIR at GND, A port = open	6 V,	3 V to 5.5 V	3 V to 5.5 V					50	μА
Ci	DIR	$V_I = V_{CCA}$ or GND	-	3.3 V	3.3 V		2.5				pF
C <sub>io</sub>	A or B port	$V_O = V_{CCA/B}$ or GNI	D	3.3 V	3.3 V		6				pF

 $<sup>\</sup>begin{array}{ll} \hbox{(1)} & V_{CCO} \text{ is the } V_{CC} \text{ associated with the output port.} \\ \hbox{(2)} & V_{CCI} \text{ is the } V_{CC} \text{ associated with the input port.} \\ \end{array}$ 

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### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see Figure 1)

PARAMETER	FROM						V <sub>CCB</sub> = 2.5 V ±0.2 V		V <sub>CCB</sub> = 3.3 V ±0.3 V		V <sub>CCB</sub> = 5 V ±0.5 V		UNIT
	(IIVI O1)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>PLH</sub>	А	В	3	20.7	2.2	13.3	1.7	11.3	1.4	10.2			
t <sub>PHL</sub>	A	В	2.8	17.3	2.2	11.5	1.8	10.1	1.7	10	ns		
t <sub>PLH</sub>	В	A	3	20.7	2.3	19	2.1	18.5	1.9	18.1	no		
t <sub>PHL</sub>	Ь	A	2.8	17.3	2.1	15.9	2	18.6	1.8	15.2	ns		
t <sub>PHZ</sub>	DIR	A	5.2	22.4	4.8	21.5	4.7	21.4	5.1	20.1	20		
t <sub>PLZ</sub>	DIK	A	2.3	13.5	2.1	13.5	2.4	13.7	3.1	13.9	ns		
t <sub>PHZ</sub>	DIR	В	7.4	24.9	4.9	14.5	4.6	13.3	2.8	11.2	no		
t <sub>PLZ</sub>	DIK	В	4.2	19	3.7	12.2	3.3	11.4	2.4	10.4	ns		
t <sub>PZH</sub> <sup>(1)</sup>	DID	^		39.7		31.2		29.9		27.5			
t <sub>PZL</sub> <sup>(1)</sup>	DIR	A		42.2		30.4		28.9		26.4	ns		
t <sub>PZH</sub> <sup>(1)</sup>	DIR	DIR B		34.2		26.8		25		24.1			
t <sub>PZL</sub> <sup>(1)</sup>		В		39.7		33		31.5		30.1	ns		

<sup>(1)</sup> The enable time is a calculated value, derived using the formula shown in the enable times section.

### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = ±0.15	1.8 V 5 V	V <sub>CCB</sub> = ±0.2		V <sub>CCB</sub> = ±0.3		V <sub>CCB</sub> = ±0.5		UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	В	2.3	19	1.5	11.5	1.3	9.4	1.1	8.1	no
t <sub>PHL</sub>	A	ь	2.1	15.9	1.4	10.5	1.3	8.4	0.9	7.6	ns
t <sub>PLH</sub>	В	А	2.2	13.3	1.5	11.5	1.4	11	1	10.5	
t <sub>PHL</sub>	Б	A	2.2	11.5	1.4	10.5	1.3	10	0.9	9.2	ns
t <sub>PHZ</sub>	DIR	А	3	11.1	3.1	11.1	2.8	11.1	3.2	11.1	no
t <sub>PLZ</sub>	DIK	A	1.3	8.9	1.3	8.9	1.3	8.9	1	8.8	ns
t <sub>PHZ</sub>	DIR	В	6.5	26.7	4.1	14.4	3.9	13.2	2.4	10.1	
t <sub>PLZ</sub>	אוט	В	3.9	21.9	3.2	12.6	2.8	11.4	1.8	8.3	ns
t <sub>PZH</sub> <sup>(1)</sup>	DID	۸		35.2		24.1		22.4		18.8	
t <sub>PZL</sub> <sup>(1)</sup>	אוט	DIR A		38.2		24.9		23.2		19.3	ns
t <sub>PZH</sub> <sup>(1)</sup>	DIB	В		27.9		20.4		18.3		16.9	no
t <sub>PZL</sub> <sup>(1)</sup>	DIR	В		27		21.6		19.5		18.7	ns

<sup>(1)</sup> The enable time is a calculated value, derived using the formula shown in the enable times section.



### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = ±0.15	1.8 V 5 V	V <sub>CCB</sub> = ±0.2		V <sub>CCB</sub> = ±0.3		V <sub>CCB</sub> = ±0.5		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	В	2.1	18.5	1.4	11	0.7	8.8	0.7	7.4	20
t <sub>PHL</sub>	A	ь	2	15.6	1.3	10	0.8	8	0.7	7	ns
t <sub>PLH</sub>	В	А	1.7	11.3	1.3	9.4	0.7	8.8	0.6	8.4	20
t <sub>PHL</sub>	В	A	1.8	10.1	1.3	8.4	0.8	8	0.7	7.5	ns
t <sub>PHZ</sub>	DIR	A	2.9	10.3	3	10.3	2.8	10.3	3.4	10.3	no
t <sub>PLZ</sub>	DIK		1.8	8.6	1.6	8.6	2.2	8.7	2.2	8.7	ns
t <sub>PHZ</sub>	DIR	В	5.4	23.5	3.9	13.1	2.9	11.8	2.4	9.8	20
t <sub>PLZ</sub>	DIK	ь	3.3	17.5	2.9	10.8	2.4	10.1	1.7	7.9	ns
t <sub>PZH</sub> <sup>(1)</sup>	DIB	۸		28.8		20.2		18.9		16.3	20
t <sub>PZL</sub> <sup>(1)</sup>	DIR	DIR A		31.6		21.5		19.8		17.3	ns
t <sub>PZH</sub> <sup>(1)</sup>	DIR	В		27.1		19.6		17.5		16.1	
t <sub>PZL</sub> <sup>(1)</sup>		DIR	В		25.9		20.3		18.3		17.3

<sup>(1)</sup> The enable time is a calculated value, derived using the formula shown in the enable times section.

### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = ±0.15	1.8 V 5 V	V <sub>CCB</sub> = ±0.2		V <sub>CCB</sub> = 3 ±0.3		V <sub>CCB</sub> = ±0.5	5 V V	UNIT
	(INPOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	В	1.9	18.1	1	10.5	0.6	8.4	0.5	6.9	ns
t <sub>PHL</sub>	A	Б	1.8	15.2	0.9	9.2	0.7	7.5	0.5	6.5	115
t <sub>PLH</sub>	В	А	1.4	10.2	1	8.1	0.7	7.4	0.5	6.9	
t <sub>PHL</sub>	Б	A	1.7	10	0.9	7.6	0.7	7	0.5	6.5	ns
t <sub>PHZ</sub>	DIR	А	2.1	8.4	2.2	8.4	2.2	8.5	2.2	8.4	ns
t <sub>PLZ</sub>	DIK	A	0.9	6.8	1	6.8	1	6.7	0.9	6.7	115
t <sub>PHZ</sub>	DIR	В	4.8	23.2	2.5	12.8	1	11.5	2.5	9.5	
t <sub>PLZ</sub>	אוט	Б	4.2	17.8	2.5	10.4	2.5	10	1.6	7.5	ns
t <sub>PZH</sub> <sup>(1)</sup>	DID	۸		28		18.5		17.4		14.4	
t <sub>PZL</sub> <sup>(1)</sup>	DIR	Α		31.2		20.4		18.5		16	ns
t <sub>PZH</sub> <sup>(1)</sup>	DIR	В		24.9		17.3		15.1		13.6	no
t <sub>PZL</sub> <sup>(1)</sup>	DIK	В		23.6		17.6		16		14.6	ns

<sup>(1)</sup> The enable time is a calculated value, derived using the formula shown in the enable times section.

### **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 5 V	UNIT
			IIF	IIF	IIF	IIF	
o (1)	A-port input, B-port output	$C_L = 0 pF$ ,	3	4	4	4	_
C <sub>pdA</sub> <sup>(1)</sup>	B-port input, A-port output	f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	18	19	20	21	pF
(4)	A-port input, B-port output	$C_L = 0 pF$ ,	18	19	20	21	
C <sub>pdB</sub> <sup>(1)</sup>	B-port input, A-port output	f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	3	4	4	4	pF

<sup>(1)</sup> Power dissipation capacitance per transceiver

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### **Power-Up Considerations**

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

- 1. Connect ground before any supply voltage is applied.
- 2. Power up V<sub>CCA</sub>.
- 3.  $V_{CCB}$  can be ramped up along with or after  $V_{CCA}$ .

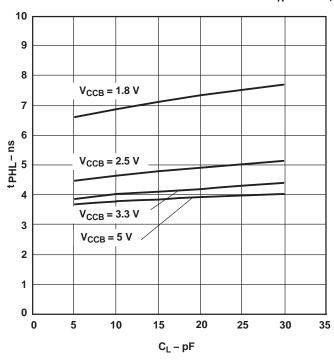
Table 1. Typical Total Static Power Consumption (I<sub>CCA</sub> + I<sub>CCB</sub>)

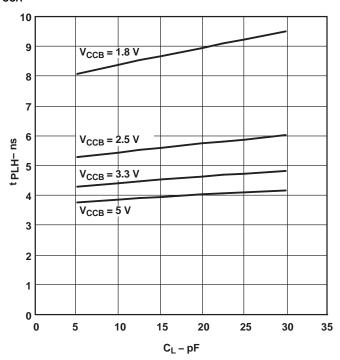
V			V <sub>CCA</sub>			UNIT
V <sub>CCB</sub>	0 V	1.8 V	2.5 V	3.3 V	5 V	UNII
0 V	0	<1	<1	<1	<1	
1.8 V	<1	<2	<2	<2	2	
2.5 V	<1	<2	<2	<2	<2	μΑ
3.3 V	<1	<2	<2	<2	<2	
5 V	<1	2	<2	<2	<2	



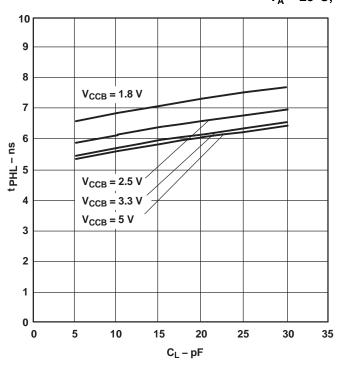
### TYPICAL CHARACTERISTICS

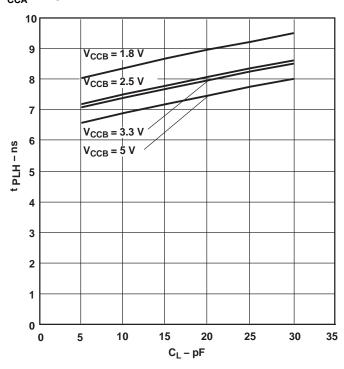
# TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_{\text{A}} = 25^{\circ}\text{C}, \, V_{\text{CCA}} = 1.8 \; \text{V}$





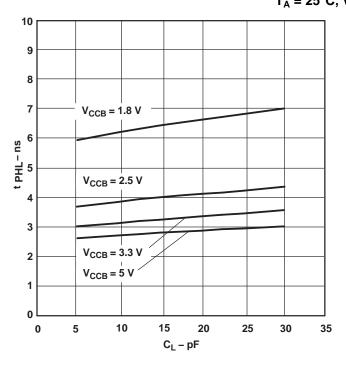
## TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE $\rm T_A = 25^{\circ}C, \, V_{CCA} = 1.8 \; V$

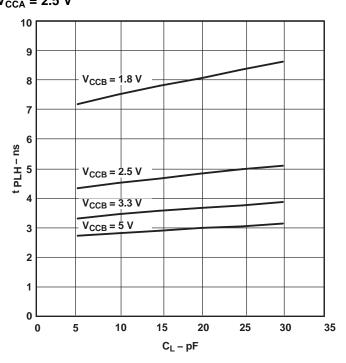




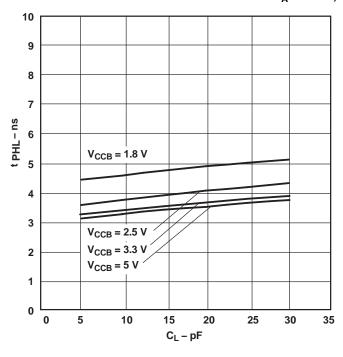


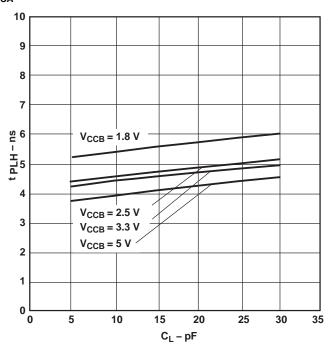
# TYPICAL CHARACTERISTICS (continued) TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_{\rm A}=25^{\circ}\text{C},\,V_{\rm CCA}=2.5\,\text{V}$





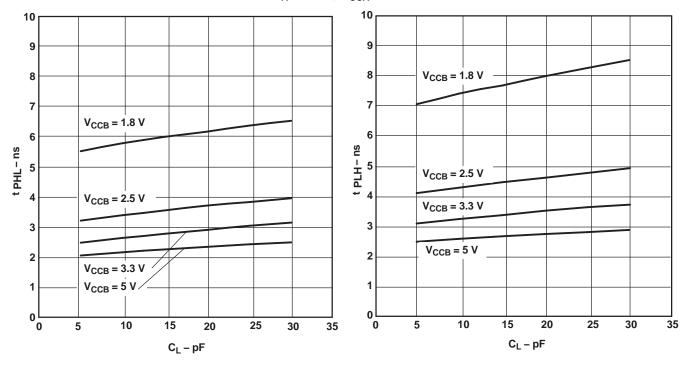
## TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE $T_{\text{A}} = 25^{\circ}\text{C}, \, V_{\text{CCA}} = 2.5 \, \text{V}$



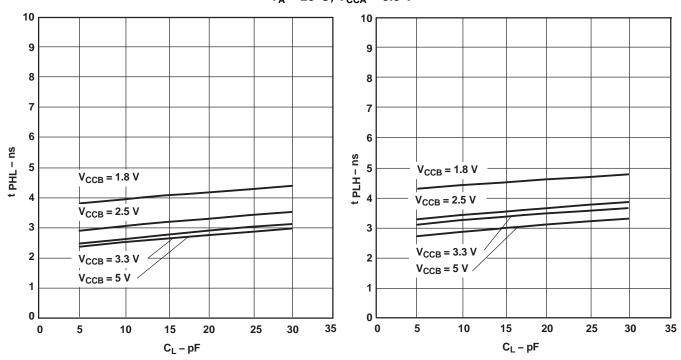


### TYPICAL CHARACTERISTICS (continued)

# TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $\rm T_A=25^{\circ}C,\,V_{CCA}=3.3~V$



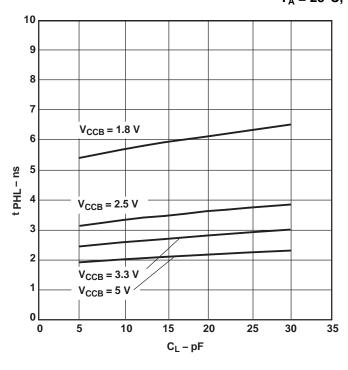
## TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE $T_{\text{A}}$ = 25°C, $V_{\text{CCA}}$ = 3.3 V

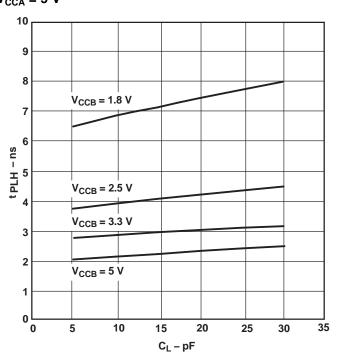


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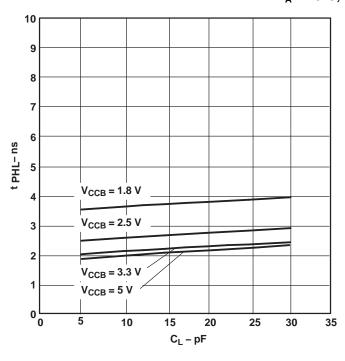


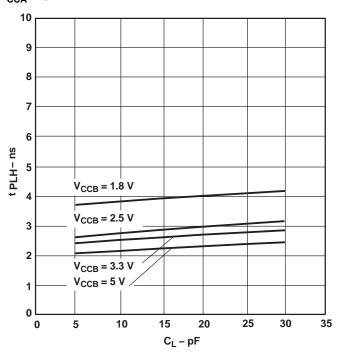
# TYPICAL CHARACTERISTICS (continued) TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_A=25^{\circ}\text{C},\,V_{\text{CCA}}=5\text{ V}$





## TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE $T_{A}$ = 25°C, $V_{CCA}$ = 5 V





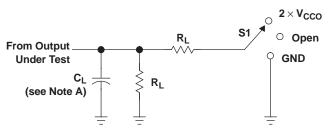
 $V_{\text{CCA}}$ 

CCA/2



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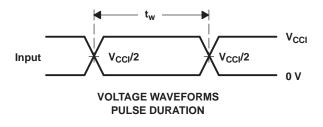
#### PARAMETER MEASUREMENT INFORMATION



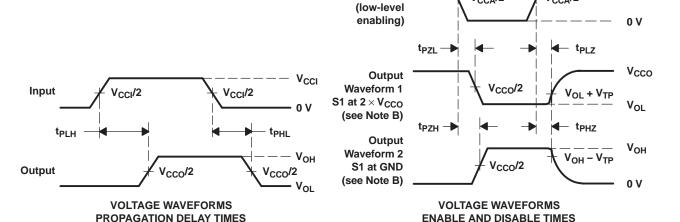
TEST	S1
t <sub>pd</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	$2 \times V_{CCO}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

**LOAD CIRCUIT** 

V <sub>cco</sub>	CL	R <sub>L</sub>	V <sub>TP</sub>
1.8 V $\pm$ 0.15 V	15 pF	<b>2 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	<b>2 k</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	<b>2 k</b> Ω	0.3 V
5 V $\pm$ 0.5 V	15 pF	<b>2 k</b> Ω	0.3 V



V<sub>CCA</sub>/2



Output Control

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $dv/dt \geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{Pl,7}$  and  $t_{PH7}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
- I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

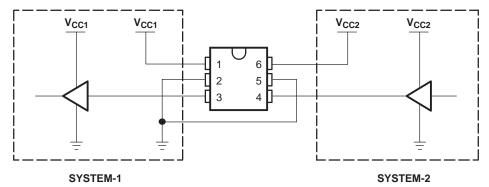
Figure 1. Load Circuit and Voltage Waveforms

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### **APPLICATION INFORMATION**

Figure 2 shows an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.

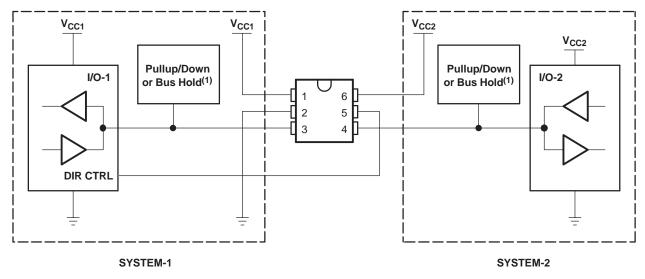


PIN	NAME	FUNCTION	DESCRIPTION
1	V <sub>CCA</sub>	V <sub>CC1</sub>	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V <sub>CC1</sub> voltage.
4	В	IN	Input threshold value depends on V <sub>CC2</sub> voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V <sub>CCB</sub>	V <sub>CC2</sub>	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

Figure 2. Unidirectional Logic Level-Shifting Application

#### **APPLICATION INFORMATION**

Figure 3 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Since the SN74LVC1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	Н	Out	In	SYSTEM-1 data to SYSTEM-2
2	Н	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. (1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. (1)
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 3. Bidirectional Logic Level-Shifting Application

### **Enable Times**

Calculate the enable times for the SN74LVC1T45 using the following formulas:

- $t_{PZH}$  (DIR to A) =  $t_{PLZ}$  (DIR to B) +  $t_{PLH}$  (B to A)
- $t_{PZL}$  (DIR to A) =  $t_{PHZ}$  (DIR to B) +  $t_{PHL}$  (B to A)
- $t_{PZH}$  (DIR to B) =  $t_{PLZ}$  (DIR to A) +  $t_{PLH}$  (A to B)
- $t_{PZL}$  (DIR to B) =  $t_{PHZ}$  (DIR to A) +  $t_{PHL}$  (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

30-Jan-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
LVC1T45MDCKREPG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1T45MDCKREP	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
V62/09608-01XE	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74LVC1T45-EP:

Catalog: SN74LVC1T45





30-Jan-2012

Automotive: SN74LVC1T45-Q1

NOTE: Qualified Version Definitions:

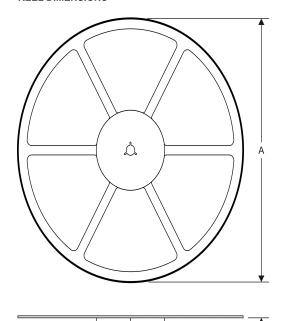
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

### PACKAGE MATERIALS INFORMATION

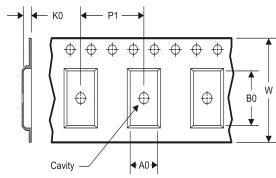
www.ti.com 6-Apr-2012

### TAPE AND REEL INFORMATION

### **REEL DIMENSIONS**







A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45MDCKREP	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3

**PACKAGE MATERIALS INFORMATION** 

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45MDCKREP	SC70	DCK	6	3000	202.0	201.0	28.0

### DCK (R-PDSO-G6)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



### DCK (R-PDSO-G6)

### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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