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18-BIT LVTTL-TO-GTLP UNIVERSAL BUS TRANSCEIVER

DGG OR DL PACKAGE

(TOP VIEW)

SCES326C-MARCH 2000-REVISED MAY 2005

FEATURES

- Member of Texas Instruments Widebus™ Family
- **UBT™ Transceiver Combines D-Type Latches** and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or **Clock-Enabled Modes**
- **OEC™** Circuitry Improves Signal Integrity and **Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal** Levels and LVTTL Logic Levels
- **LVTTL Interfaces are 5-V Tolerant**
- Medium-Drive GTLP Outputs (34 mA)
- LVTTL Outputs (-32 mA/64 mA)
- GTLP Rise and Fall Times Designed for **Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- I_{off} Supports Partial-Power-Down Mode Operation
- **Bus Hold on A-Port Inputs**
- Distributed V_{CC} and GND Pins Minimize **High-Speed Switching Noise**
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

56 CEAB OEAB 1 LEAB 2 55 CLKAB A1 🛮 3 54∏ B1 GND 4 53 GND A2 🛮 5 52∏ B2 A3 🛮 6 51 **∏** B3 V_{CC} (3.3 V) **1**7 50 V_{CC} (5 V) A4 🛮 8 49∏ B4 A5 🛮 9 48 B5 47**∏** B6 A6 🛮 10 46 GND GND 11 A7 🛮 12 45**∏** B7 A8 II 13 44∏ B8 A9 🛮 14 43 ∏ B9 A10 [] 15 42**∏** B10 A11 116 41**∏** B11 A12 🛮 17 40**∏** B12 GND 18 39 **∏** GND A13 🛮 19 38**∏** B13 A14 20 37**∏** B14 A15 21 36 B15 V_{CC} (3.3 V) 22 35 [] V_{REF} A16 23 34 🛮 B16 A17 🛮 24 33**∏** B17 GND **2**5 32 GND A18 🛮 26 31 B18 30 CLKBA OEBA 27 LEBA 28 29 CEBA

DESCRIPTION

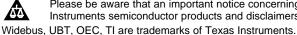
The SN74GTLPH16612 is a medium-drive, 18-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer. This device provides a high-speed interface between cards operating at LVTTL logic levels and backplanes operating at GTLP signal levels. High-speed (about two times faster than standard LVTTL or TTL) backplane operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry. These improvements minimize bus-settling time and have been designed and tested using several backplane models.

GTLP is a Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16612 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2 \text{ V}$ and $V_{REF} = 0.8 \text{ V}$) or GTLP ($V_{TT} = 1.5 \text{ V}$ and

 $V_{REF} = 1 \text{ V}$) signal levels.

The B port normally operates at GTLP levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{RFF} is the reference input voltage for the B port.

To improve signal integrity, the SN74GTLPH16612 B-port output transition time is optimized for distributed backplane loads.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DESCRIPTION (CONTINUED)

V_{CC} (5 V) supplies the internal and GTLP circuitry, while V_{CC} (3.3 V) supplies the LVTTL output buffers.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKA	GE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP – DL	Tube	SN74GTLPH16612DL	GTLPH16612	
–40°C to 85°C	330P - DL	Tape and reel	SN74GTLPH16612DLR		
	TSSOP - DGG	Tape and reel	SN74GTLPH16612GR	GTLPH16612	

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLPH16612 is a medium-drive (34 mA), 18-bit UBT transceiver, containing D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16612 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT	
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863	
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825	
Latched transceiver	'543			'16543	'16472	
Latch	'373, '573	'843	'841	'16373	'16843	
Registered transceiver	'646, '652			'16646, '16652	'16474	
Flip-flop	'374, '574		'821	'16374		
Standard UBT					'16500, '16501	
Universal bus driver					'16835	
Registered transceiver with clock enable	'2952			'16470, '16952		
Flip-flop with clock enable	'377	'823			'16823	
Standard UBT with clock enable					'16600, '16601	
SN74G	TLPH16612 UBT transc	eiver repla	ces all abov	ve functions		

Data flow in each direction is controlled by the clock enables (CEAB and CEBA), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables (OEAB and OEBA).

For A-to-B data flow, when $\overline{\text{CEAB}}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{\text{CEAB}}$ and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state.

The data flow for B-to-A is similar to that of A-to-B, except that CEBA, OEBA, LEBA, and CLKBA are used.

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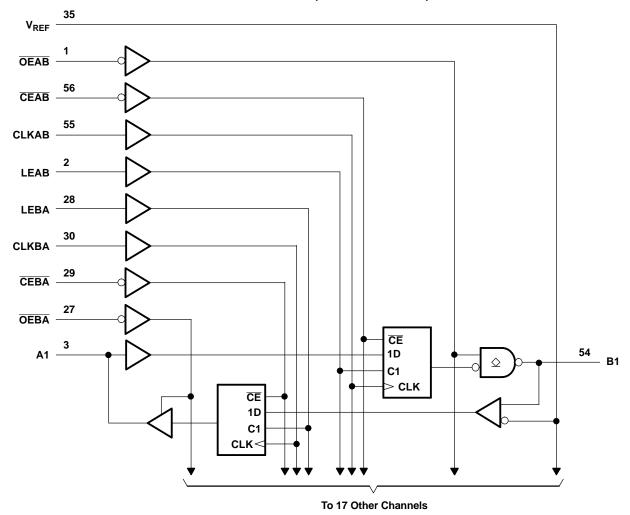


FUNCTION TABLE(1)

		INPUTS			OUTPUT	MODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
Х	Н	Χ	Χ	Χ	Z	Isolation
L	L	L	Н	Χ	B ₀ ⁽²⁾	Latebad storage of A data
L	L	L	L	Χ	B ₀ ⁽³⁾	Latched storage of A data
Х	L	Н	Х	L	L	True transparent
Х	L	Н	Χ	Н	Н	True transparent
L	L	L	1	L	L	Clocked stores of A data
L	L	L	\uparrow	Н	Н	Clocked storage of A data
Н	L	L	Х	Х	B ₀ ⁽³⁾	Clock inhibit

- (1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, LEBA, and CLKBA. The condition when $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ are both low at the same time is not recommended.
- (2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.
- (3) Output level before the indicated steady-state input conditions were established.

LOGIC DIAGRAM (POSITIVE LOGIC)



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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT		
.,	Cupply veltage range	3.3 V	-0.5	4.6	V		
V _{CC}	Supply voltage range	5 V	-0.5	7	V		
\/	Input valtage range (2)	A port and control inputs	-0.5	7	V		
VI	Input voltage range (2)	B port and V _{REF}	-0.5	4.6	V		
\/	Voltage range applied to any output in the high-impedance or	A port	-0.5	7	V		
Vo	power-off state (2)	B port	-0.5	4.6	V		
	Comment into any system tin the law state	A port		128	A		
IO	Current into any output in the low state	B port		80	mA		
Io	Current into any A-port output in the high state (3)			64	mA		
	Continuous current through each V _{CC} or GND			±100	mA		
I _{IK}	Input clamp current	V ₁ < 0		-50	mA		
I _{OK}	Output clamp current	V _O < 0		-50	mA		
0	Declines the small improduces (4)	DGG package		64	00/1/1		
θ_{JA}	Package thermal impedance ⁽⁴⁾	DL package		7 4.6 128 80 64 ±100 -50 -50	°C/W		
T _{stg}	Storage temperature range	·	-65	150	°C		

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings (1) only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (1)(2)(3)(4)

			MIN	NOM	MAX	UNIT		
V	Cupply voltage	3.3 V	3.15	3.3	3.45	V		
V _{CC}	Supply voltage	5 V	4.75	5	5.25	V		
V	Towningtion welfang	GTL	1.14	1.2	1.26	V		
V _{TT}	Termination voltage	GTLP	1.35	1.5	1.65	V		
.,	Defended with the	GTL	0.74	0.8	0.87			
V_{REF}	Reference voltage	GTLP	0.87	1	1.1	V		
V	lament coalita a a	B port			V _{TT}	V		
VI	Input voltage	Except B port		V _{CC}	5.5	V		
V	High level input valtage	B port	V _{REF} + 50 mV	0 mV		V		
V _{IH}	High-level input voltage	Except B port	2			V		
V	Lauran in must walte an	B port		V	_{REF} – 50 mV	V		
V_{IL}	Low-level input voltage	Except B port			0.8	V		
I _{IK}	Input clamp current	·			-18	mA		
I _{OH}	High-level output current	A port			-32	mA		
1	Law law all autout aumant	A port			64	A		
I _{OL}	Low-level output current	B port			34	mA		
T _A	Operating free-air temperature		-40		85	°C		

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This current flows only when the output is in the high state and $V_O > V_{CC}$.

The package thermal impedance is calculated in accordance with JESD 51-7.

Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} , and V_{REF} (any order) last. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

 V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} .



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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER		TEST CONDITIONS		MIN	TYP ⁽¹⁾ MAX	UNIT	
V _{IK}		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I _I = -18 mA		-1.2	V	
		V _{CC} (3.3 V) = 3.15 V to 3.45 V V _{CC} (5 V) = 4.75 V to 5.25 V	V,	I _{OH} = -100 μA	V _{CC} (3.3 V) - 0.2			
V_{OH}	A port	V (2.2.V) 2.45.V	\/ (F\)\\ A7E\/	$I_{OH} = -8 \text{ mA}$	2.4		V	
		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	$I_{OH} = -32 \text{ mA}$	2			
				I _{OL} = 100 μA		0.2		
	At	V _{CC} (3.3 V) = 3.15 V,	\/ (F\)\\ 47E\/	I _{OL} = 16 mA		0.4		
V_{OL}	A port		V_{CC} (5 V) = 4.75 V	I _{OL} = 32 mA		0.5	V	
				I _{OL} = 64 mA		0.55		
	B port	V_{CC} (3.3 V) = 3.15 V,	V _{CC} (5 V) = 4.75 V,	I _{OL} = 34 mA		0.65		
	Control inputs	V_{CC} (3.3 V) = 0 or 3.45 V,	V_{CC} (5 V) = 0 or 5.25 V,	V _I = 5.5 V		10		
				V _I = 5.5 V		20		
I _I	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	$V_{I} = V_{CC} (3.3 \text{ V})$		1	μA	
				$V_I = 0$		-30	μ, ι	
	.	V (0.0.V) 0.45.V	V (5.10 5.05.V	$V_{I} = V_{CC} (3.3 \text{ V})$		5	1	
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V _I = 0		-5		
I _{off}		$V_{CC} = 0$,	V_{1} or $V_{0} = 0$ to 4.5 V			100	μA	
				V _I = 0.8 V	75			
l	A port	V_{CC} (3.3 V) = 3.15 V,	V _{CC} (5 V) = 4.75 V	V _I = 2 V	-75		μA	
I _{I(hold)}	A poit	VCC (0.0 V) = 3.10 V,	VCC (5 V) = 4.75 V	$V_1 = 0 \text{ to}$ $V_{CC} (3.3 \text{ V})^{(2)}$		±500	μΛ	
	A port	V_{CC} (3.3 V) = 3.45 V,	V _{CC} (5 V) = 5.25 V,	$V_{O} = V_{CC} (3.3 \text{ V})$		1		
l _{OZH}	B port	V_{CC} (3.3 V) = 3.45 V,	V _{CC} (5 V) = 5.25 V,	V _O = 1.5 V		10	μA	
	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V _O = 0		-1	^	
I _{OZL}	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V _O = 0.65 V		-10	μA	
				Outputs high		1		
I _{CC} (3.3 V)	A or B	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = V_{CC} (3.3 V) or GND ⁽³⁾ , V	$V) = 5.25 \text{ V}, I_0 = 0,$ $V_1 = V_{} \text{ or } GND^{(4)}$	Outputs low		5	mA	
(0.0 1)	port	V1 = VCC (0.0 V) 01 0142 × , V	- V OF GIVE	Outputs disabled		1		
				Outputs high		120		
I _{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = $V_{L} = V_{CC}$ (3.3 V) or GND ⁽³⁾ , V	$V) = 5.25 \text{ V}, I_0 = 0,$ $V = V = \text{ or } GND^{(4)}$	Outputs low		120	mA	
(0 1)	port	V1 = VCC (0.0 V) 01 0142 ··· , V	= V OF GIVE	Outputs disabled		120		
Δl _{CC} (3.	3 V) ⁽⁵⁾	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) Other A-port or control inputs		r control input at 2.7 V,		1	mA	
C _i	Control inputs	V _I = 3.15 V or 0				4	pF	
C	A port	V _O = 3.15 V or 0				8.5	~F	
C _{io}	B port	V _O = 1.5 V or 0		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	8	pF		

All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to (2) another.

This is the V_I for A-port or control inputs. This is the V_I for B port.

⁽⁵⁾ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted) (see Figure 1)

	·		MIN	MAX	UNIT		
f _{clock}	Clock frequency			85	MHz		
	Pulse duration	LEAB or LEBA high	3.3				
t _w	Pulse duration	CLKAB or CLKBA high or low	5.7		ns		
		A before CLKAB↑	1				
		B before CLKBA↑	1.8				
t _{su} Se	Output Care	A before LEAB↓	0.5		20		
	Setup time	B before LEBA↓	1.2		ns		
		CEAB before CLKAB↑	1.2				
		CEBA before CLKBA↑	1.4				
		A after CLKAB↑	1.9				
		B after CLKBA↑	0.5				
	Halden	A after LEAB↓	2.7				
t _h	Hold time	B after LEBA↓	3.5		ns		
		CEAB after CLKAB↑	1.2				
		CEBA after CLKBA↑	1.1				

Switching Characteristics

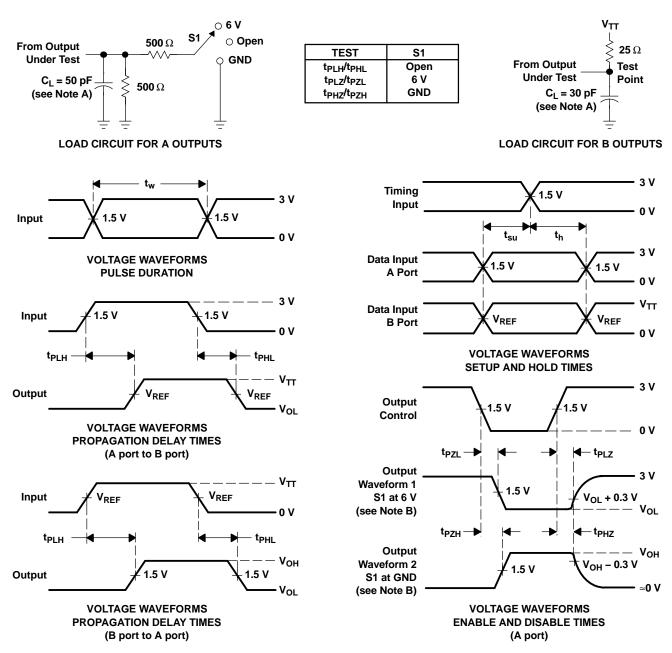
over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP(1)	MAX	UNIT	
f _{max}			85		MHz	
t _{PLH}	A	В	2.5	6.9	20	
t _{PHL}	^	Б	2.5	6.9	ns	
t _{PLH}	LEAB	В	3.2	7.3	ns	
t _{PHL}	LEAD	Б	3.2	7.3	115	
t _{PLH}	CLKAB	В	3.4	7.8	20	
t _{PHL}	CLRAB	Б	3.4	7.8	ns	
t _{en}	OEAB	В	2.8	7	20	
t _{dis}	OEAB	Б	2.8	7	ns	
t _r	Transition time, B or	utputs (20% to 80%)	2.6		ns	
t _f	Transition time, B or	utputs (80% to 20%)	2.6		ns	
t _{PLH}	В	А	1.5	5.7		
t _{PHL}	В	A	1.5	5.7	ns	
t _{PLH}	LEBA	А	1.8	5.7	20	
t _{PHL}	LEBA	A	1.8	5.7	ns	
t _{PLH}	CLKBA	٨	2.3	5.5		
t _{PHL}	CLKBA	А	2.3	5.5	ns	
t _{en}	ОЕВА	۸	1.8	6.1	20	
t _{dis}	OEDA	A	1.8	6.1	ns	

⁽¹⁾ All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25 °C.



PARAMETER MEASUREMENT INFORMATION



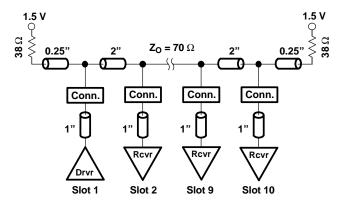
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



Distributed-Load Backplane Switching Characteristics

The previous switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to an RLC circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.



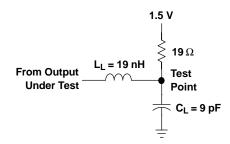


Figure 3. Medium-Drive RLC Network

Figure 2. Medium-Drive Test Backplane

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5 \text{ V}$ and $V_{RFF} = 1 \text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP(1)	UNIT	
f _{max}			85	MHz	
t _{PLH}	۸	В	3.6	no	
t _{PHL}	Α	D	3.6	ns	
t _{PLH}	LEAB	В	4.3	ns	
t _{PHL}	LLAB	J.	4.3	115	
t _{PLH}	CLKAB	В	4.4	20	
t _{PHL}	CLNAB	D	4.4	ns	
t _{en}	OEAB	В	4.1	ns	
t _{dis}	OEAB	D	4.3		
t _r	Rise time, B outpo	uts (20% to 80%)	1.4	ns	
t _f	Fall time, B outpu	2.1	ns		

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.





20-Jul-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74GTLPH16612DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74GTLPH16612DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74GTLPH16612GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74GTLPH16612GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH16612DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH16612DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH16612GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH16612DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74GTLPH16612GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH16612DLR	SSOP	DL	56	1000	346.0	346.0	49.0
SN74GTLPH16612GR	TSSOP	DGG	56	2000	346.0	346.0	41.0

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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