# SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D - DECEMBER 1988 - REVISED APRIL 2003

 Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V 28

- Very Low Power Consumption . . .5 mW Typ
- Wide Driver Supply Voltage . . . ±4.5 V to ±15 V
- Driver Output Slew Rate Limited to 30 V/μs Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1-μs Noise Filter

#### SN65C1154...N PACKAGE SN75C1154 . . . DW. N. OR NS PACKAGE (TOP VIEW) 20 🛮 V<sub>CC</sub> $V_{DD}$ 1RA 🛮 2 19 1 1RY 18 🛮 1DA 1DY [] 3 2RA **∏** 4 17 **∏** 2RY 2DY **∏** 5 16 2DA 15 3RY 3RA 🛮 6 3DY 🛮 7 14 ¶ 3DA 4RA **∏** 8 13 **∏** 4RY 12 **]** 4DA 4DY 🛮 9 11 GND

#### description/ordering information

The SN65C1164 and SN75C1154 are low-power BiMOS devices containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices are designed to conform to TIA/EIA-232-F. The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/ $\mu$ s and the receivers have filters that reject input noise pulses of shorter than 1  $\mu$ s. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP (N)	Tube of 20	SN65C1154N	SN65C1154N
	PDIP (N)	Tube of 20	SN75C1154N	SN75C1154N
0°C to 70°C	SOIC (DW)	Tube of 25	SN75C1154DW	SN75C1154
0010700	SOIC (DVV)	Reel of 2500	SN75C1154DWR	311/30/1134
	SOP (NS)	Reel of 2000	SN75C1154NSR	SN75C1154

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



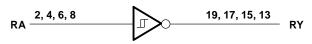
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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## logic diagram (positive logic)

Typical of Each Receiver

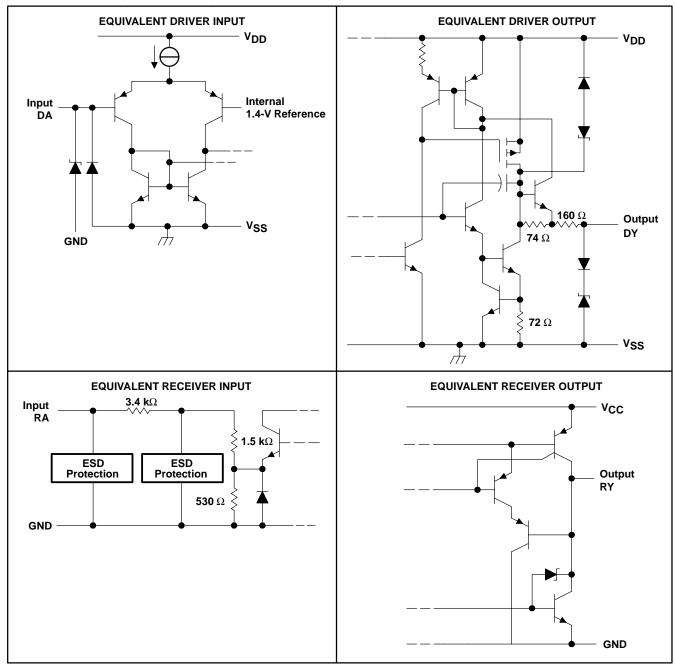


**Typical of Each Driver** 





# schematics of inputs and outputs



Resistor values shown are nominal.

# SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V <sub>DD</sub> (see Note 1)	15 V
V <sub>SS</sub>	
V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> : Driver	$V_{SS}$ to $V_{DD}$
Receiver	–30 V to 30 V
Output voltage range, VO:Driver	
Receiver	0.3 V to (V <sub>CC</sub> + 0.3 V)
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3):	DW package 58°C/W
	N package 69°C/W
	NS package 60°C/W
Operating virtual junction temperature, T <sub>J</sub>	
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10	seconds 260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage s are with respect to the network GND terminal.
  - 2. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

			MIN	NOM	MAX	UNIT
$V_{DD}$	Supply voltage		4.5	12	15	V
VSS	V <sub>SS</sub> Supply voltage				-15	V
Vcc	Supply voltage		4.5	5	6	V
١/،	Input voltage	Driver	V <sub>SS</sub> + 2		$V_{DD}$	V
٧ <sub>I</sub>	input voitage	Receiver			±25	v
VIH	High-level input voltage	Driver	2			V
V <sub>IL</sub>	Low-level input voltage	Driver			0.8	٧
ЮН	High-level output current	Receiver			-1	mA
loL	High-level output current	Receiver			3.2	mA
т.	Operating free-air temperature	SN65C1154	-40		85	°C
TA	Operating free-air temperature SN75C1154		0		70	



#### **DRIVER SECTION**

# electrical characteristics over operating free-air temperature range, $V_{DD}$ = 12 V, $V_{SS}$ = –12 V, $V_{CC}$ = 5 V $\pm 10\%$ (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS		MIN	TYP†	MAX	UNIT
Va	High-level output voltage	$V_{IL} = 0.8 V,$	$R_L = 3 k\Omega$ ,	$V_{DD} = 5 V$ ,	$V_{SS} = -5 V$	4	4.5		V
VOH	r light-level output voltage	See Figure 1		$V_{DD} = 12 V$ ,	$V_{SS} = -12 \text{ V}$	10	10.8		٧
\/o!	Low-level output voltage	V <sub>IH</sub> = 2 V,	$R_L = 3 k\Omega$ ,	$V_{DD} = 5 V$ ,	$V_{SS} = -5 V$		-4.4	-4	V
VOL	(see Note 4)	See Figure 1		$V_{DD} = 12 V$ ,	$V_{SS} = -12 \text{ V}$		-10.7	-10	V
lн	High-level input current	V <sub>I</sub> = 5 V,	See Figure 2					1	μΑ
Ι <sub>Ι</sub> L	Low-level input current	$V_{I} = 0,$	See Figure 2					-1	μΑ
IOS(H)	High-level short-circuit output current‡	V <sub>I</sub> = 0.8 V,	$V_O = 0$ or $V_{SS}$ ,	See Figure 1		-7.5	-12	-19.5	mA
IOS(L)	Low-level short-circuit output current‡	V <sub>I</sub> = 2 V,	$V_O = 0$ or $V_{DD}$ ,	See Figure 1		7.5	12	19.5	mA
Inn	Supply current from VDD	No load,		$V_{DD} = 5 V$ ,	$V_{SS} = -5 V$		115	250	^
IDD	Supply current from VDD	All inputs at 2 V	/ or 0.8 V	$V_{DD} = 12 V$ ,	$V_{SS} = -12 \text{ V}$		115	250	μΑ
loo	Supply current from VSS	No load,	No load,		$V_{SS} = -5 V$		-115	-250	^
Iss	Supply current from VSS	All inputs at 2 V or 0.8 V		V <sub>DD</sub> = 12 V,	V <sub>SS</sub> = -12 V		-115	-250	μΑ
ro	Output resistance	$V_{DD} = V_{SS} = V_{DD}$	$V_{CC} = 0$ , $V_{O} = -2$	2 V to 2 V,	See Note 5	300	400		Ω

<sup>†</sup> All typical values are at  $T_A = 25^{\circ}C$ .

NOTES: 4. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

5. Test conditions are those specified by TIA/EIA-232-F.

# switching characteristics, $V_{DD}$ = 12 V, $V_{SS}$ = –12 V, $V_{CC}$ = 5 V ±10%, $T_A$ = 25°C (see Figure 3)

	PARAMETER	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output§	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	CL = 15 pF		1.2	3	μs
tPHL	Propagation delay time, high- to low-level output§	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	CL = 15 pF		2.5	3.5	μs
tTLH	Transition time, low- to high-level output¶	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	CL = 15 pF	0.53	2	3.2	μs
tTHL	Transition time, high- to low-level output¶	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	CL = 15 pF	0.53	2	3.2	μs
tTLH	Transition time, low- to high-level output#	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	C <sub>L</sub> = 2500 pF		1	2	μs
tTHL	Transition time, high- to low-level output#	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	C <sub>L</sub> = 2500 pF		1	2	μs
SR	Output slew rate	$R_L = 3 \text{ to } 7 \text{ k}\Omega$	CL = 15 pF	4	10	30	V/μs

<sup>§</sup> tpHL and tpLH include the additional time due to on-chip slew rate control and are measured at the 50% points.



<sup>‡</sup> Not more than one output should be shorted at one time.

<sup>¶</sup> Measured between 10% and 90% points of output waveform

<sup>#</sup> Measured between 3 V and –3 V points of output waveform (TIA/EIA-232-F conditions) with all unused inputs tied either high or low

#### **RECEIVER SECTION**

## electrical characteristics over operating free-air temperature range, $V_{DD} = 12 \text{ V}$ , $V_{SS} = -12 \text{ V}$ , $V_{CC}$ = 5 V ± 10% (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT	
V <sub>IT+</sub>	Positive-going input threshold voltage	See Figure 5		1.7	2.1	2.55	٧	
V <sub>IT</sub> –	Negative-going input threshold voltage	See Figure 5		0.65	1	1.25	٧	
V <sub>hys</sub>	Input hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )			600	1000		mV	
		$V_I = 0.75 \text{ V}, \qquad I_{OH} = -20 \mu\text{A},$	See Figure 5 and Note 6	3.5				
VOH	High-level output voltage	V 0.75 V 1 4 4	V <sub>CC</sub> = 4.5 V	2.8	4.4		V	
		$V_I = 0.75 \text{ V},  I_{OH} = -1 \text{ mA},$ See Figure 5	V <sub>CC</sub> = 5 V	3.8	4.9		V	
		ess i igais s	V <sub>CC</sub> = 5.5 V	4.3	5.4			
VOL	Low-level output voltage	$V_I = 3 V$ , $I_{OL} = 3.2 \text{ mA}$ ,	See Figure 5		0.17	0.4	V	
lu i	High lovel input ourrent	V <sub>I</sub> = 25 V		3.6	4.6	8.3	m ^	
ΊΗ	High-level input current	V <sub>I</sub> = 3 V	0.43	0.55	1	mA		
l	Low-level input current	V <sub>I</sub> = -25 V		-3.6	<b>–</b> 5	-8.3	mA	
ΙIL	Low-level input current	V <sub>I</sub> = −3 V		-0.43	-0.55	-1	ША	
IOS(H)	Short-circuit output at high level	$V_I = 0.75 \text{ V},  V_O = 0,$	See Figure 4		-8	-15	mA	
los(L)	Short-circuit output at low level	$V_I = V_{CC},$ $V_O = V_{CC},$	See Figure 4		13	25	mA	
laa	Supply current from V <sub>CC</sub>	No load,	$V_{DD} = 5 \text{ V}, \qquad V_{SS} = -5 \text{ V}$		400	600		
ICC	and bis content none ACC	All inputs at 0 or 5 V	$V_{DD} = 12 \text{ V},  V_{SS} = -12 \text{ V}$		400	600	μΑ	

 $^{\dagger}$  All typical values are at  $T_A = 25^{\circ}$ C. NOTE 6: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

## switching characteristics, $V_{DD}$ = 12 V, $V_{SS}$ = -12 V, $V_{CC}$ = 5 V $\pm$ 10%, $T_A$ = 25°C

	PARAMETER	Т	EST CONDITIO	NS	MIN	TYP	MAX	UNIT
<sup>t</sup> PLH	Propagation delay time, low- to high-level output	C <sub>L</sub> = 50 pF,	$R_L = 5 k\Omega$ ,	See Figure 6		3	4	μs
<sup>t</sup> PHL	Propagation delay time, high- to low-level output	C <sub>L</sub> = 50 pF,	$R_L = 5 \text{ k}\Omega$ ,	See Figure 6		3	4	μs
<sup>t</sup> TLH	Transition time, low- to high-level output	$C_L = 50 \text{ pF},$	$R_L = 5 k\Omega$ ,	See Figure 6		300	450	ns
tTHL	Transition time, high- to low-level output	C <sub>L</sub> = 50 pF,	$R_L = 5 k\Omega$ ,	See Figure 6		100	300	ns
t <sub>w(N)</sub>	Duration of longest pulse rejected as noise‡	C <sub>L</sub> = 50 pF,	$R_L = 5 \text{ k}\Omega$		1		4	μs

 $<sup>^{\</sup>ddagger}$  The receiver ignores any positive- or negative-going pulse that is less than the minimum value of  $t_{W(N)}$  and accepts any positive- or negative-going pulse greater than the maximum of  $t_{W(N)}$ .



#### PARAMETER MEASUREMENT INFORMATION

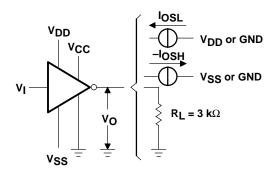


Figure 1. Driver Test Circuit  $(V_{OH}, V_{OL}, I_{OSL}, I_{OSH})$ 

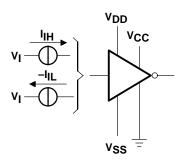
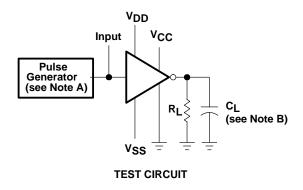
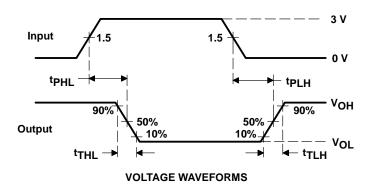


Figure 2. Driver Test Circuit (I<sub>IL</sub>, I<sub>IH</sub>)





NOTES: A. The pulse generator has the following characteristics:  $t_W$  = 25  $\mu$ s, PRR = 20 kHz,  $Z_O$  = 50  $\Omega$ ,  $t_f$  =  $t_f$  < 50 ns.

B. C<sub>L</sub> includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

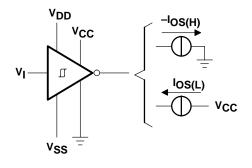


Figure 4. Receiver Test Circuit (I<sub>OSH</sub>, I<sub>OSL</sub>)

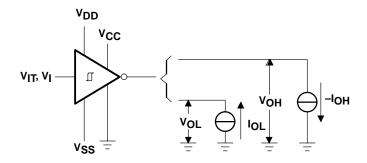
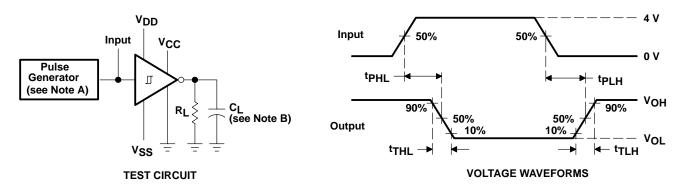


Figure 5. Receiver Test Circuit (V<sub>IT</sub>, V<sub>OL</sub>, V<sub>OH</sub>)

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics:  $t_W$  = 25  $\mu$ s, PRR = 20 kHz,  $Z_O$  = 50  $\Omega$ ,  $t_\Gamma$  =  $t_f$  < 50 ns.
  - B. C<sub>L</sub> includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms





28-Aug-2010

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN65C1154DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN65C1154DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN65C1154N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
SN65C1154NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
SN75C1154DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN75C1154DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN75C1154DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN75C1154DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75C1154DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75C1154DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75C1154N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
SN75C1154NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



### PACKAGE OPTION ADDENDUM

28-Aug-2010

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

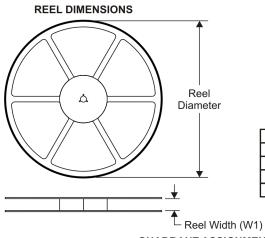
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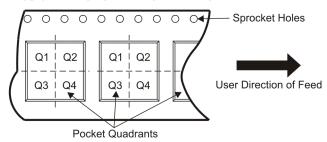
## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C1154DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 23-Jul-2010



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C1154DWR	SOIC	DW	20	2000	346.0	346.0	41.0

# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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