CEL NEC'S LOW POWER GPS RF RECEIVER BIPOLAR ANALOG + INTEGRATED CIRCUIT

UPB1009K

DESCRIPTION

The μ PB1009K is a silicon monolithic IC developed for GPS receivers. This IC integrates a full VCO, second IF filter, 4-bit ADC, and digital control interface to reduce cost and mounting space. In addition, its power consumption is low.

Moreover, use of a TCXO with frequency of 16.368 MHz/16.384 MHz, 14.4 MHz, 19.2 MHz, or 26 MHz switchable with an on-chip divider is possible.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

FEATURES

•	Double conversion	: frefin = 16.368 MHz, f1stlFin = 61.380 MHz, f2ndlFin = 4.092 MHz
		: frefin = 14.4, 16.384, 19.2, 26 MHz, f1stlFin = 62.980 MHz, f2ndlFin = 2.556 MHz
•	Multiple system clocks	: On-chip switchable frequency divider (1/N = 100, 3/256, 9/1024, 65/4096)
•	A/D converter	: On-chip 4-bit A/D converter
•	High-density RF block	: On-chip VCO tank circuit and 2ndIF filter
•	Supply voltage	: $V_{CC} = 2.7$ to 3.3 V
•	Low current consumption	: Icc = 26.0 mA TYP. @ Vcc = 3.0 V, N = 100
•	High-density surface mountable	: 44-pin plastic QFN

APPLICATIONS

- Consumer use GPS receiver of reference frequency 16.368 MHz, 2nd IF frequency 4.092 MHz
- Consumer use GPS receiver of reference frequency 14.4, 16.384, 19.2, 26 MHz, 2ndIF frequency 2.556 MHz

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

ORDERING INFORMATION

Part Number	Package	Supplying Form
μΡΒ1009Κ-Ε1-Α	44-pin plastic QFN	 12 mm wide embossed taping Pin 1 indicates pull-out direction of tape Qty 1.5 kpcs/reel, Dry pack specification

Remark To order evaluation samples, contact your nearby sales office. Part number for sample order: μ PB1009K

Туре	Part Number	Functions (Frequency unit: MHz)	Vcc (V)	lcc (mA)	CG (dB)	Package	Status
Clock Frequency Specific 1 chip IC	μ ₽ Β1009Κ	Pre-amplifier + RF/IF down- converter + PLL synthesizer REF = 16.368 1stIF = 61.380/2ndIF = 4.092 REF = 14.4, 16.384, 19.2, 26 1stIF = 62.980/2ndIF = 2.556 On-chip 4-bit ADC	2.7 to 3.3	26.0		44-pin plastic QFN	New Device
	μPB1008K	LNA + Pre-amplifier + RF/IF down-converter + PLL synthesizer REF = 27.456 1stIF = 175.164/2ndIF = 0.132 On-chip 2-bit ADC	2.7 to 3.3	18.0	100 to 120	36-pin plastic QFN	
	μΡΒ1007K	Pre-amplifier + RF/IF down- converter + PLL synthesizer REF = 16.368 1stIF = 61.380/2ndIF = 4.092	2.7 to 3.3	25.0	100 to 120	36-pin plastic QFN	Available
	μΡΒ1005K	REF = 16.368 1stlF = 61.380/2ndlF = 4.092				36-pin plastic QFN	

PRODUCT LINE-UP ($T_A = +25^{\circ}C$, $V_{CC} = 3.0 V$)

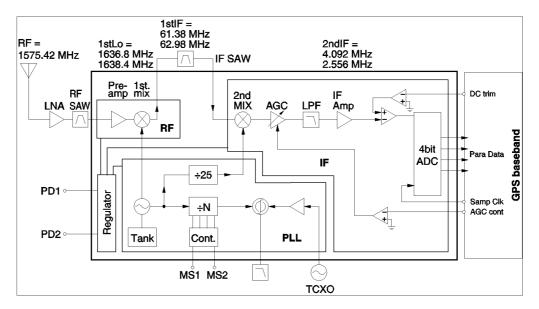
Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

SYSTEM APPLICATION EXAMPLE

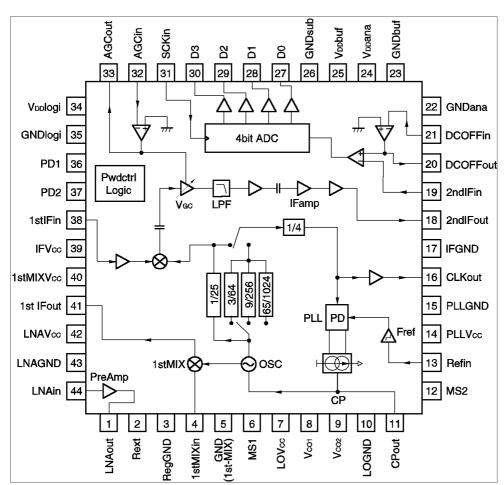
GPS receiver RF block diagram

PD1 and PD2 in the figure are Power Save Mode control pins.

 $\mathsf{MS1}$ and $\mathsf{MS2}$ in the figure are TXCO (GPS, W-CDMA, PDC, GSM) control pins.



Caution This diagram schematically shows only the μ PB1009K's internal functions on the system. This diagram does not present the actual application circuits.



PIN CONNECTION AND INTERNAL BLOCK DIAGRAM

PIN EXPLANATION

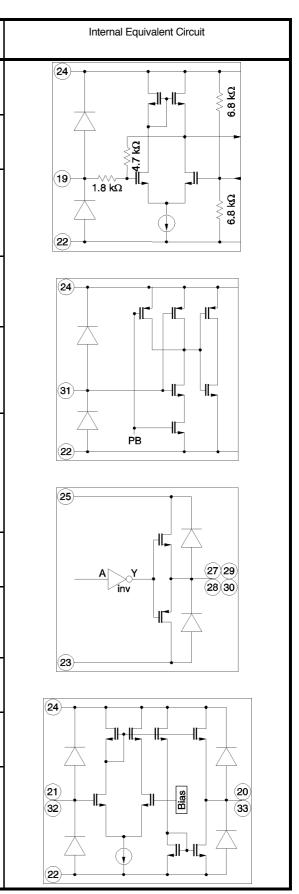
Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
1	PreAMPout	Output pin of preamplifier.	1 42
2	Rext	Connect a resistor for the reference constant- current power supply to this pin. Ground this pin at 22 k Ω .	
3	RegGND	Ground pin for regulator.	
42	PreAmpVcc	Power supply voltage pin for preamplifier. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.	
43	PreAmpGND	Ground pin of preamplifier.	
44	PreAmpin	Input pin of preamplifier.	
4	1stMIXin	1stMIX input pin.	
5	1stMIXGND	Ground pin for first MIX.	
40	1stMIXVcc	Power supply voltage pin for RF mixer. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.	Gibert Cell
41	1stlFout	Output pin of RF mixer. Insert an IFSAW filter between this pin and pin 37. The VCO oscillation signal can be monitored on this pin.	4 Bias 5

Pin No.	Pin Name	Fu	Inction and	Application	Internal Equivalent Circuit
6 12	MS1 MS2	Low : 0 to 0.3 (V)	MS1 : L MS2 : L	TCXO : 16.368, 16.384 MHz	
		High : Vcc – 0.3 to	MS1 : L MS2 : H	TCXO : 19.2 MHz	
		Vcc (V)	MS1 : H MS2 : L	TCXO : 14.4 MHz	
			MS1 : H MS2 : H	TCXO : 26 MHz	
11	CPout	R and C to thi	is pin to set	np. Connect external a dumping factor and cy (Isink = Isource = 0.45	
13	Refin		ence transr	ut pin. Connect an nitter (such as	
14	PLLVcc	Power supply Connect a by reduce the hig	pass capac	itor to this pin to	
15	PLLGND	Ground pin of	PLL.		
16	CLKout	Clock (frcxo)	output pin (IC test pin).	from divider

15

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
7	LoVcc	Power supply voltage pin of VCO. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.	VCO out
8 9	VCO1 VCO2	IC test pin. Leave this pin open when the μ PB1009K is mounted on board.	8 + VCO cont + VCO cont
10	LoGND	Ground pin of VCO.	
17	IFGND	Ground pin of IF block.	
18	2ndlFout	Output pin of IF amplifier.	
38	1stlFin	Input pin of second IF mixer.	
39	IFVcc	Power supply voltage pin of IF block.	Bias 55 17 17

Pin No.	Pin Name	Function and Application
19	2ndlFin	Input pin of ADC buffer amplifier.
20	DCOFFout	Output pin of DC trimming OP amplifier.
21	DCOFFin	DC trimming pulse input pin. Connect this pin to pin 20 via a capacitor to convert an input pulse signal into DC.
22 23	GNDana GNDbuf	Ground pin for OP amplifier and ADC power supply.
24	Vodana	Power supply pin for OP amplifier and ADC comparator.
25	V⊳⊳buf	Power supply pin for output driver amplifier of ADC. Connect this pin to the ground pin of the A/D converter via a bypass capacitor to reduce the high-frequency impedance.
26	GNDsub	Ground pin of CMOS substrate.
27 28 29 30	D0 D1 D2 D3	Digital signal output pins. LSB = D0, MSB = D3
31	SCKin	Sampling clock signal input pin.
32	AGCin	AGC control pulse signal input pin.
33	AGCout	AGC control signal output pin.



Pin No.	Pin Name	Fur	nction and A	Application	Internal Equivalent Circuit
34	Vddlogi	Power supply logic.	voltage pin	for power control	34
35	GNDlogi	Ground pin for	power cor	ntrol logic.	
36 37	PD1 PD2	Low : 0 to 0.3 (V)	PD1 : L PD2 : L	Sleep mode (all circuits off).	36
		High : Vcc – 0.3 to	PD1 : L PD2 : H	Warm-up mode (PLL on).	37
		Vcc (V)	PD1 : H PD2 : L	Calibration mode (PLL + IF + AD C on).	
			PD1 : H PD2 : H	Active mode (all circuits on).	35

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	Vcc	$T_A = +25^{\circ}C$	3.6	V
Total Circuit Current	ICCTotal	$T_A = +25^{\circ}C$	100	mA
Power Dissipation	PD	T _A = +25°C Note	266	mW
Operating Ambient Temperature	Ta		-40 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

Note Mounted on double-sided copper-clad 50 \times 50 \times 1.6 mm epoxy glass PWB

RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc	2.7	3.0	3.3	V
Operating Ambient Temperature	TA	-30	+25	+85	°C
RF Input Frequency	fRFin	-	1 575.42	-	MHz
1st LO Oscillating Frequency	f 1stLOin	-	1 636.8/1 638.4	-	MHz
1st IF Input Frequency	f1stlFin	-	61.38/62.98	-	MHz
2nd LO Input Frequency	f2ndLOin	-	65.472/65.536	-	MHz
2nd IF Input Frequency	f 2ndlFin	-	4.092/2.556	-	MHz
Reference Input/Output Frequency	freFin freFout	-	тсхо	-	MHz
Clock mode control voltage (Low Level)	VIL1	0	-	0.3	V
Clock mode control voltage (High Level)	VIH1	Vcc - 0.3	-	Vcc	V
Power-down control voltage (Low Level)	VIL2	0	-	0.3	V
Power-down control voltage (High Level)	VIH2	Vcc - 0.3	-	Vcc	V

POWER-DOWN CONTROL MODE

The μ PB1009K consists of an RF block, an IF block, and a PLL block. By controlling reduction of power to each block (by applying a voltage to the PD1 and PD2 pins), the following four modes can be used.

Mode	Mode Name	Test Conditions		RF Block	IF Block	PLL Block
No.		PD1	PD2		(IF + ADC)	
1	Active mode	L	Н	ON	ON	ON
2	Calibration mode	н	Н	OFF	ON	ON
3	Warm-up mode	н	L	OFF	OFF	ON
4	Sleep mode	L	L	OFF	OFF	OFF

Caution To use only the active mode and sleep mode, fix PD1 to L and select the desired mode with PD2.

REFERENCE CLOCK CONTROL MODE

The divided frequency can be selected as follows so that it can be shared with the TCXO of each system.

TCXO Frequency	Test Conditions		1/N	Phase Comparison Frequency
	PD1	PD2		
16.368 MHz (GPS) 16.384 MHz (GPS)	L	L	1/100	16.368 MHz 16.384 MHz
19.2 MHz (W-CDMA)	L	Н	3/256	19.2 MHz
14.4 MHz (PDC)	Н	L	9/1024	14.4 MHz
26 MHz (GSM)	Н	Н	65/4096	26 MHz

Caution When the reference clock frequency is 16.368 MHz, the 1stIF frequency and 2ndIF frequency are 61.38 MHz and 4.092 MHz, respectively. They are respectively 62.98 MHz and 2.556 MHz in all other cases.

ELECTRICAL CHARACTERISTICS (TA = +25°C, Vcc = 3.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit		
Rest current of overall IC in each mode		Rest status without input signal, including sampling clock. MS1 = L, MS2 = L						
Sleep mode Note	ls	PD1 = L, PD2 = L	1.3	2.2	3.5	mA		
Warm-up mode	lw	PD1 = H, PD2 = L	10.5	13.0	15.5	mA		
Calibration mode	lc	PD1 = H, PD2 = H	18.0	22.0	25.3	mA		
Active mode	la	PD1 = L, PD2 = H	22.1	26.0	30.0	mA		
Rest current of PLL block in each clock mode		PLL block. Overall current in calibration mode e (MS1 = L, MS2 = L). PD1 = H, PD2 = L.	e and active	e mode incr	eases from	that in		
Current when 1/100 divider is used	lw1	MS1 = L, MS2 = L	5.3	6.5	7.6	mA		
Current when 256/3 divider is used	lw2	MS1 = L, MS2 = H	9.7	11.3	12.6	mA		
Current when 1024/9 divider is used	lwз	MS1 = H, MS2 = L	10.2	12.1	13.5	mA		
Current when 4096/65 divider is used	lw4	MS1 = H, MS2 = H	10.4	12.3	13.9	mA		
Maximum mode control pin current								
6 pin	MS1	H application	-	-	20	μA		
		L application	-20	-	-	μA		
12 pin	MS2	H application	-	-	20	μΑ		
		L application	-20	-	-	μΑ		
36 pin	PD1	H application	-	-	1	μΑ		
		L application	–1	-	-	μA		
37 pin	PD2	H application	-	-	1	μΑ		
		L application	-1	-	-	μA		
<pre-amplifier></pre-amplifier>	frin = 1 57	5.42 MHz						
Circuit Current 1	Icc1	No Signals, 1-pin current	1.9	2.3	2.7	mA		
Power Gain	Glna	P _{RFin} = -40 dBm	12.5	15.0	17.5	dB		
Noise Figure	NFlna	f _{RFin} = 1 575 MHz	-	3.0	3.5	dB		
Saturated Output Power	Po(sat)lna	$P_{\text{RFin}} = -10 \text{ dBm}$	-4.0	-2.7	_	dBm		
Input 1dB Compression Level	Plna-1	f _{RFin} = 1 575.42 MHz	-25	-21.8	_	dBm		
Input 3rd Order Intercept Point	IIP3lna	f _{RFin} = 1 575.42 MHz, 1 576.42 MHz	-12	-9.5	-	dBm		
Input Inpedance	Zinlna	Calculated from S-parameter where input DC cut capacitance = 1 nF, output load L =	-	11.2 – j21.5	-	Ω		
Output Inpedance	ZoutLNA	100 n, and DC cut capacitance = 1 nF	-	16.4 – j136.6	-	Ω		

Note Most of the current flows into the ADC ladder resistor (V_{DD}ana ♦ GNDana) in the sleep mode, and the sleep mode current between other V_{CC} (V_{DD}) and GND is 10 µA maximum.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, Vcc = 3.0 V)

Parameter	Symbol	Test C	onditions	MIN.	TYP.	MAX.	Unit
<rf mixer=""></rf>	fr⊧ = 1 575	.42 MHz, f1stLOin = 1 63	6.80 MHz, f1stlF = 61.38	MHz			
Circuit Current 2	Icc2	No Signals, 40 pin current		2.0	2.5	3.0	mA
RF Conversion Gain	CGRF	PRFMIXin = -40 dBm		14.0	16.1	19.0	dB
Noise Figure	S SBN Fremik	SSBNF = 10*log (2*I –1) MHz	OSBNF (Linear value)	_	12.8	16.0	dB
Maximum IF Output	Po(SAT) REMIX	$P_{\text{RFMIXin}} = -10 \text{ dBm}$		-4.0	-0.8	_	dBm
Input 1dB Compression Level	PRFMIX-1	frfmixin = 1 575.42 MH	łz	-29.0	-25.5	-	dBm
Input 3rd Order Intercept Point	ШРзвеміх	fremixin = 1 575.42 MH f1stL0 = 1 636.8 MHz	lz, 1 576.42 MHz	-19.0	-17.2	-	dBm
LO Leakage to IF Pin	LO⊫	Leakage of 1 636.8 M		-	-34.5	-30	dBm
LO Leakage to RF Pin	LORF	VCO oscillates corre	ctly.	-	-54.7	-30	dBm
Input Inpedance	ZinMIX	Calculated from S-pa DC cut capacitance =		-	50.1 – j22.3	-	Ω
Output Inpedance	ZoutMIX	cut capacitance = 1 nF		-	57.3 + j2.6	-	Ω
<if ifamp="" lpf,="" mixer,=""></if>	$f_{1stFin} = 61.3$	38 MHz, f2ndL0in = 65.4	72 MHz, Z∟ = 2 kΩ				
Circuit Current 3	Іссз	No Signals, 39 pin cu	rrent	6.3	7.3	8.5	mA
IF Conversion Gain	CG (GV) IF	$V_{\text{AGC}} = 0.5 \text{ V}$		66.0	70.3	75.0	dB
		VAGC = 1.5 V		45.0	51.2	58.0	dB
		$V_{AGC} = 2.5 V$		19.5	26.4	33.5	dB
In Band Gain Fluctuation	⊿CG1	3.092 to 5.092 MHz		-	0.7	1.0	dB
Out Of Band Attenuation	⊿CG2	Gain difference at 4.0 MHz, VAGC = 0.5 V	92 MHz and 9.092	20.0	25.0	-	dB
Conversion Gain Range	CGRange	$V_{AGC} = 0$ to 2.5 V		32.5	43.9	-	dB
IF · SSB Noise Figure	NFIF	V _{AGC} = 0.5 V (at max	imum gain)	_	13.7	17.5	dB
Maximum 2ndIF Output	VO (SAT) F	$P_{in} = -50 \text{ dBm}, V_{AGC} =$	= 0.5 V	1.0	1.3	-	VPP
Input 1dB Compression Level	PIF-1	f1stlFin = 61.38 MHz	$V_{\text{AGC}} = 0.5 \text{ V}$	-70.5	-64.4	-	dBm
			$V_{\text{AGC}} = 1.5 \text{ V}$	-53.5	-44.9	-	dBm
		VAGC = 2.5 V		-37.0	-30.6	-	dBm
Input 3rd Order Intercept Point	IIРзг	f1stlFin1 = 61.28 MHz	$V_{AGC} = 0.5 V$	-56.0	-51.3	-	dBm
		f1stlFin2 = 61.38 MHz VAGC = 1.5 V		-38.0	-30.7	-	dBm
		f _{2ndLO} = 65.472 MHz V _{AGC} = 2.5 V		-27.0	-21.4	I	dBm
Input Inpedance	ZinIF	Calculated from S-parameter where input DC cut capacitance = 1 nF and output DC cut capacitance = 100 nF		_	69.3 – j4.8	-	Ω
Output Inpedance	ZoutIF			-	163 + j3.8	I	Ω

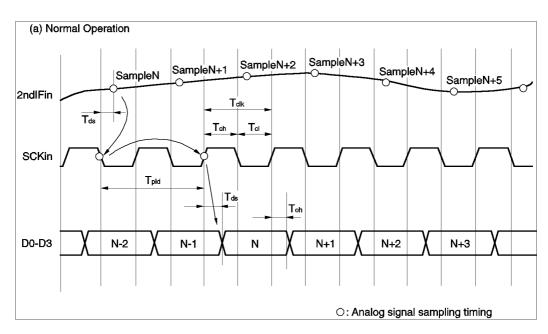
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
<pll synthesizer=""></pll>						
Circuit Current 4	Icc4	PLL, VCO current, MS1 = L, MS2 = L	8.0	9.5	10.6	mA
Charge Pump Output Current	Icpsink	V _{13 pin} = Vcc/2	-0.55	-0.45	-0.35	mA
	Icpsource		0.35	0.45	0.55	mA
Loop Filer Output (High Level)	Vон		Vcc-0.3	-	-	V
Loop Filer Output (Low Level)	Vol		-	-	0.2	V
Reference Input Level	VREFin		-	0.2	1.6	VPP
VCO Modulation Sensitivity	КV	Center frequency	-	100	-	MHz
VCO Control Voltage	VT	When PLL is Locked	0.5	1.3	2.0	V
C/N	C/N	⊿10 kHz	70.0	81.0	-	dBc/Hz
						
Circuit Current 5	lcc5		3.1	4.1	5.4	mA
Resolution	ResAD		-	4	-	bits
Sampling Clock	fs		-	-	20	MHz
Input Band Width	ADBW		5.1	-	-	MHz
Integral Non-linear Error	INL	DC characteristics	-	0.2	1.0	LSB
Signal-to-noise Ratio	SNR	IF = 5.17 MHz, fs = 20.48 MHz	22.0	25.3	-	dB
Signal-to-noise + Distortion Ratio	SINAD	IF = 5.17 MHz, fs = 20.48 MHz	20.0	25.1	-	dB
Number	ENOB	ENOB = (SINAD-1.763)/6.02	3.0	3.9	-	bits
Total Harmonic Distortion Ratio	THD	IF = 5.17 MHz, fs = 20.48 MHz Second-degree to fifth-degree distortion components	-	-40	-30	dBc

ELECTRICAL CHARACTERISTICS (TA = +25°C, Vcc = 3.0 V)

Remarks 1. Timing characteristics of ADC during normal operation

A buffer amplifier is internally inserted before the ADC core of the µPB1009K. The bias of this buffer amplifier is controlled by the signal input from the DC trim pin, and is used to eliminate the DC offset of the ADC. Because the ladder resistor of the ADC is directly connected between V_{DD}ana and GNDana, changes in V_{DD}ana affect the resolution of the ADC.

As illustrated in the operation timing chart below, the data of SampleN is pipeline delayed by 1.5 clocks during normal operation, and is output at the rising edge of the sample clock with output delay time Tod. When the operation is changed from normal operation to power-down operation, the status of the output data immediately before the power-down operation is retained (drive status).

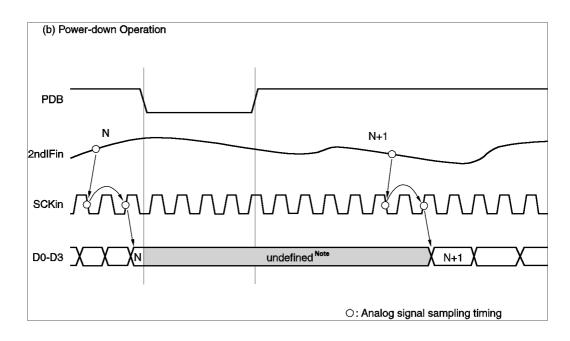


Symbol	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Tod	Output Delay	$C_{\text{L}} = 10 \text{ pF}, f_{\text{Clk}} = 19.2 \text{ MHz}$	-	-	12	ns
Tpld	Pipeline Delay		-	1.5	-	clock
Tds	Sampling Delay (Aperture Delay)		-	2	1	ns
Toh	Output Hold Time		2	-	-	ns

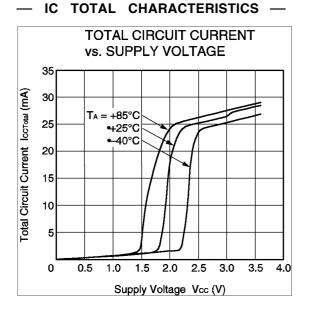
The following table shows each timing parameter for reference purposes.

Remarks 2. Power-down timing characteristics of ADC

The output code of the ADC of the μ PB1009K is undefined for 7.5 clocks after the power-down signal is cleared when the ADC returns from the power-down status to normal operation.

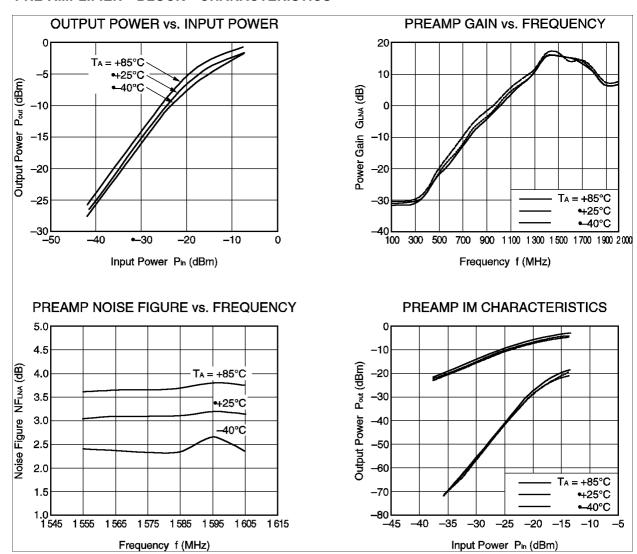


Note The output data is undefined from the start of the power-down operation to the 7.5th clock from the falling edge of the clock at which the power-down operation is cleared.



Remark The graphs indicate nominal characteristics.

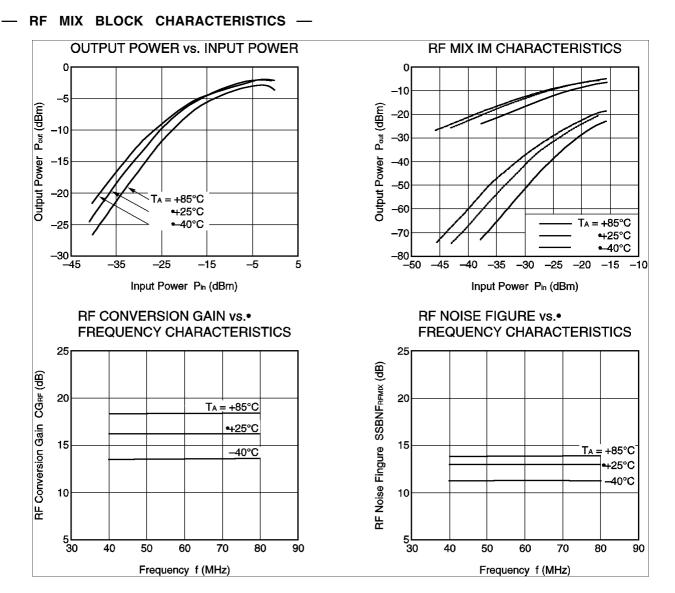




— PRE-AMPLIFIER BLOCK CHARACTERISTICS —

Remark The graphs indicate nominal characteristics.

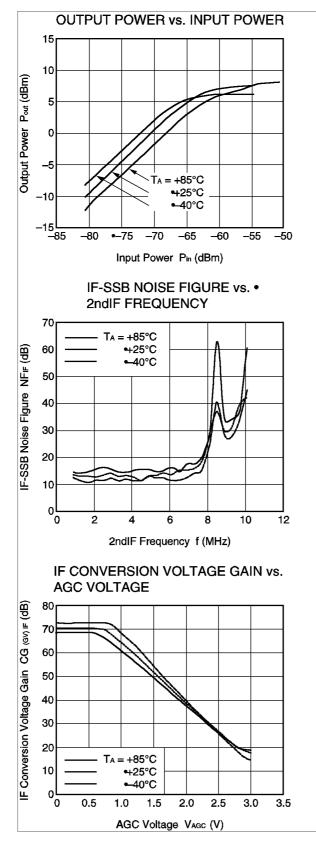


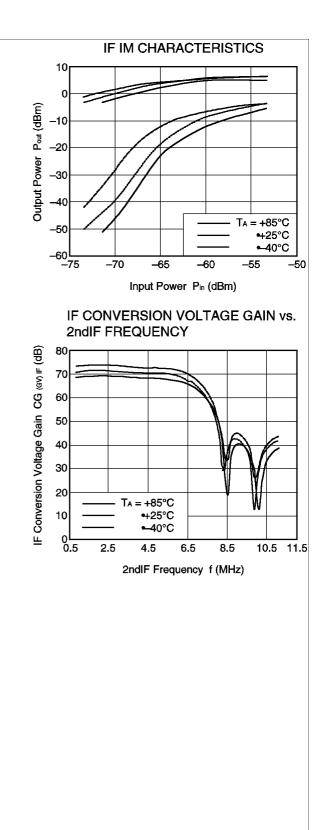


Remark The graphs indicate nominal characteristics.



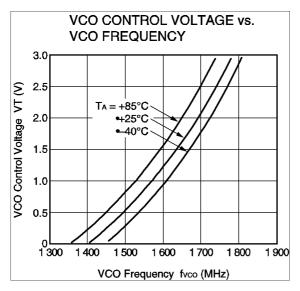
IF BLOCK CHARACTERISTICS -



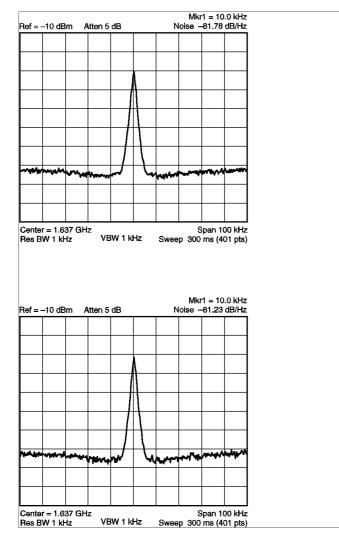


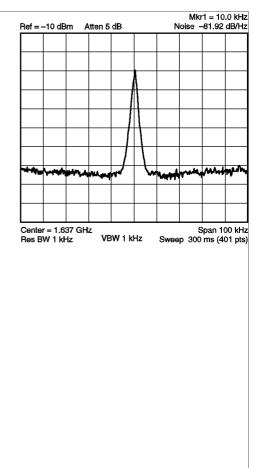
Remark The graphs indicate nominal characteristics.

— VCO MODULATION SENSITIVITY CHARACTERISTICS –

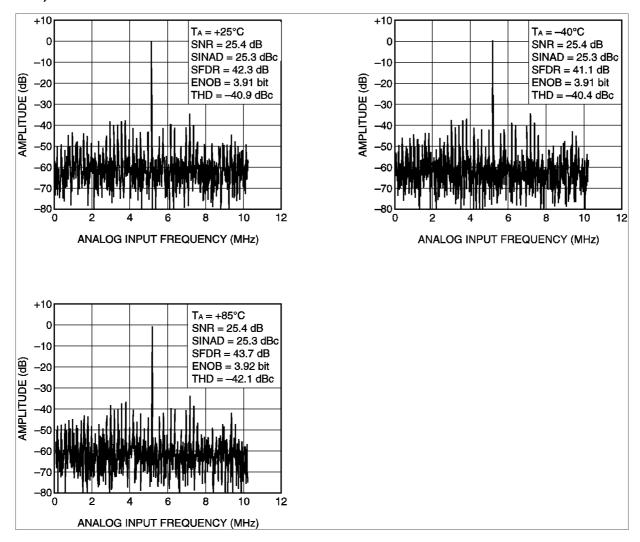


— C/N CHARACTERISTICS —





Remark The graphs indicate nominal characteristics.

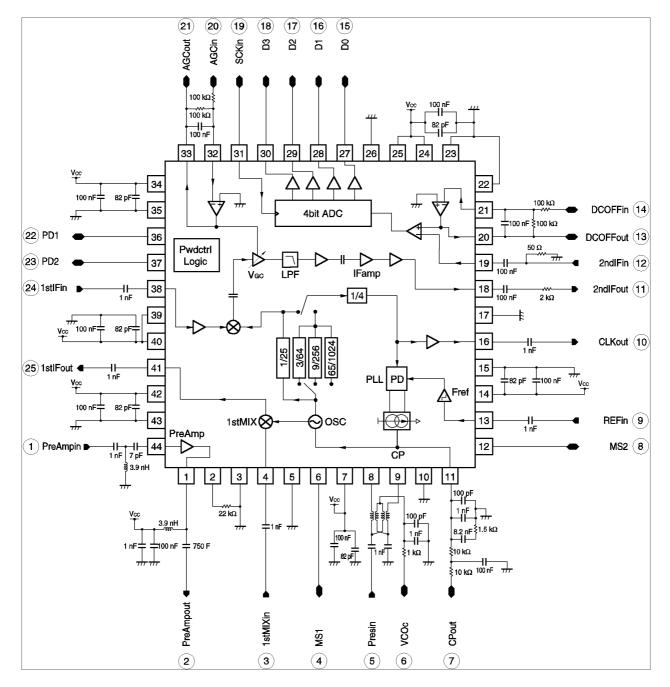


— SINAD CHARACTERISTICS OF A/D CONVERTOR (IFin = 5.17 MHz, SCLKin = 20.48 MHz) —

Remark The graphs indicate nominal characteristics.

CEL

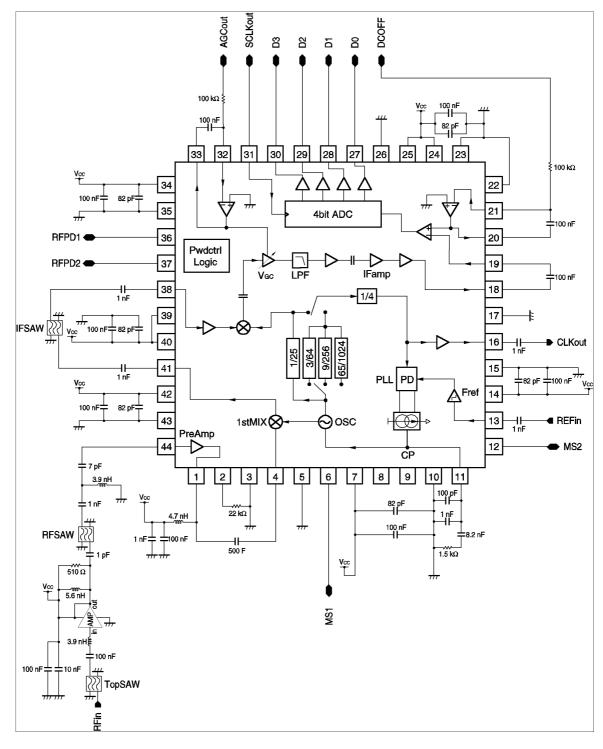
MEASUREMENT CIRCUIT



Pin No.	Pin Function	Pin Name	Pin No.	Pin Function	Pin Name
1	Preamplifier Input	PreAmpin	(14)	DC Offset Input	DCOFFin
2	Preamplifier Output	PreAmpout	15	Digital Signal Output Pin	D0
3	RF Mixer Input	1stMIXin	16		D1
4	MS1	MS1	17		D2
5	Prescaler Input	Presin	18		D3
6	VCO Power Control Pin	VCOc	19	Sampling Signal Input	SCKin
0	VT Measurement Pin (Charge Pump Output)	CPout	8	AGC Input	AGCin
8	MS2	MS2	21	AGC Control Voltage Output	AGCout
9	Reference Clock Input	REFin	2	PD1 Output (Default onboard : GND)	PD1
(10)	Clock Output	CLKout	3	PD1 Output (Default on board : Vcc)	PD2
(1)	2ndIF Output	2ndlFout	24	1stlF Input	1stlFin
(12)	2ndIF Input	2ndlFin	ෂ	1stIF Output	1stlFout
(13)	DC Offset Output	DCOFFout			

DESCRIPTION OF PINS OF TEST CIRCUIT

APPLICATION CIRCUIT



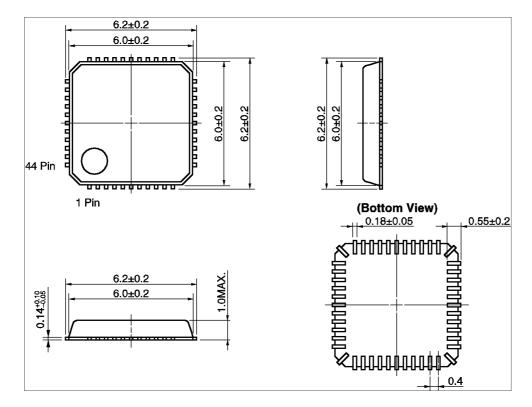
PD1	PD2	Power-down mode
0	0	Sleep mode (full off)
1	0	Warm-up mode (PLL on)
1	1	Calibration mode (PLL on)
0	1	Active mode (full on)

MS1	MS2	тсхо	Ν
0	0	16.368/16.384 MHz	100
0	1	19.2 MHz	256/3
1	0	14.4 MHz	1024/9
1	1	26.0 MHz	4096/65

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PACKAGE DIMENSIONS

44-PIN PLASTIC QFN (UNIT: mm)



Caution The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function. Consequently the island pins should not be soldered and should remain non-connection pins.

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent abnormal oscillation).
- (3) Keep the wiring length of the ground pins as short as possible.
- (4) Connect a bypass capacitor to the $V{\rm cc}$ pin.
- (5) High-frequency signal I/O pins must be coupled with the external circuit using a coupling capacitor.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	H\$350

Caution Do not use different soldering methods together (except for partial heating).

Life Support Applications

These NEC products are not intended for use in life support devices, appliances, or systems where the mahunction of these products can reasonably be expected to result in personal injury. The customers of CEL using or selling these products for use in such applications do so at their own risk and agree to fully indemnity CEL for all damages resulting from such improper use or sale.

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Subject: Compliance with EU Directives

CEL certifies, to its knowledge, that semiconductor and laser products detailed below are compliant with the requirements of European Union (EU) Directive 2002/95/EC Restriction on Use of Hazardous Substances in electrical and electronic equipment (RoHS) and the requirements of EU Directive 2003/11/EC Restriction on Penta and Octa BDE.

CEL Pb-free products have the same base part number with a suffix added. The suffix –A indicates that the device is Pb-free. The –AZ suffix is used to designate devices containing Pb which are exempted from the requirement of RoHS directive (*). In all cases the devices have Pb-free terminals. All devices with these suffixes meet the requirements of the RoHS directive.

This status is based on CEL's understanding of the EU Directives and knowledge of the materials that go into its products as of the date of disclosure of this information.

Restricted Substance per RoHS	Concentration Limit per RoHS (values are not yet fixed)	Concentration contained in CEL devices		
Lead (Pb)	< 1000 PPM	-A -AZ Not Detected (*)		
Mercury	< 1000 PPM	Not Detected		
Cadmium	< 100 PPM	Not Detected		
Hexavalent Chromium	< 1000 PPM	Not Detected		
РВВ	< 1000 PPM	Not Detected		
PBDE	< 1000 PPM	Not Detected		

If you should have any additional questions regarding our devices and compliance to environmental standards, please do not hesitate to contact your local representative.

In no event shall CEL's liability arising out of such information exceed the total purchase price of the CEL part(s) at issue sold by CEL to customer on an annual basis.

See CEL Terms and Conditions for additional clarification of warranties and liability.

Important Information and Disclaimer: Information provided by CEL on its website or in other communications concerting the substance content of its products represents knowledge and belief as of the date that it is provided. CEL bases its knowledge and belief on information provided by third parties and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. CEL has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. CEL and CEL suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.