

DGG PACKAGE

(TOP VIEW)

CEAB

64 CLKAB

FEATURES

- Member of the Texas Instruments Widebus™ Family
- OEC[™] Circuitry Improves Signal Integrity and **Reduces Electromagnetic Interference**
- **D-Type Flip-Flops With Qualified Storage** Enable
- **Translates Between GTL/GTL+ Signal Levels** and LVTTL Logic Levels
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltages With 3.3-V V_{cc})
- Ioff Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port
- Distributed V_{cc} and GND Pins Minimize **High-Speed Switching Noise**
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

The SN74GTL16923 is an 18-bit registered bus transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two 9-bit transceivers with individual output-enable controls and contains D-type flip-flops for temporary storage of data flowing in either direction. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC[™] circuitry.

	ч		• •	
1A1	C	2	63	10EAB
GND	_	3		10EBA
1A2		4]1B1
1A3	[5		GND
GND	[6]1B2
V_{CC}	[7	58]1B3
1A4		8	57]v _{cc}
GND		9]1B4
1A5	Ц	10]1B5
1A6	Ц	11]1B6
GND	Π	12	53] GND
1A7		13	52]1B7
1A8	_	14]1B8
GND		15] GND
1A9		16]1B9
2A1		17]2B1
GND	_	18] GND
2A2	_	19	46]2B2
2A3		20		2B3
GND		21] GND
2A4	Ц	22]2B4
2A5	[23		2B5
GND		24	41]2B6
2A6		25	40	V _{REF}
V _{CC}	[26	39	2B7
GND	Ц	27		2B8
2A7		28] GND
2A8	[29	36	2B9
GND		30	35	20EBA
2A9	C	31	34	20EAB
CEBA	Ц	32	33	CLKBA

The user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or the preferred higher noise margin GTL+ ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels. All inputs can be driven from either 3.3-V or 5-V devices, which allows use in a mixed 3.3-V/5-V system environment. V_{RFF} is the reference input voltage for the B port.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Data flow in each direction is controlled by the output-enable (\overline{OEAB} and \overline{OEBA}) and clock (CLKAB and CLKBA) inputs. The clock-enable (\overline{CEAB} and \overline{CEBA}) inputs enable or disable the clock for all 18 bits at a time. However, \overline{OEAB} and \overline{OEBA} are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if \overline{CEAB} is low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , CLKBA, and \overline{CEBA} .

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PACK	AGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL16923DGGR	GTL16923

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE ⁽¹⁾	
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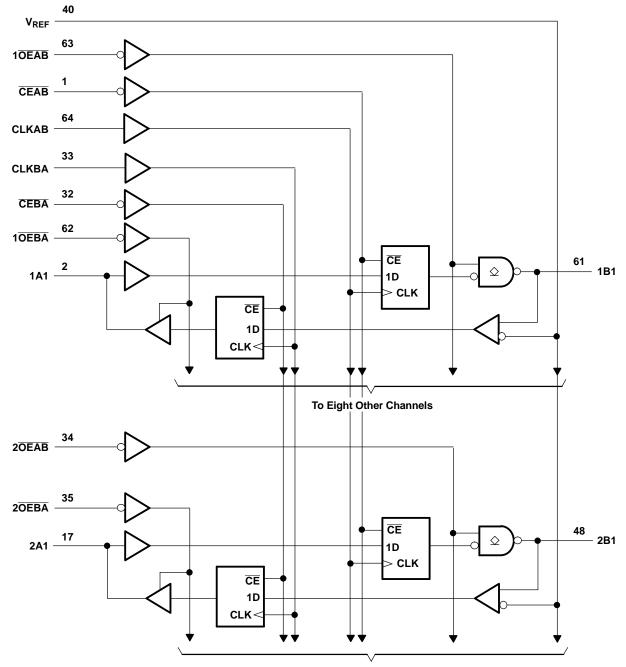
....

	INP	UTS		OUTPUT	MODE
CEAB	OEAB	CLKAB	Α	В	MODE
Х	Н	Х	Х	Z	Isolation
Н	L	Х	Х	B ₀ ⁽²⁾	Latabad starage of A data
Х	L	H or L	Х	B ₀ ⁽²⁾	Latched storage of A data
L	L	\uparrow	L	L	Clocked storage of A data
L	L	\uparrow	Н	Н	Clocked storage of A data

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses OEBA, CLKBA, and CEBA.

(2) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



To Eight Other Channels

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Voltage range applied to any output in the high or p	ower-off state ⁽²⁾	-0.5	7	V
	Current into any autout in the low state		48	~ ^	
I _O	Current into any output in the low state	B port		100	mA
lo	Current into any A-port output in the high state ⁽³⁾			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			55	°C/W
T _{stg}	Storage temperature range		-65	150	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings (1) only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This current flows only when the output is in the high state and $V_O > V_{CC}$. The package thermal impedance is calculated in accordance with JESD 51-7. (2)

(3)

(4)

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage		3.15	3.3	3.45	V	
V	Termination voltage	GTL	1.14	1.2	1.26	V	
V _{TT}	Termination voltage	GTL+	1.35	1.5	1.65	v	
M	GTL		0.74	0.8	0.87	N/	
V _{REF}	Reference voltage	GTL+	0.87	1	1.1	V	
V		B port	0		V _{TT}	V	
VI	Input voltage	Except B port	0		5.5	v	
V		B port	V _{REF} + 50 mV			V	
V _{IH}	High-level input voltage	Except B port	2			v	
\ <i>\</i>		B port			V _{REF} – 50 mV	V	
V _{IL}	Low-level input voltage	Except B port			0.8	V	
I _{IK}	Input clamp current				-18	mA	
I _{OH}	High-level output current	A port			-24	mA	
		A port			24	mA	
I _{OL}	Low-level output current	B port		50			
T _A	Operating free-air temperature		-40		85	°C	

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
Normal connection sequence is GND first, V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS	MIN TYP	¹⁾ MAX	UNIT	
V _{IK}		$V_{CC} = 3.15 \text{ V}, \text{ I}_{\text{I}} = -18 \text{ mA}$			-1.2	V	
		$V_{CC} = 3.15 \text{ V} \text{ to } 3.45 \text{ V},$	I _{OH} = −100 μA	V _{CC} – 0.2			
V _{OH}	A port	V 0.45.V	I _{OH} = -12 mA	2.4		V	
		V _{CC} = 3.15 V	I _{OH} = -24 mA	2			
		$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	I _{OL} = 100 μA		0.2		
	A port	V 0.45 V	I _{OL} = 12 mA		0.4		
		V _{CC} = 3.15 V	I _{OL} = 24 mA		0.5		
V _{OL}		$V_{CC} = 3.15 \text{ V} \text{ to } 3.45 \text{ V},$	I _{OL} = 100 μA		0.2	V	
P. port		I _{OL} = 10 mA		0.2			
	B port	V _{CC} = 3.15 V	I _{OL} = 40 mA		0.4		
			I _{OL} = 50 mA		0.55		
h .	B port	V _{CC} = 3.45 V,	$V_{I} = 5.5 \text{ V or GND}$		±5		
	A part and control inputs	V 0.45.V	$V_I = V_{CC}$ or GND		±5	μA	
	A-port and control inputs	V _{CC} = 3.45 V	$V_I = 5.5 V \text{ or GND}$		±20		
I _{off}		$V_{CC} = 0, V_1 \text{ or } V_0 = 0 \text{ to } 5.5 V_0$	V		±100	μA	
		V 045.V	V _I = 0.8 V	75			
I _{I(hold)}	A port	V _{CC} = 3.15 V	V ₁ = 2 V	-75		μA	
		$V_{CC} = 3.45 V^{(2)},$	V _I = 0.8 V to 2 V		±500		
I _{OZ} ⁽³⁾	A port	V _{CC} = 3.45 V,	$V_{O} = V_{CC}$ or GND		±10	μA	
I _{OZH}	B port	V _{CC} = 3.45 V,	V _O = 1.5 V		10	μA	
		V _{CC} = 3.45 V,	Outputs high		60		
I _{CC}	A or B port	$I_{0} = 0,$	Outputs low		60	mA	
		$V_{I} = V_{CC}$ or GND	Outputs disabled		60		
$\Delta I_{CC}^{(4)}$		V_{CC} = 3.45 V, A-port or contro One input at V_{CC} – 0.6 V	ol inputs at V_{CC} or GND,		500	μA	
Ci	Control inputs	V _I = 3.15 V or 0		2	.5 3	pF	
<u> </u>	A port	V _O = 3.15 V or 0			6 8.5	~ Г	
C _{io}	B port	V _O = 3.15 V or 0			7 9.5	pF	

(1)

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to (2) another.

For I/O ports, the parameter I_{OZ} includes the input leakage current. (3)

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)

			MIN	MAX	UNIT
f _{clock}	Clock frequency			200	MHz
t _w	Pulse duration, CLK high or low		2.5		ns
	Coture time	Data before CLK↑	2.6		~~~
lsu	Setup time	CE before CLK↑	3.3		ns
	Lold time	Data after CLK↑	0.1		~~~
ι _h	Hold time	CE after CLK↑	0		ns

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN 1	ГҮР ⁽¹⁾ МАХ	UNIT
f _{max}			200		MHz
t _{PLH}	CLKAB	В	2.2	5.8	– ns
t _{PHL}	ULKAD	D	2.1	6.3	115
t _{dis}		В	1.7	5.3	
t _{en}	OEAB	Б	2	5	ns
Slew rate	Both tr	ansitions		0.5	V/ns
t _r	Transition time, B	outputs (0.6 V to 1 V)	0.3	2.9	ns
t _f	Transition time, B	outputs (1 V to 0.6 V)	0.1	3.9	ns
t _{PLH}		•	1.8	5	
t _{PHL}	CLKBA	A	1.7	4.8	ns
t _{en}		٨	1.3	4.8	
t _{dis}	OEBA	A	2	4.8	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

			MIN	MAX	UNIT
f _{clock}	Clock frequency			200	MHz
tw	Pulse duration, CLK high or low		2.5		ns
	Coture time	Data before CLK↑	2.3		20
ι _{su}	Setup time	CE before CLK↑	3.3		ns
		Data after CLK↑	0.1		20
τ _h	Hold time	CE after CLK↑	0		ns

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
f _{max}			200			MHz
t _{PLH}	CLKAB	В	2.2	4	5.9	20
t _{PHL}	ULKAD	D	2.1	4	6.1	ns
t _{PLH}	OEAB	D	1.9	3.4	5.2	~~~
t _{PHL}	UEAD	В	1.7	3.1	5.1	ns
Slew rate	Both tr	ansitions		0.5		V/ns
t _r	Transition time, B o	utputs (0.6 V to 1.3 V)	0.6	1.3	2.6	ns
t _f	Transition time, B o	utputs (1.3 V to 0.6 V)	0.4	1.3	3	ns
t _{PLH}		•	1.8	3.5	5.1	
t _{PHL}	CLKBA	A	1.7	3.3	4.9	ns
t _{en}	OEBA	٨	1.3	2.9	4.8	20
t _{dis}	UEBA	A	2	3.2	5	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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1.5 V

From Output

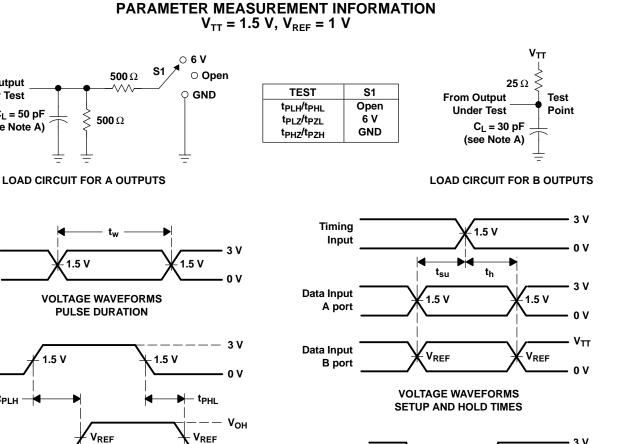
Input

Input

Under Test

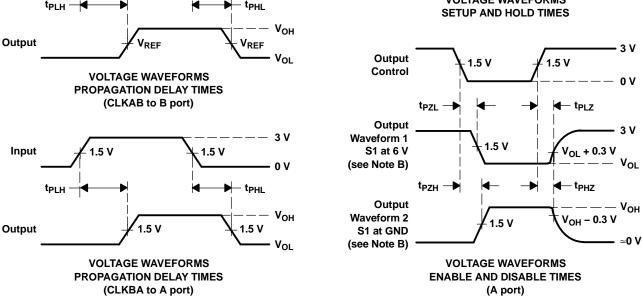
 $C_L = 50 \text{ pF}$

(see Note A)



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NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74GTL16923DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74GTL16923DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL16923DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

w

(mm)

24.0

K0

(mm)

1.7

P1

(mm)

12.0

Pin1

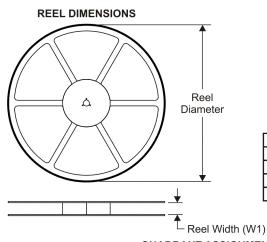
Quadrant

Q1

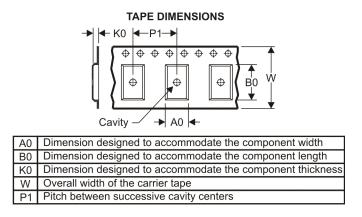
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TAPE AND REEL INFORMATION



SN74GTL16923DGGR



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



330.0

24.4

8.4

17.3

All dimensions are nominal					
Device	Package Type	Package Drawing		Reel Width W1 (mm)	B0 (mm)

64

2000

DGG

TSSOP

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

19-Jul-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL16923DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
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