TRSF3232E 3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER

TRUMENTS www.ti.com WITH ±15-kV IEC ESD PROTECTION SLLS825-AUGUST 2007

FEATURES

- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 1 Mbit/s
- Low Supply Current . . . 300 μA Typ
- External Capacitors . . . 4 \times 0.1 μF
- Accept 5-V Logic Input With 3.3-V Supply
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection for RS-232 Pins
 - ±15-kV Human-Body Model (HBM)
 - ±15-kV IEC 61000-4-2 Air-Gap Discharge
 - ±8-kV IEC 61000-4-2 Contact Discharge

APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

DESCRIPTION/ORDERING INFORMATION

The TRSF3232E consists of two line drivers, two line receivers, and a dual charge-pump circuit with \pm 15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3232E operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 14 V/µs to 150 V/µs.

ORDERING INFORMATION

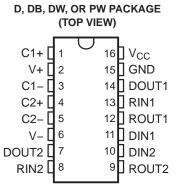
T _A	PACKA	GE ⁽¹⁾⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – D	Tube of 40	TRSF3232ECD	TRSF3232EC
	3010 - 0	Reel of 2500	TRSF3232ECDR	1K3F3232EC
	SOIC – DW	Tube of 40	TRSF3232ECDW	TRSF3232EC
0°C to 70°C	50IC - DW	Reel of 2000	TRSF3232ECDWR	TROF3232EC
	SSOP – DB	Reel of 2000	TRSF3232ECDBR	RT32EC
	TSSOP – PW	Tube of 90	TRSF3232ECPW	RT32EC
	1330P - PW	Reel of 2000	TRSF3232ECPWR	RIJZEC
	2010 0	Tube of 40	TRSF3232EID	TDOF2020EL
	SOIC – D	SOIC – DW	TRSF3232EIDR	TRSF3232EI
	SOIC – DW	Tube of 40	TRSF3232EIDW	TRSF3232EI
–40°C to 85°C	50IC - DW	TSSOP – PW	TRSF3232EIDWR	IRSF3232EI
	SSOP – DB	Reel of 2000	TRSF3232EIDBR	RT32EI
		Tube of 90	TRSF3232EIPW	DT22EL
	TSSOP – PW	Reel of 2000	TRSF3232EIPWR	RT32EI

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



TRSF3232E 3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION



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Table 1. 1-Mbit/s RS-232 Parts

TEMPERATURE RANGE	PART NO.	NO. OF DRIVERS	NO. OF RECEIVERS	ESD	SUPPLY V _{CC} (V)	FEATURE	PIN/ PACKAGE
	TRSF3221E	1	1	±15-kV Air-Gap Discharge, ±8-kV Contact Discharge, ±15-kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
	TRSF3232E	2	2	±15-kV Air-Gap Discharge, ±8-kV Contact Discharge, ±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
	TRS3227	1	1	±8-kV Air-Gap Discharge, ±8-kV Contact Discharge, ±15-kV HBM	3.3 or 5	Auto-powerdown plus, ready signal	16-pin SSOP
	TRSF3221	1	1	±15-kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
0°C to 70°C	TRSF3222	2	2	±15-kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
	TRSF3223	2	2	±15-kV HBM	3.5 or 5	Auto-powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
	TRSF3232	2	2	±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
	TRSF3238	5	3	±15-kV HBM	3.3 or 5	Auto-powerdown plus	28-pin SOIC, SSOP, TSSOP
	TRSF3243	3	5	±15-kV HBM	3.3 or 5	Auto-powerdown	28-pin SOIC, SSOP, TSSOP
	TRSF3221E	1	1	±15-kV Air-Gap Discharge, ±8-kV Contact Discharge, ±15-kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
	TRSF3232E	2	2	±15-kV Air-Gap Discharge, ±8-kV Contact Discharge, ±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
	TRS3227	1	1	±8-kV Air-Gap Discharge, ±8-kV Contact Discharge, ±15-kV HBM	3.3 or 5	Auto-powerdown plus, ready signal	16-pin SSOP
	TRSF3221	1	1	±15-kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
–40°C to 85°C	TRSF3222	2	2	±15-kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
	TRSF3223	2	2	±15-kV HBM	3.3 or 5	Auto-powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
	TRSF3232	2	2	±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
	TRSF3238	5	3	±15-kV HBM	3.3 or 5	Auto-powerdown plus	28-pin SOIC, SSOP, TSSOP
	TRSF3243	3	5	±15-kV HBM	3.3 or 5	Auto-powerdown	28-pin SOIC, SSOP, TSSOP

FUNCTION TABLES

Each Driver⁽¹⁾

INPUT DIN	OUTPUT DOUT
L	Н
н	L

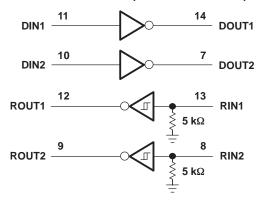
(1) H = high level, L = low level

Each Receiver⁽¹⁾

INPUT RIN	OUTPUT ROUT
L	Н
н	L
Open	Н

 (1) H = high level, L = low level, Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



TRSF3232E 3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER WITH \pm 15-kV IEC ESD PROTECTION



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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		-0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾		-0.3	7	V
V–	Negative-output supply voltage range ⁽²⁾		0.3	-7	V
V + - V -	Supply voltage difference ⁽²⁾			13	V
VI		Drivers	-0.3	6	
	Input voltage range	Receivers	-25	25	V
.,	Output voltage range	Drivers	-13.2	13.2	
Vo		Receivers	-0.3	V _{CC} + 0.3	V
		D package		82	
0	Declares the second interval $(3)(4)$	DB package		46	0000
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DW package		57	°C/W
		PW package		108	
TJ	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

				MIN	NOM	MAX	UNIT
	Supply voltage		$V_{CC} = 3.3 V$	3	3.3	3.6	V
	Supply voltage		$V_{CC} = 5 V$	4.5	5	5.5	v
v	Driver high-level input voltage	DIN	$V_{CC} = 3.3 V$	2			V
VIH		DIN	$V_{CC} = 5 V$	2.4			v
VIL	Driver low-level input voltage		DIN			0.8	V
v	Driver input voltage		DIN	0		5.5	N
VI	Receiver input voltage			-25		25	V
-	Operating free-air temperature		TRSF3232EI	-40		85	°C
T _A			TRSF3232EC	0		70	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V (see Figure 4).

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC}	Supply current	No load,	V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V (see Figure 4). (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDIT	IONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at $R_L = 3 k\Omega$ to GND,	DIN = GND	5	5.5		V
V _{OL}	Low-level output voltage	DOUT at $R_L = 3 k\Omega$ to GND,	$DIN = V_{CC}$	-5	-5.4		V
I _{IH}	High-level input current	$V_{I} = V_{CC}$			±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	μA
ı (3)	Short-circuit output current	V _{CC} = 3.6 V,	$V_0 = 0 V$		±35	±60	<u>س</u> ۸
I _{OS} ⁽³⁾		V _{CC} = 5.5 V,	$V_0 = 0 V$		±35	±90	mA
r _o	Output resistance	V_{CC} , V+, and V- = 0 V,	$V_0 = \pm 2 V$	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V (see Figure 4).

(2) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^{\circ}$ C. (3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER TEST CONDITIONS		MIN	TYP ⁽²⁾ M/	X UNIT	
	Maximum data rate	$R_{L} = 3 k\Omega,$	$C_L = 250 \text{ pF}, \qquad V_{CC} = 3 \text{ V to } 4.5 \text{ V}$	1000		kbit/s
	(see Figure 1)	One DOUT switching	$C_L = 1000 \text{ pF}, V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$			KDII/S
t _{sk(p)}	Pulse skew ⁽³⁾	C_L = 150 pF to 2500 pF, R_L	L = 150 pF to 2500 pF, RL = 3 kΩ to 7 kΩ, See Figure 2			ns
SR(tr)	Slew rate, transition region (see Figure 1)	$R_L = 3 k\Omega$ to 7 k Ω , $C_L = 150$	= 3 k\Omega to 7 kΩ, C_{L} = 150 pF to 1000 pF, V_{CC} = 3.3 V		1	50 V/µs

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V (see Figure 4). All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device. (1)

(2)

(3)

ESD Protection

TERM	INAL	TEST CONDITIONS		UNIT
NAME	NO.	TEST CONDITIONS	TYP	UNIT
		НВМ	±15	
DOUT	7, 14	IEC 61000-4-2 Air-Gap Discharge	±15	kV
		IEC 61000-4-2 Contact Discharge	±8	

TRSF3232E 3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION



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RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.6$	V _{CC} – 0.1		V
V_{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
14	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
V _{IT+}		$V_{CC} = 5 V$		1.8	2.4	v
	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		
V _{IT-}		$V_{CC} = 5 V$	0.8	1.5		v
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.3		V
ri	Input resistance	$V_1 = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V (see Figure 4). (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF	300	ns
t _{sk(p)}	Pulse skew ⁽³⁾		300	ns

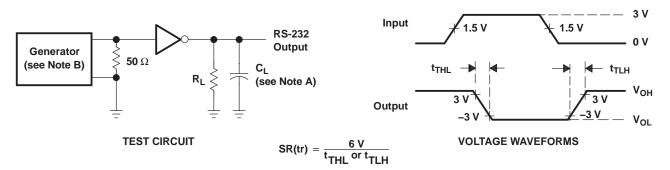
(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V (see Figure 4). (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

ESD Protection

TERMINAL		TEST CONDITIONS	ТҮР	UNIT
NAME	NO.	TEST CONDITIONS	ITP	UNIT
		НВМ	±15	
RIN	8, 13	IEC 61000-4-2 Air-Gap Discharge	±15	kV
		IEC 61000-4-2 Contact Discharge	±8	

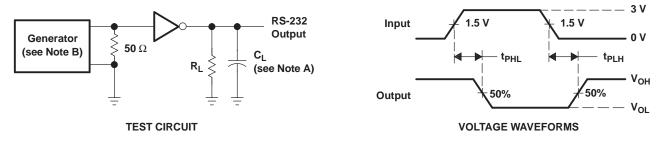
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

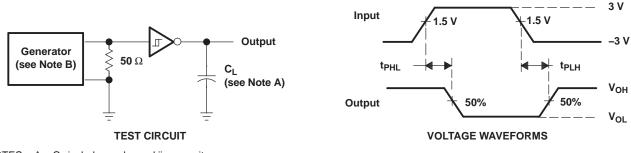
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_0 = 50 Ω , 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance. B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance. B. The pulse generator has the following characteristics: $Z_0 = 50 \ \Omega$, 50% duty cycle, $t_r \le 10 \text{ ns}$, $t_f \le 10 \text{ ns}$.

Figure 3. Receiver Propagation Delay Times





V _{CC}	C1	C2, C3, C4
$\begin{array}{c} \textbf{3.3 V} \pm \textbf{0.3 V} \\ \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{3 V to 5.5 V} \end{array}$	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF

A. C3 can be connected to $V_{\mbox{\scriptsize CC}}$ or GND.

Figure 4. Typical Operating Circuit and Capacitor Values

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2

3

4

5 C2-

6 V_

7

8

 5 kΩ

C3 +

C2

DOUT2

RIN2

C1 =

V+

C1-

C2+

1 C1+ V_{CC} 16 -+ C_{BYPASS} = 0.1 μ F

15

14

13

12

11

10

9

DOUT1

RIN1

ROUT1

DIN1

DIN2

ROUT2

GND

5 kΩ <

APPLICATION INFORMATION



TEXAS INSTRUMENTS www.ti.com

26-Sep-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TRSF3232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TRSF3232EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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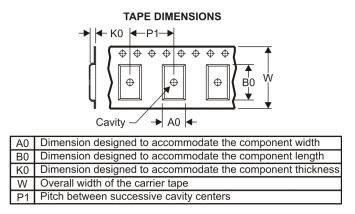
PACKAGE MATERIALS INFORMATION

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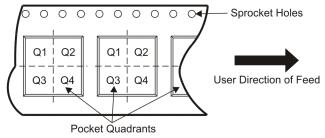
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



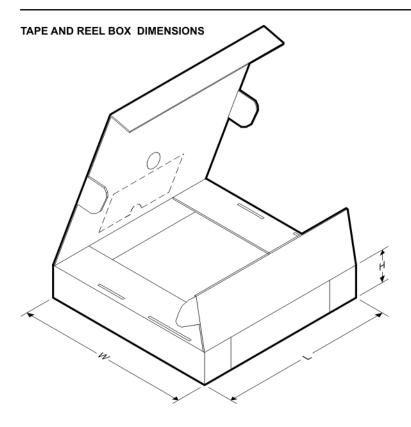
*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRSF3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRSF3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRSF3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRSF3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRSF3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRSF3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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5-Mar-2011



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3232ECDBR	SSOP	DB	16	2000	346.0	346.0	33.0
TRSF3232ECDR	SOIC	D	16	2500	346.0	346.0	33.0
TRSF3232ECDWR	SOIC	DW	16	2000	346.0	346.0	33.0
TRSF3232ECPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TRSF3232EIDBR	SSOP	DB	16	2000	346.0	346.0	33.0
TRSF3232EIDR	SOIC	D	16	2500	346.0	346.0	33.0
TRSF3232EIDWR	SOIC	DW	16	2000	346.0	346.0	33.0
TRSF3232EIPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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