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# SN74GTL1655 16-BIT LVTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVER WITH LIVE INSERTION

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#### **FEATURES**

- Member of the Texas Instruments Widebus™ Family
- UBT<sup>™</sup> Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- OEC<sup>™</sup> Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Translates Between GTL/GTL+ Signal Level and LVTTL Logic Levels
- High-Drive (100 mA), Low-Output-Impedance (12 Ω) Bus Transceiver (B Port)
- Edge-Rate-Control Input Configures the B-Port Output Rise and Fall Times
- I<sub>off</sub>, Power-Up 3-State, and BIAS V<sub>CC</sub> Support Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise

#### **DESCRIPTION/ORDERING INFORMATION**

The SN74GTL1655 is a high-drive (100 mA), **UBT**TM low-output-impedance  $(12 \Omega)$ 16-bit transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two 8-bit transceivers and combines D-type flip-flops and D-type latches to allow for transparent, latched, and clocked modes of data transfer similar to the '16501 function. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry. drive is suitable for high driving double-terminated low-impedance backplanes using incident-wave switching.

#### DGG PACKAGE (TOP VIEW)

1 <del>OEAB</del>	1	$\bigcup_{64}$	CLK
	2		1LEAB
	3	62	
	4	61	V <sub>ERC</sub>
GND	5	60	GND
1A2		59	] 1B1
1A3	7	58	] 1B2
GND	8	57	] GND
1A4	9	56	] 1B3
GND	10	55	] 1B4
1A5	11	54	] 1B5
GND	12	53	] GND
1A6	13	52	] 1B6
1A7	14	51	] 1B7
V <sub>CC</sub>	15	50	] v <sub>cc</sub>
1A8	16		] 1B8
2A1	17	48	] 2B1
GND		47	] GND
2A2		46	] 2B2
2A3	20		] 2B3
GND			GND
2A4	22		] 2B4
	23	42	] 2B5
GND	24	41	] V <sub>REF</sub>
2A6	25		] 2B6
GND	26	39	] GND
	27		2B7
V <sub>CC</sub>	28	37	] 2B8
2A8	_	36	BIAS V <sub>CC</sub>
GND		35	2LEAB
2 <mark>OEAB</mark>	31	34	2LEBA
2 <mark>OEBA</mark>	32	33	] OE
			•

The user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2 \text{ V}$  and  $V_{REF} = 0.8 \text{ V}$ ) or the preferred higher noise margin GTL+ ( $V_{TT} = 1.5 \text{ V}$  and  $V_{REF} = 1 \text{ V}$ ) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels, but are not 5-V tolerant.  $V_{REF}$  is the reference input voltage for the B port.



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### **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

This device is partitioned uniquely as two 8-bit transceivers with individual latch timing and output signals, but with a common clock and output enable inputs for both transceiver words.

Data flow for each word is determined by the respective latch enables (LEAB and LEBA), output enables (OEAB and OEBA), and clock (CLK). The output enables (1OEAB, 1OEBA, 2OEAB, and 2OEBA) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When  $\overline{OEAB}$  is low, the outputs are active. With  $\overline{OEAB}$  high, the outputs are in the high-impedance state.

Data flow for the B-to-A direction is identical, but uses  $\overline{\text{OEBA}}$ , LEBA, and CLK. Note that CLK is common to both directions and both 8-bit words.  $\overline{\text{OE}}$  also is common and is used to disable all I/O ports simultaneously.

The SN74GTL1655 has adjustable edge-rate control ( $V_{ERC}$ ). Changing  $V_{ERC}$  input voltage between GND and  $V_{CC}$  adjusts the B-port output rise and fall times. This allows the designer to optimize for various loading conditions.

This device is fully specified for live-insertion applications using  $I_{\rm off}$ , power-up 3-state, and BIAS  $V_{\rm CC}$ . The  $I_{\rm off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{\rm CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL1655DGGR	GTL1655

<sup>(1)</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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### **FUNCTION TABLES**

## **FUNCTION**<sup>(1)</sup>

INPUTS				OUTPUT	MODE
OEAB	LEAB	CLK	Α	В	MODE
Н	Χ	Χ	X	Z	Isolation
L	Н	X	L	L	Transparent
L	Н	X	Н	Н	Transparent
L	L	$\uparrow$	L	L	Registered
L	L	$\uparrow$	Н	Н	Registered
L	L	Н	Χ	B <sub>0</sub> <sup>(2)</sup>	Previous state
L	L	L	Χ	B <sub>0</sub> <sup>(3)</sup>	Previous state

- A-to-B data flow is shown. B-to-A flow is similar, but uses <del>OEBA</del>, LEBA, and CLK.
- (2) Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low
- (3) Output level before the indicated steady-state input conditions were established

### **OUTPUT ENABLE**

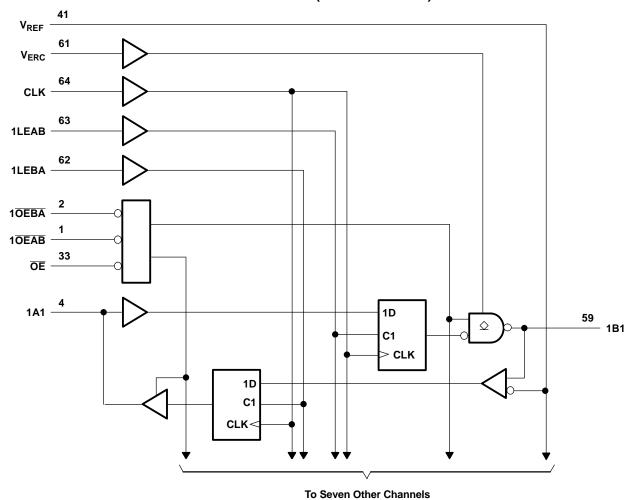
INPUTS			OUT	PUTS
ŌĒ	OEAB	OEBA	A PORT	B PORT
L	L	L	Active	Active
L	L	Н	Z	Active
L	Н	L	Active	Z
L	Н	Н	Z	Z
Н	Х	Χ	Z	Z

## **B-PORT EDGE-RATE CONTROL (VERC)**

in	put V <sub>ERC</sub>	OUTPUT
LOGIC LEVEL	NOMINAL VOLTAGE	B-PORT EDGE RATE
Н	V <sub>CC</sub>	Slow
L	GND	Fast



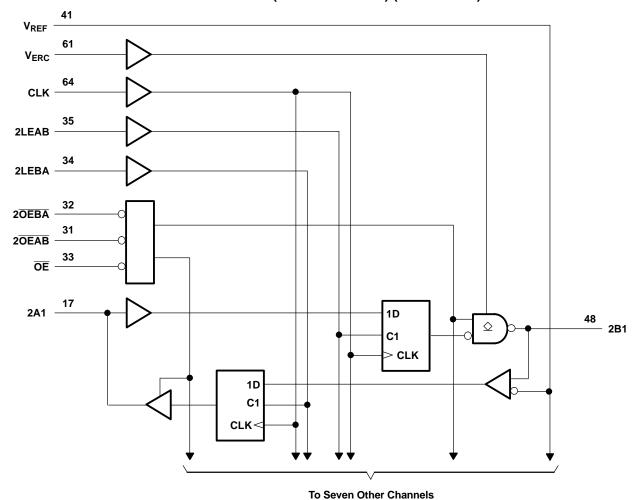
## **LOGIC DIAGRAM (POSITIVE LOGIC)**





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# LOGIC DIAGRAM (POSITIVE LOGIC) (CONTINUED)



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# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$ BIAS $V_{CC}$	Supply voltage range			4.6	V
V	Input voltage range <sup>(2)</sup>	A-port and control inputs	-0.5	4.6	V
VI	input voltage range -/	B port, $V_{ERC}$ , and $V_{REF}$	-0.5	4.6	V
V	Voltage range applied to any output in the high or power-off state (2)	A port	-0.5	4.6	V
Vo	voltage range applied to any output in the high of power-on state (=)	B port	-0.5 4.6	V	
	Current into any autaut in the law state	A port		48	mA
I <sub>O</sub> C	Current into any output in the low state	B port		200	IIIA
Io	Current into any A-port output in the high state (3)			48	mA
	Continuous current through each V <sub>CC</sub> or GND			±100	mA
$I_{lK}$	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
$\theta_{JA}$	Package thermal impedance (4)			55	°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

The current flows only when the output is in the high state and  $V_{\rm O} > V_{\rm CC}$ . The package thermal impedance is calculated in accordance with JESD 51-7.

# Recommended Operating Conditions (1)(2)(3)(4)

			MIN	NOM	MAX	UNIT
BIAS V <sub>CC</sub>	Supply voltage		3	3.3	3.6	V
	Tanadaattaa saltaa	GTL	1.14	1.2	1.26	
$V_{TT}$	Termination voltage	GTL+	1.35	1.5	1.65	V
	Defenses valteres	GTL	0.74	0.8	0.87	V
$V_{REF}$	Reference voltage	GTL+	0.87	1	1.1	V
	langut valtana	B port	0		V <sub>TT</sub>	V
V <sub>I</sub>	Input voltage	Except B port	0		V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	B port	V <sub>REF</sub> + 50 mV			
		V <sub>ERC</sub>	V <sub>CC</sub> - 0.6	V <sub>CC</sub>		V
		Except B port and ERC	2			
		B port		١	/ <sub>REF</sub> – 50 mV	
$V_{IL}$	Low-level input voltage	V <sub>ERC</sub>		GND	0.6	V
		Except B port and ERC			3.6 1.26 1.65 0.87 1.1 V <sub>TT</sub> V <sub>CC</sub>	
I <sub>IK</sub>	Input clamp current				-18	mA
I <sub>OH</sub>	High-level output current	A port			-24	mA
	Lour lovel output output	A port			24	mA
l <sub>OL</sub>	Low-level output current	B port			100	mA
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			μs/V
T <sub>A</sub>	Operating free-air temperature		-40		85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Normal connection sequence is GND first, BIAS  $V_{CC}$  = 3.3 V second, and  $V_{CC}$  = 3.3 V, I/O, control inputs,  $V_{TT}$  and  $V_{REF}$  (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and  $V_{CC} = 3.3 \text{ V}$ , BIAS  $V_{CC} = 3.3 \text{ V}$ , I/O, control inputs,  $V_{TT}$  and  $V_{REF}$  (any order) last. When  $V_{CC}$  is connected, the BIAS  $V_{CC}$  circuitry is disabled.

 $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded.  $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ .



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### **Electrical Characteristics**

over recommended operating free-air temperature range,  $V_{REF} = 1 \text{ V}$  and  $V_{TT} = 1.5 \text{ V}$  (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN T	(P <sup>(1)</sup> MAX	UNIT
$V_{IK}$		$V_{CC} = 3 V$ ,	$I_{I} = -18 \text{ mA}$		-1.2	V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$	$I_{OH} = -100 \mu A$	V <sub>CC</sub> - 0.2		
$V_{OH}$	A port	V 0.V	$I_{OH} = -12 \text{ mA}$	2.4		V
		$V_{CC} = 3 V$	$I_{OH} = -24 \text{ mA}$	2.2		
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$	I <sub>OL</sub> = 100 μA		0.2	
	A port	V 0.V	I <sub>OL</sub> = 12 mA		0.4	
.,		$V_{CC} = 3 V$	I <sub>OL</sub> = 24 mA		0.55	
$V_{OL}$			I <sub>OL</sub> = 40 mA		0.2	V
	B port	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 80 mA		0.4	
			I <sub>OL</sub> = 100 mA		0.5	
	Control inputs	V 00V	$V_I = V_{CC}$ or GND		±10	^
I <sub>I</sub> B port	B port	V <sub>CC</sub> = 3.6 V	$V_I = V_{TT}$ or GND		±10	μΑ
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_{1}$ or $V_{0} = 0$ to 3.6 V		±100	μΑ
	A port	v <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	75		
I <sub>I(hold)</sub>			V <sub>I</sub> = 2 V	-75		μΑ
, ,		$V_{CC} = 3.6 V^{(2)},$	$V_I = 0$ to $V_{CC}$		±500	
l <sub>ozh</sub>	B port	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 1.5 V		10	μΑ
I <sub>OZL</sub>	B port	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.4 V		-10	μΑ
I <sub>OZ</sub> (3)	A port	V <sub>CC</sub> = 3.6 V,	$V_O = V_{CC}$ or GND		±10	μΑ
I <sub>OZPU</sub>	A port	$V_{CC} = 0 \text{ to } 3.6 \text{ V}, V_{O} = 0.5$	V to 3 V, $\overline{OE} = low$		±50	μΑ
I <sub>OZPD</sub>	A port	$V_{CC} = 3.6 \text{ V to } 0, V_{O} = 0.5$	V to 3 V, $\overline{OE} = low$		±50	μΑ
			Outputs high		80	
$I_{CC}$	A or B port	$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		80	mA
		1 = AGG OL GIAD	Outputs disabled		80	
ΔI <sub>CC</sub> <sup>(4)</sup>	Except B port	$V_{CC} = 3.6 \text{ V}$ , A-port or cont One input at $V_{CC} - 0.6 \text{ V}$	rol inputs at V <sub>CC</sub> or GND,		1	mA
C <sub>i</sub>	Control inputs	$V_I = V_{CC}$ or 0			3 5	pF
^	A port	\/ \/ or 0			5 6	~F
$C_{io}$	B port	$V_O = V_{CC}$ or 0			6 8	pF

- (1) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ . (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to
- (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.
  (4) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

### **Live-Insertion Specifications**

over recommended operating free-air temperature range

PA	RAMETER		TEST CONDITIONS				UNIT
I (DIA	C \/ \	$V_{CC} = 0$ to 3 V	\/ (P nort) = 0 to 1 2 \/	V (BIAS V ) = 2 V to 2 6 V		5	mA
I <sub>CC</sub> (BIA	S V <sub>CC</sub> )	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_0$ (B port) = 0 to 1.2 V,	$V_I$ (BIAS $V_{CC}$ ) = 3 V to 3.6 V		10	μΑ
Vo	B port	$V_{CC} = 0$ ,	$V_{I}$ (BIAS $V_{CC}$ ) = 3.3 V		1	1.2	V
		$V_{CC} = 0$ ,	$V_O$ (B port) = 0.4 V,	$V_I$ (BIAS $V_{CC}$ ) = 3 V to 3.6 V	-1		
Io	B port	$V_{CC} = 0 \text{ to } 3.6 \text{ V},$	<del>OE</del> = 3.3 V			100	μΑ
		$V_{CC} = 0 \text{ to } 1.5 \text{ V},$	OE = 0 to 3.3 V			100	

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### **Timing Requirements**

over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT}$  = 1.2 V,  $V_{REF}$  = 0.8 V, and  $V_{ERC}$  =  $V_{CC}$  or GND for GTL (unless otherwise noted)

				MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency				160	MHz
	Pulse duration	LE high		3		
t <sub>w</sub> Pulse duration	CLK high or low		3		ns	
		Data before CLK↑	•	2.7		
t <sub>su</sub>	Setup time	Data hafara I 5	CLK high	2.8		ns
		Data before LE↓	CLK low	2.6		
	Hald time	Data after CLK↑		0.4		
t <sub>h</sub>	поіа ште	Hold time Data after LE↓	CLK high or low	0.9		ns

### A-to-B Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,

 $V_{TT} = 1.2 \text{ V}$ ,  $V_{REF} = 0.8 \text{ V}$ , and  $V_{ERC} = V_{CC}$  or GND for GTL (see Figure 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
	f <sub>max</sub>			160			MHz
	t <sub>PLH</sub>	А	В	3.1		5.2	20
	t <sub>PHL</sub>	$V_{ERC} = V_{CC}$	В	2.6		6.2	ns
	t <sub>PLH</sub>	CLK	В	3.4		5.5	ns
	t <sub>PHL</sub>	$V_{ERC} = V_{CC}$	Б	2.4		5.8	115
	t <sub>PLH</sub>	LEAB	В	3.5		5.8	ns
	t <sub>PHL</sub>	$V_{ERC} = V_{CC}$	В	2.6		6.4	115
	t <sub>en</sub>	OEAB or OE	В	3.3		5.4	
	$t_{dis}$	$V_{ERC} = V_{CC}$	Ь	2.7		5.9	ns
	t <sub>PLH</sub>	А	В	2.3		4.3	ns
	t <sub>PHL</sub>	$V_{ERC} = GND$	Ь	1.9		4.3	115
	t <sub>PLH</sub>	CLK V <sub>ERC</sub> = GND	В	2.7		4.8	ns
	t <sub>PHL</sub>			1.8		4.3	115
	t <sub>PLH</sub>	LEAB	В	2.8		4.9	20
	t <sub>PHL</sub>	$V_{ERC} = GND$	В	2		4.8	ns
	t <sub>en</sub>	OEAB or OE	В	2.5		4.5	ne
	$t_{dis}$	$V_{ERC} = GND$	Ь	2		4.2	ns
	$V_{ERC} = GND$	Transition time P.	outputs (0.6 V to 1 V)		0.6		ns
t <sub>r</sub>	$V_{ERC} = V_{CC}$	Transition time, b c	outputs (0.6 V to 1 V)	2.8 4.9 2 4.8 2.5 4.5 2 4.2 0.6 1.2 1.1		115	
	V <sub>ERC</sub> = GND	Transition time P.	outputs (1 V to 0.6 V)		1.1		20
t <sub>f</sub>	$V_{ERC} = V_{CC}$	Transition time, b c	outputs (1 v to 0.6 v)		1.7		ns
	t <sub>sk(o)</sub> <sup>(1)</sup>	Skew between driver switching in the	s in the same package e same direction			1	ns
	t <sub>sk(o)</sub> (2)		veen drivers on in the same package			1	ns

<sup>(1)</sup> Skew values are applicable for through mode only.

<sup>(2)</sup> Skew values are applicable for CLK mode only, with all outputs switching simultaneously.



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## **B-to-A Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT}$  = 1.2 V and  $V_{REF}$  = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>max</sub>			160		MHz
t <sub>PLH</sub>	В	A	1.8	4.7	ns
t <sub>PHL</sub>	В	A	2.3	4.6	115
t <sub>PLH</sub>	CLK	CLK A	1.6	4	
t <sub>PHL</sub>	CLK		1.5	3.4	ns
t <sub>PLH</sub>	LEBA	^	1.7	4	20
t <sub>PHL</sub>	LEBA	A	1.4	3.5	ns
t <sub>en</sub>	OEBA or OE	^	1.2	4.2	20
t <sub>dis</sub>	OEBA OI OE	A	1.2	6.1	ns
t <sub>sk(o)</sub> <sup>(1)</sup>		s in the same package same direction		1	ns
t <sub>sk(o)</sub> (2)		een drivers on in the same package		1	ns

<sup>(1)</sup> Skew values are applicable for through mode only.(2) Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

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### **Timing Requirements**

over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT}$  = 1.5 V,  $V_{REF}$  = 1 V, and  $V_{ERC}$  =  $V_{CC}$  or GND for GTL+ (unless otherwise noted)

				MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency				160	MHz
A Dules duration		LE high	LE high			
ι <sub>w</sub>	Pulse duration	CLK high or low	CLK high or low			ns
		Data before CLK↑	Data before CLK↑			
t <sub>su</sub>	Setup time	Data hatara I.E.	CLK high	2.8		ns
		Data before LE↓	CLK low	2.6		
t <sub>h</sub>	Hald time	Data after CLK↑		0.4		ns
	Hold time	Data after LE↓	CLK high or low	0.9		

### A-to-B Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,

 $V_{TT}$  = 1.5 V,  $V_{REF}$  = 1 V, and  $V_{ERC}$  =  $V_{CC}$  or GND for GTL+ (see Figure 1)

PAR	AMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
	f <sub>max</sub>			160			MHz
	t <sub>PLH</sub>	Α	В	3		5.1	ns
	t <sub>PHL</sub>	$V_{ERC} = V_{CC}$	Ь	2.9		6.5	115
	t <sub>PLH</sub>	CLK	В	3.4		5.4	ns
	t <sub>PHL</sub>	$V_{ERC} = V_{CC}$	Ь	2.7		6.2	115
	t <sub>PLH</sub>	LEAB	В	3.5		5.7	ns
	t <sub>PHL</sub>	$V_{ERC} = V_{CC}$	Ь	2.8		6.7	115
	t <sub>en</sub>	OEAB	В	3.3		5.4	ns
	t <sub>dis</sub>	$V_{ERC} = V_{CC}$	Ь	3		6.3	115
	t <sub>en</sub>	ŌĒ	В	3		5.5	ns
	t <sub>dis</sub>	$V_{ERC} = V_{CC}$	Ь	3.6		5.8	115
	t <sub>PLH</sub>	Α	В	2.3		4.3	ns
	t <sub>PHL</sub>	$V_{ERC} = GND$	D	2		4.4	113
	t <sub>PLH</sub>	CLK	В	2.7		4.8	ns
	t <sub>PHL</sub>	$V_{ERC} = GND$	Ь	1.9		4.5	115
	t <sub>PLH</sub>	LEAB	В	2.8		4.9	ns
	t <sub>PHL</sub>	$V_{ERC} = GND$	D	2.1		4.9	113
	t <sub>en</sub>	OEAB	В	2.5		4.5	ns
	t <sub>dis</sub>	$V_{ERC} = GND$	Ь	2.1		4.4	
	t <sub>en</sub>	ŌĒ	В	2.5		4.6	ns
	t <sub>dis</sub>	$V_{ERC} = GND$	D	2.9		4.9	113
t <sub>r</sub>	$V_{ERC} = GND$	Transition time R ou	tputs (0.6 V to 1.3 V)		0.9		ns
۲r	$V_{ERC} = V_{CC}$	Transition time, b ou		1.7			
+	$V_{ERC} = GND$	Transition time R ou	tputs (1.3 V to 0.6 V)		1.6		ns
t <sub>f</sub>	$V_{ERC} = V_{CC}$	Transition time, b ou		2.4		113	
t,	sk(o) <sup>(1)</sup>	Skew between drivers switching in the			1	ns	
t,	sk(o) <sup>(2)</sup>		een drivers on in the same package			1	ns

<sup>(1)</sup> Skew values are applicable for through mode only.

<sup>(2)</sup> Skew values are applicable for CLK mode only, with all outputs switching simultaneously.



SCBS696I-JULY 1997-REVISED APRIL 2005

# **B-to-A Switching Characteristics**

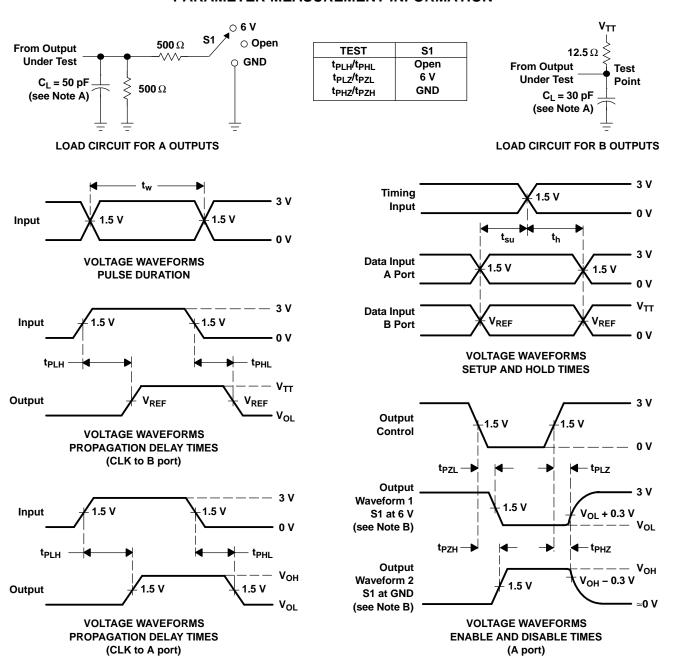
over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT}$  = 1.5 V and  $V_{REF}$  = 1 V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>max</sub>			160		MHz
t <sub>PLH</sub>	В	A	2	4.8	20
t <sub>PHL</sub>	Ь	A	2.4	4.7	ns
t <sub>PLH</sub>	CLK	A	1.6	4.4	20
t <sub>PHL</sub>	CLK	A	1.5	3.4	ns
t <sub>PLH</sub>	LEBA	А	1.7	4	20
t <sub>PHL</sub>	LEBA	A	1.4	3.5	ns
t <sub>en</sub>	<del>-</del> <del>OEBA</del>	A	1.2	4.2	20
t <sub>dis</sub>	OEBA	A	1.2	6.1	ns
t <sub>en</sub>	- OE	A	1.2	4.7	20
t <sub>dis</sub>	- OE	A	1.2	6.3	ns
t <sub>sk(o)</sub> <sup>(1)</sup>	Skew between drivers switching in the		1	ns	
t <sub>sk(o)</sub> (2)	Skew betw switching in any direction		1	ns	

Skew values are applicable for through mode only. Skew values are applicable for CLK mode only, with all outputs switching simultaneously.



#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{O}$  = 50  $\Omega$ ,  $t_{f} \leq$  2.5 ns,  $t_{f} \leq$  2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

Figure 1. Load Circuits and Voltage Waveforms





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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74GTL1655DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL1655DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL1655DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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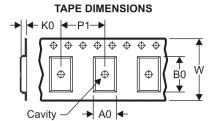
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# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL1655DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL1655DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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