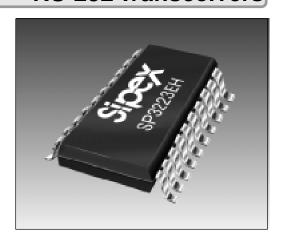


# SP3223EH/3243EH

# High Speed Intelligent +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- Auto-Online™ circuitry automatically wakes up from a 1µA shutdown
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V<sub>cc</sub> Variations
- Enhanced ESD Specifications: ±15KV Human Body Model ±15KV IEC1000-4-2 Air Discharge +8KV IEC1000-4-2 Contact Discharge
- 460 Kbps minimum transmission rate
- Ideal for High Speed RS-232 Applications



#### **DESCRIPTION**

The SP3223EH and 3243EH products are RS-232 transceiver solutions intended for portable or hand-held applications such as notebook and palmtop computers. The "H" series is based on Sipex's SP3223E/3243E series and has been enhanced for high speed. The data rate is improved to 460Kbps, easily meeting the demands of high speed RS-232 applications. The SP3223EH and 3243EH use an internal high-efficiency, charge-pump power supply that requires only 0.1μF capacitors in 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3223EH/3243EH series to deliver compliant RS-232 performance from a single power supply ranging from +3.3V to +5.0V. The SP3223EH is a 2-driver/2-receiver device, and the SP3243EH is a 3-driver/5-receiver device, ideal for laptop/notebook computer and PDA applications. The SP3243EH includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown.

The *Auto-Online* feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than  $1\mu A$ .

# **SELECTION TABLE**

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Auto-Online Circuitry	TTL 3-State	No. of Pins
SP3223EH	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
SP3243EH	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28

Applicable U.S. Patents - 5,306,954; and other patents pending.

#### **ABSOLUTE MAXIMUM RATINGS**

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

401.001	
V <sub>cc</sub>	0.3V to +6.0V
V+ (NOTE 1)	0.3V to +7.0V
V- (NOTE 1)	+0.3V to -7.0V
V+ +  V-  (NOTE 1)	
I <sub>cc</sub> (DC V <sub>cc</sub> or GND current)	
Input Voltages	
TxIN, ONLINE,	
SHUTDOWN, EN (SP3223EH)	0.3V to +6.0V
RxIN	<u>+</u> 15V
Output Voltages	
TxOUT	<u>+</u> 15V
RxOUT, STATUS	$0.3V \text{ to } (V_{cc} + 0.3V)$
Short-Circuit Duration	, ,
TxOUT	Continuous
Storage Temperature	65°C to +150°C

#### Power Dissipation per package

20-pin PDIP (derate 16.0mW/°C above+70°C).....1300mW 20-pin SSOP (derate 9.25mW/°C above +70°C).....750mW 20-pin TSSOP (derate 11.1mW/°C above +70°C)...900mW 28-pin SOIC (derate 12.7mW/°C above +70°C)....1000mW 28-pin SSOP (derate 11.2mW/°C above +70°C).....900mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

#### **SPECIFICATIONS**

Unless otherwise noted, the following specifications apply for  $V_{CC}$  = +3.0V to +5.5V with  $T_{AMB}$  =  $T_{MIN}$  to  $T_{MAX}$ . Typical values apply at  $V_{CC}$  = +3.3V or +5.0V and  $T_{AMB}$  = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current, Auto-Online		1.0	10	μА	All RxIN open, $\overline{\text{ONLINE}} = \text{GND}$ , $\overline{\text{SHUTDOWN}} = \text{V}_{\text{CC}}$ , $\overline{\text{V}}_{\text{CC}} = +3.3\text{V}$ , $\overline{\text{T}}_{\text{AMB}} = +25^{\circ}\text{C}$
Supply Current, Shutdown		1.0	10	μА	$\overline{\text{SHUTDOWN}} = \text{GND},$ $V_{\text{CC}} = +3.3\text{V}, T_{\text{AMB}} = +25^{\circ} \text{ C}$
Supply Current, Auto-Online Disabled		0.3	1.0	mA	$\overline{\text{ONLINE}} = \overline{\text{SHUTDOWN}} = \text{V}_{\text{CC}},$ no load, $\text{V}_{\text{CC}} = +3.3\text{V}, \text{T}_{\text{AMB}} = +25^{\circ} \text{C}$
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	2.0		0.8	V	V <sub>CC</sub> = +3.3V or +5.0V, TxIN, <u>EN (<b>SP3223EH</b>), ONLINE,</u> <u>SHUTDOWN</u>
Input Leakage Current		<u>+</u> 0.01	<u>+</u> 1.0	μА	$T_{XIN}$ , $\overline{EN}$ , $\overline{ONLINE}$ , $\overline{SHUTDOWN}$ , $T_{AMB} = +25^{\circ}$ C
Output Leakage Current		<u>+</u> 0.05	<u>+</u> 10	μΑ	Receivers disabled
Output Voltage LOW			0.4	V	I <sub>OUT</sub> = 1.6mA
Output Voltage HIGH	V <sub>CC</sub> - 0.6	V <sub>cc</sub> - 0.1		V	I <sub>OUT</sub> = -1.0mA

**SPECIFICATIONS (continued)** Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0 \text{V}$  to +5.5 V with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ . Typical values apply at  $V_{CC} = +3.3 \text{V}$  or +5.0 V and  $T_{AMB} = 25 ^{\circ}\text{C}$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS					
Output Voltage Swing	<u>+</u> 5.0	<u>+</u> 5.4		V	All driver outputs loaded with $3K\Omega$ to GND, $T_{AMB} = +25^{\circ}$ C
Output Resistance	300			Ω	$V_{CC} = V + = V - = 0V, V_{OUT} = \pm 2V$
Output Short-Circuit Current		<u>+</u> 35 <u>+</u> 70	<u>+</u> 60 <u>+</u> 100	mA	$V_{OUT} = 0V$ $V_{OUT} = \pm 15V$
Output Leakage Current			±25	μА	$V_{CC} = 0V \text{ or } 3.0V \text{ to } 5.5V,$ $V_{OUT} = \pm 12V, \text{ Drivers disabled}$
RECEIVER INPUTS					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	V <sub>CC</sub> = 3.3V
Input Threshold LOW	0.8	1.5		V	V <sub>CC</sub> = 5.0V
Input Threshold HIGH		1.5	2.4	V	V <sub>CC</sub> = 3.3V
Input Threshold HIGH		1.8	2.4	V	V <sub>CC</sub> = 5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
Auto-Online CIRCUITRY CHAR	ACTERISTIC	CS (ONL	INE = GN	ND, SHUT	FDOWN = V <sub>cc</sub> )
STATUS Output Voltage LOW			0.4	V	I <sub>OUT</sub> = 1.6mA
STATUS Output Voltage HIGH	V <sub>cc</sub> - 0.6			V	I <sub>OUT</sub> = -1.0mA
Receiver Threshold to Drivers Enabled (t <sub>ONLINE</sub> )		200		μS	Figure 15
Receiver Positive or Negative Threshold to STATUS HIGH (t <sub>STSH</sub> )		0.5		μS	Figure 15
Receiver Positive or Negative Threshold to STATUS LOW (t <sub>STSL</sub> )		20		μS	Figure 15

# **SPECIFICATIONS** (continued)

Unless otherwise noted, the following specifications apply for  $V_{CC}$  = +3.0V to +5.5V with  $T_{AMB}$  =  $T_{MIN}$  to  $T_{MAX}$ . Typical values apply at  $V_{CC}$  = +3.3V or +5.0V and  $T_{AMB}$  = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TIMING CHARACTERISTICS					
Maximum Data Rate	460			Kbps	$R_L = 3K\Omega$ , $C_L = 1000pF$ , one driver active
Receiver Propagation Delay $ \begin{matrix} t_{\text{PHL}} \\ t_{\text{PLH}} \end{matrix} $		0.3 0.3		μs	Receiver input to Receiver output, C <sub>L</sub> = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		50	100	ns	t <sub>PHL</sub> - t <sub>PLH</sub>
Receiver Skew		200	1000	ns	t <sub>PHL</sub> - t <sub>PLH</sub>
Transition-Region Slew Rate		60		V/µs	$\label{eq:Vcc} \begin{array}{l} \rm V_{\rm CC} = 3.3V, \ R_L = 3K\Omega, \ T_{\rm AMB} = 25^{\circ}\rm C, \\ \rm measurements \ taken \ from \ -3.0V \ to \ +3.0V \ or \\ \rm +3.0V \ to \ -3.0V \end{array}$

# TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for  $V_{CC}$  = +3.3V, 235Kbps data rate, all drivers loaded with 3k $\Omega$ , 0.1 $\mu$ F charge pump capacitors, and  $T_{AMB}$  = +25°C.

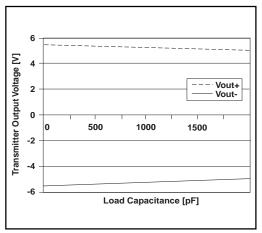


Figure 1. Transmitter Output Voltage VS. Load Capacitance for the SP3223EH

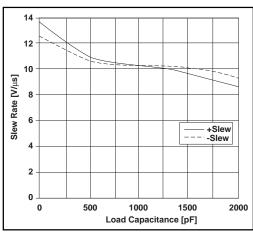


Figure 2. Slew Rate VS. Load Capacitance for the SP3223EH

### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted, the following performance characteristics apply for  $V_{CC}$  = +3.3V, 235Kbps data rate, all drivers loaded with 3k $\Omega$ , 0.1 $\mu$ F charge pump capacitors, and  $T_{AMB}$  = +25°C.

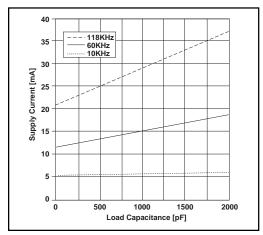


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data for the SP3223EH

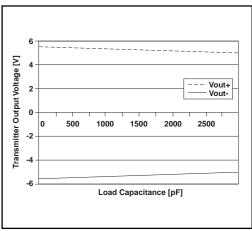


Figure 4. Transmitter Output Voltage VS. Load Capacitance for the SP3243EH

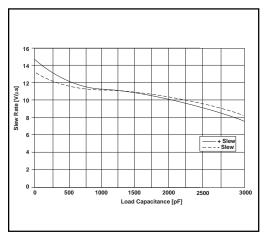


Figure 5. Slew Rate VS. Load Capacitance for the SP3243EH

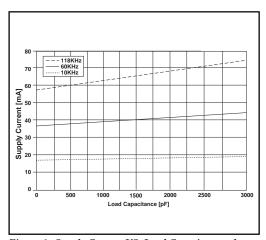


Figure 6. Supply Current VS. Load Capacitance when Transmitting Data for the SP3243EH

NAME	FUNCTION		PIN NUMBER		
NAME	FUNCTION	SP3223EH	SP3243EH		
EN	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state).	1	-		
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	28		
V+	Regulated +5.5V output generated by the charge pump.	3	27		
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	24		
C2+	Positive terminal of the inverting charge-pump capacitor.	5	1		
C2-	Negative terminal of the inverting charge-pump capacitor.	6	2		
V-	Regulated -5.5V output generated by the charge pump.	7	3		
R₁IN	RS-232 receiver input.	16	4		
R <sub>2</sub> IN	RS-232 receiver input.	9	5		
R <sub>3</sub> IN	RS-232 receiver input.	-	6		
R <sub>4</sub> IN	RS-232 receiver input.	-	7		
R₅IN	RS-232 receiver input.	-	8		
R₁OUT	TTL/CMOS receiver output.	15	19		
R₂OUT	TTL/CMOS receiver output.	10	18		
R <sub>2</sub> OUT	Non-inverting receiver-2 output, active in shutdown.	-	20		
R₃OUT	TTL/CMOS receiver output.	-	17		
R₄OUT	TTL/CMOS receiver output.	-	16		
R₅OUT	TTL/CMOS receiver output.	-	15		
STATUS	TTL/CMOS Output indicating online and shutdown status.	11	21		
T <sub>1</sub> IN	TTL/CMOS driver input.	13	14		
T <sub>2</sub> IN	TTL/CMOS driver input.	12	13		
T <sub>3</sub> IN	TTL/CMOS driver input.	-	12		
ONLINE	Apply logic HIGH to override <i>Auto-Online</i> circuitry keeping drivers active (SHUTDOWN must also be logic HIGH, refer to Table 2).	14	23		
T₁OUT	RS-232 driver output.	17	9		
T <sub>2</sub> OUT	RS-232 driver output.	8	10		
T <sub>3</sub> OUT	RS-232 driver output.	-	11		
GND	Ground.	18	25		
V <sub>cc</sub>	+3.0V to +5.5V supply voltage.	19	26		
SHUTDOWN	Apply logic LOW to shut down drivers and charge pump. This overrides all Auto-Online circuitry and ONLINE (refer to Table 2).	20	22		

Table 1. Device Pin Description

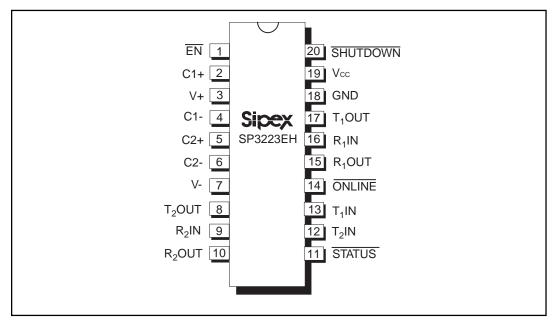


Figure 7. SP3223EH Pinout Configuration

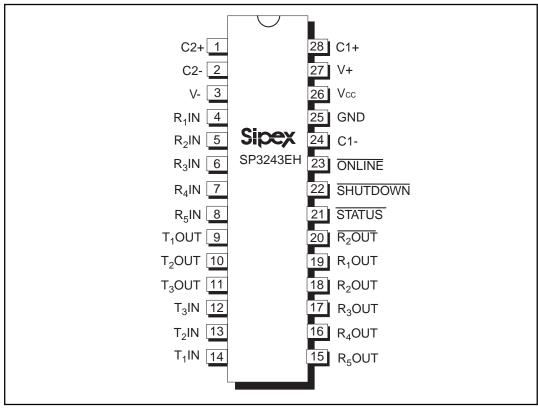


Figure 8. SP3243EH Pinout Configuration

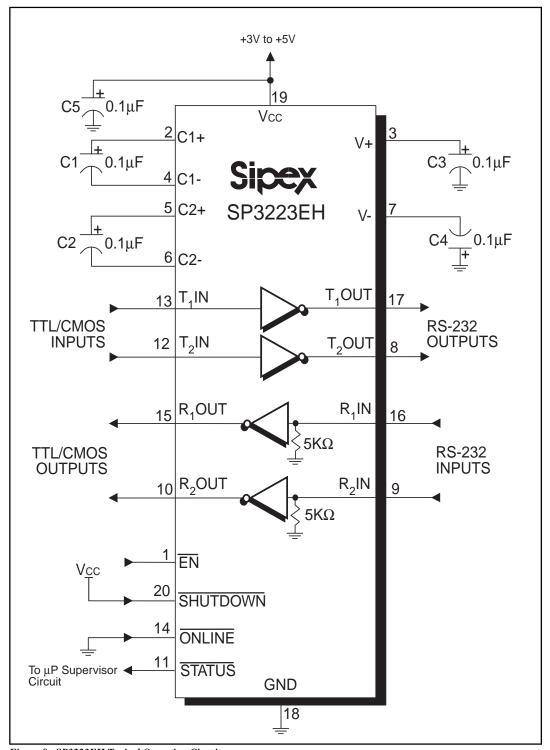


Figure 9. SP3223EH Typical Operating Circuit

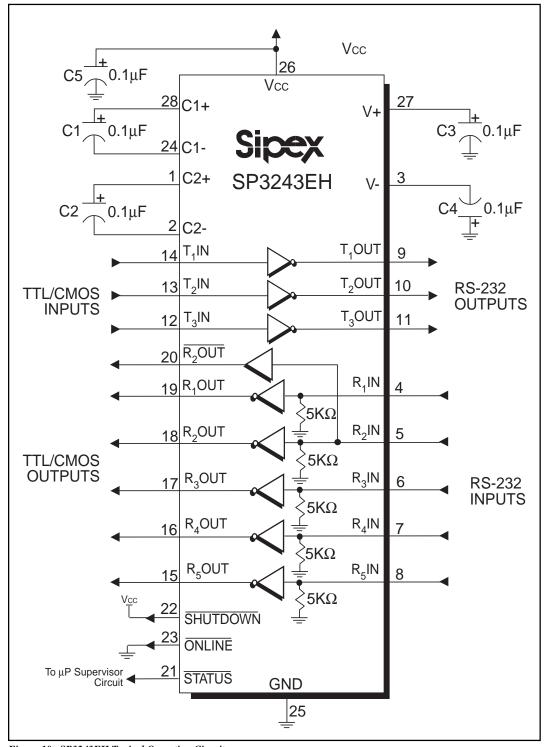


Figure 10. SP3243EH Typical Operating Circuit

#### DESCRIPTION

The **SP3223EH** and **SP3243EH** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3223EH** and **SP3243EH** devices feature **Sipex's** proprietary and patented (U.S.--5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The **SP3223EH** and **SP3243EH** devices can operate at a data rate of 460Kbps fully loaded.

The **SP3223EH** is a 2-driver/2-receiver device, and the **SP3243EH** is a 3-driver/5-receiver device, ideal for portable or hand-held applications. The **SP3243EH** includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where  $V_{\rm CC}$  may be disconnected.

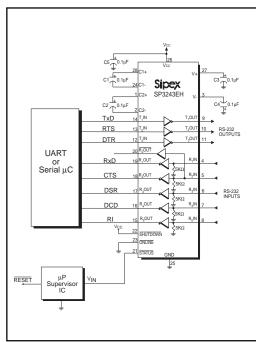


Figure 11. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

The **SP3223EH** and **SP3243EH** series is an ideal choice for power sensitive designs. The **SP3223EH** and **SP3243EH** devices feature *Auto-Online* circuitry which reduces the power supply drain to a 1µA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

#### THEORY OF OPERATION

The **SP3223EH** and **SP3243EH** series is made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. *Auto-Online* circuitry.

#### **Drivers**

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 5.4V$  with no load and  $\pm 5V$  minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions.

The drivers can guarantee a data rate over 460 Kbps fully loaded with  $3 \text{K}\Omega$  in parallel with 1000 pF, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

DEVICE: SP3223EH						
SHUTDOWN	EN	T <sub>x</sub> OUT	R <sub>x</sub> OUT			
0	0	High Z	Active			
0	1	High Z	High Z			
1	0	Active	Active			
1	1	Active	High Z			
DEVICE: SP3243EH						
SHUTDOWN	T <sub>x</sub> OUT	R <sub>x</sub> OUT	R <sub>2</sub> OUT			
0	High Z	High Z	Active			
1	Active	Active	Active			

Table 2.  $\overline{SHUTDOWN}$  and  $\overline{EN}$  Truth Tables Note: In Auto-Online Mode where  $\overline{ONLINE}$  = GND and  $\overline{SHUTDOWN}$  =  $V_{CC}$  the device will shut down if there is no activity present at the Receiver inputs.

The **SP3223EH** and **SP3243EH** drivers can maintain high data rates over 460Kbps fully loaded. *Figure 12* shows a loopback test circuit used to test the RS-232 Drivers. *Figure 13* shows the test results of the loopback circuit with all three drivers active at 120Kbps with typical RS-232 loads in parallel with 1000pF capacitors. *Figure 14* shows the test results where one driver was active at 1Mbps and all three drivers loaded

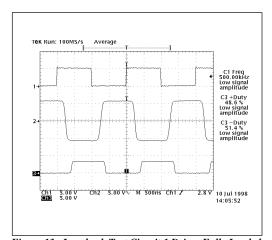


Figure 13. Loopback Test Circuit 1 Driver Fully Loaded

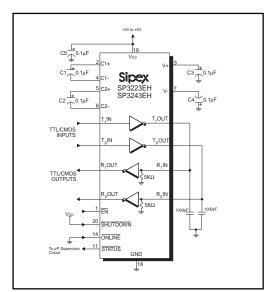


Figure 12. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

with an RS-232 receiver in parallel with a 1000pF capacitor. A superior RS-232 data transmission rate of 1Mbps makes the **SP3223EH/3243EH** series an ideal match for high speed LAN and personal computer peripheral applications.

#### Receivers

The receivers convert  $\pm 5.0$ V EIA/TIA-232 levels to TTL or CMOS logic output levels. All receivers have an inverting output that can be disabled by using the  $\overline{\text{EN}}$  pin.

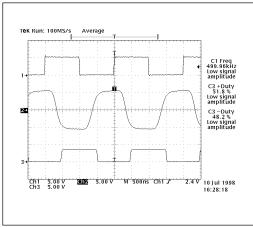


Figure 14. Loopback Test Circuit (All Drivers Fully Loaded)

Receivers are active when the *Auto-Online* circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100µs or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1µA. Driving EN to a logic HIGH forces the outputs of the receivers into high-impedance. The truth table logic of the SP3223EH and SP3243EH driver and receiver outputs can be found in *Table* 2.

The **SP3243EH** includes an additional non-inverting receiver with an output  $\overline{R_2OUT}$ .  $\overline{R_2OUT}$  is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal  $5K\Omega$  pulldown resistor to ground will commit the output of the receiver to a HIGH state.

#### Charge Pump

The charge pump is a **Sipex**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage ( $V_{CC}$ ) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

#### Phase 1

—  $V_{SS}$  charge storage — During this phase of the clock cycle, the positive side of capacitors  $C_1$  and  $C_2$  are initially charged to  $V_{CC}$ .  $C_1^+$  is then switched to GND and the charge in  $C_1^-$  is transferred to  $C_2^-$ . Since  $C_2^+$  is connected to  $V_{CC}$ , the voltage potential across capacitor  $C_2$  is now 2 times  $V_{CC}$ .

#### Phase 2

—  $V_{SS}$  transfer — Phase two of the clock connects the negative terminal of  $C_2$  to the  $V_{SS}$  storage capacitor and the positive terminal of  $C_2$  to GND. This transfers a negative generated voltage to  $C_3$ . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to  $C_3$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND.

#### Phase 3

—  $V_{DD}$  charge storage — The third phase of the clock is identical to the first phase — the charge transferred in  $C_1$  produces  $-V_{CC}$  in the negative terminal of  $C_1$ , which is applied to the negative side of capacitor  $C_2$ . Since  $C_2^+$  is at  $V_{CC}$ , the voltage potential across  $C_2$  is 2 times  $V_{CC}$ .

#### Phase 4

— $V_{DD}$  transfer — The fourth phase of the clock connects the negative terminal of  $C_2$  to GND, and transfers this positive generated voltage across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to  $C_4$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$ , in a no–load condition  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250 kHz. The external capacitors can be as low as  $0.1 \mu F$  with a 16V breakdown voltage rating.

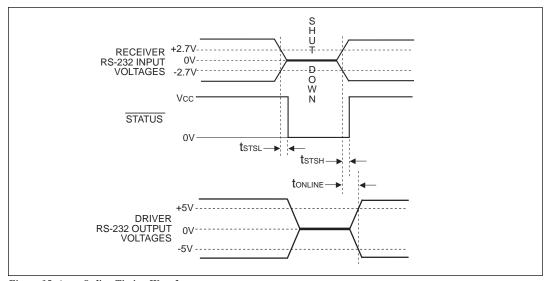


Figure 15. Auto-Online Timing Waveforms

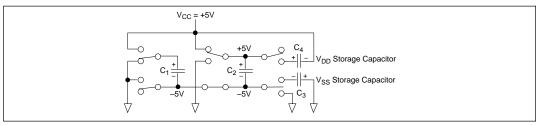


Figure 16. Charge Pump — Phase 1

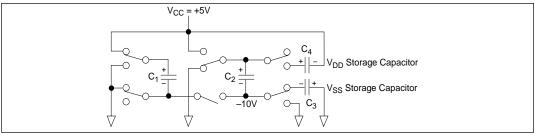


Figure 17. Charge Pump — Phase 2

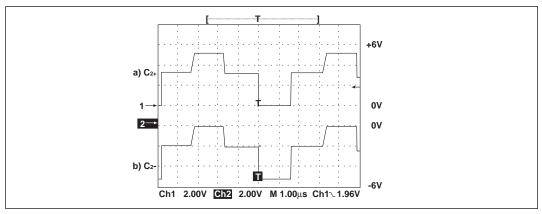


Figure 18. Charge Pump Waveforms

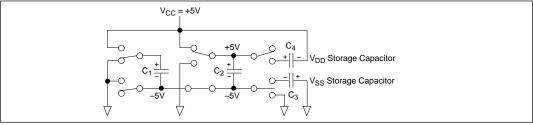


Figure 19. Charge Pump — Phase 3

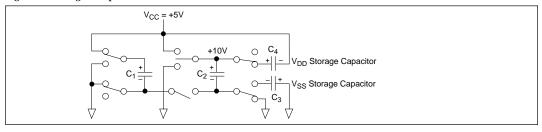


Figure 20. Charge Pump — Phase 4

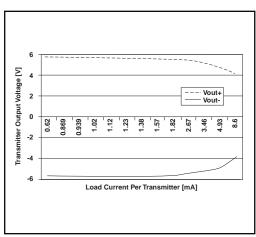


Figure 21. SP3243EH Driver Output Voltages vs. Load Current per Transmitter

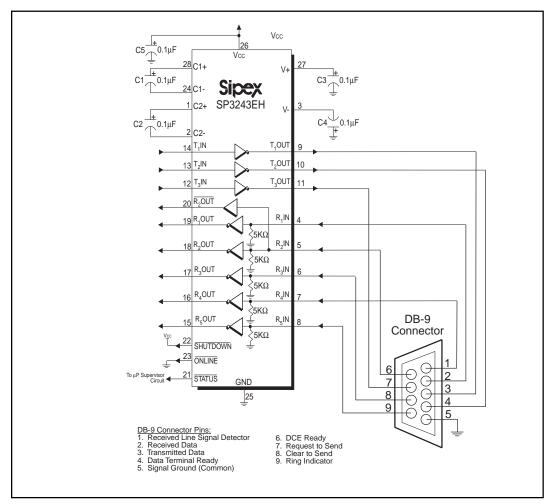


Figure 22. Circuit for the connectivity of the SP3243EH with a DB-9 connector

RS-232 SIGNAL AT RECEIVER INPUT	SHUTDOWN INPUT	ONLINE INPUT	STATUS OUTPUT	TRANSCEIVER STATUS
YES	HIGH	-	HIGH	Normal Operation
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown ( <i>Auto-Online</i> )
YES	LOW	-	HIGH	Shutdown
NO	LOW	-	LOW	Shutdown

Table 3. Auto-Online Logic

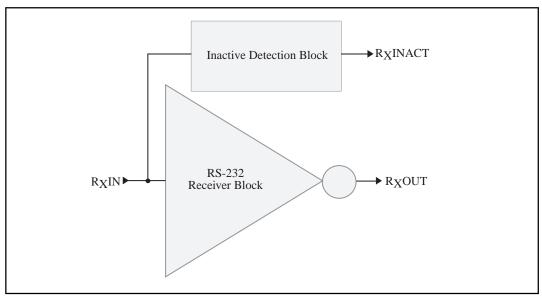


Figure 23. Stage I of Auto-Online Circuitry

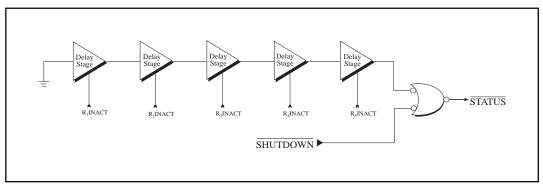


Figure 24. Stage II of Auto-Online Circuitry

## **Auto-Online Circuitry**

The **SP3223EH** and **SP3243EH** devices have a patent pending *Auto-Online* circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SP3223EH and SP3243EH devices incorporate an Auto-Online circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the Auto-Online circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1µA. This function can also be externally controlled by the ONLINE pin. When this pin is tied to a logic LOW, the Auto-Online function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least  $\pm 3V$ , which are generated from the transmitters at the other end of the cable with a +5V minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal  $5k\Omega$  resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standy mode. When ONLINE is HIGH, the Auto-Online mode is disabled.

The Auto-Online circuit has two stages:

- 1) Inactive Detection
- 2) Accumulated Delay

The first stage, shown in *Figure 23*, detects an inactive input. A logic HIGH is asserted on  $R_xINACT$  if the cable is disconnected or the external transmitters are disabled. Otherwise,  $R_xINACT$  will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the *Auto-Online* circuitry, shown in *Figure 24*, processes all the receiver's  $R_x$ INACT signals with an accumulated delay that disables the device to a  $1\mu$ A supply current. The  $\overline{STATUS}$  pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the  $\overline{SHUTDOWN}$  pin is invoked. The typical accumulated delay is around  $20\mu$ s.

When the **SP3223EH** and **SP3243EH** drivers or internal charge pump are disabled, the supply current is reduced to  $1\mu A$ . This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The *Auto-Online* mode can be disabled by the SHUTDOWN pin. If this pin is a logic LOW, the *Auto-Online* function will not operate regardless of the logic state of the ONLINE pin. *Table 3* summarizes the logic of the *Auto-Online* operating modes. The truth table logic of the SP3223EH and SP3243EH driver and receiver outputs can be found in *Table 2*.

The STATUS pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the **SP3223EH** and **SP3243EH** devices are shut down, the charge pumps are turned off. V+ charge pump output decays to  $V_{\rm CC}$ , the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200 $\mu$ s.

For easy programming, the STATUS can be used to indicate DTR or a Ring Indicator signal. Tying ONLINE and SHUTDOWN together will bypass the *Auto-Online* circuitry so this connection acts like a shutdown input pin.

#### **ESD TOLERANCE**

The **SP3223EH/3243EH** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least  $\pm 15$ kV without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC1000-4-2 Air-Discharge
- c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 25*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during

normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 26*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

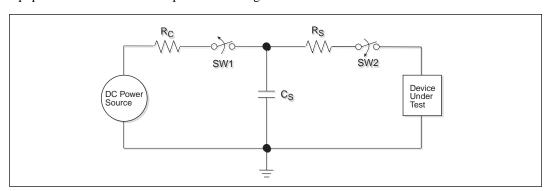


Figure 25. ESD Test Circuit for Human Body Model

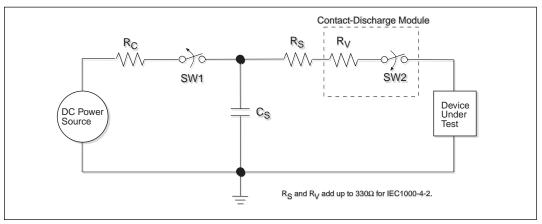


Figure 26. ESD Test Circuit for IEC1000-4-2

The circuit models in Figures 25 and 26 represent the typical ESD testing circuit used for all three methods. The  $C_S$  is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through  $R_S$ , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor ( $R_s$ ) and the source capacitor ( $C_s$ ) are 1.5k $\Omega$  an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor ( $R_s$ ) and the source capacitor ( $C_s$ ) are 330 $\Omega$  an 150pF, respectively.

The higher  $C_s$  value and lower  $R_s$  value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

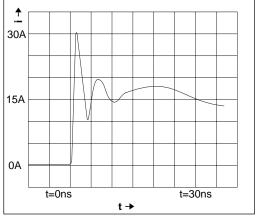
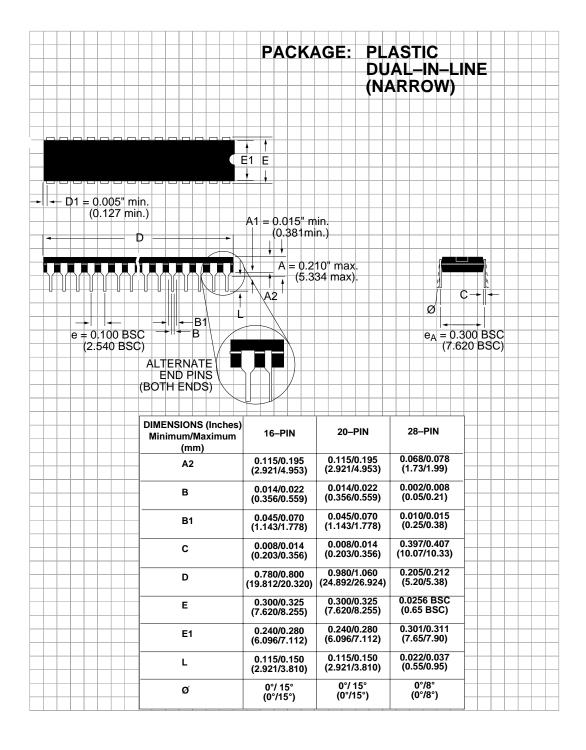
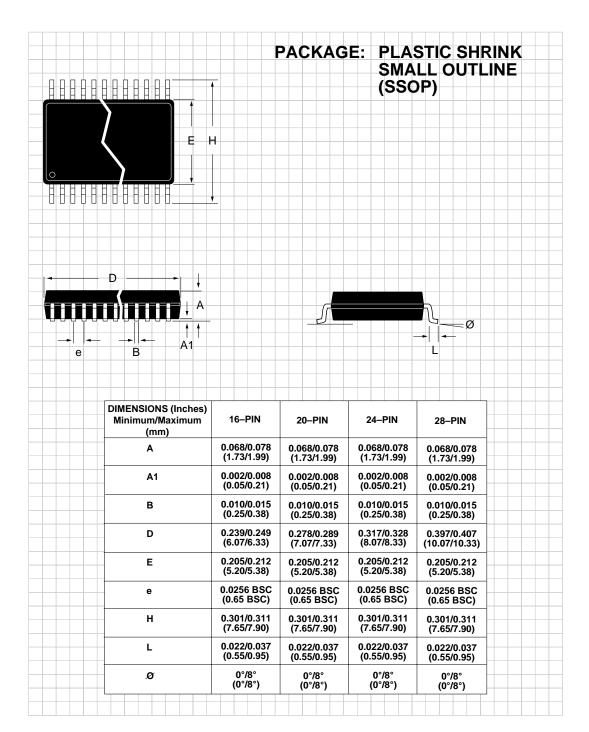


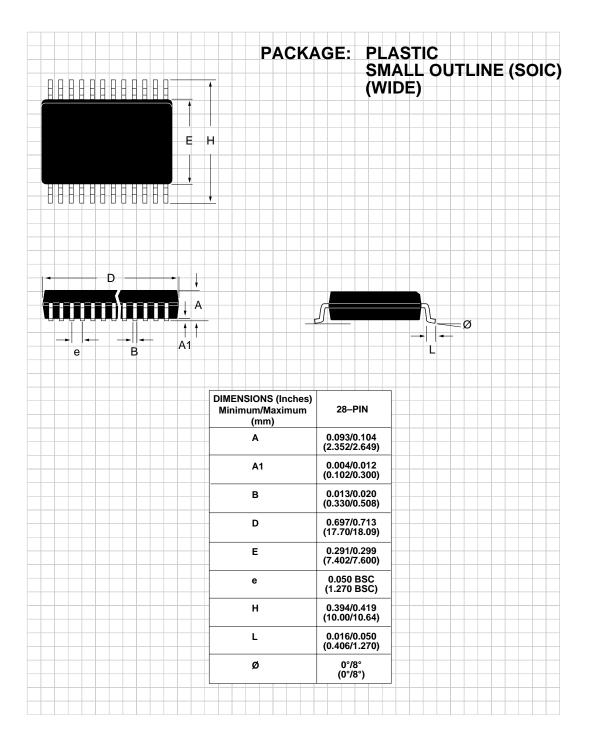
Figure 27. ESD Test Waveform for IEC1000-4-2

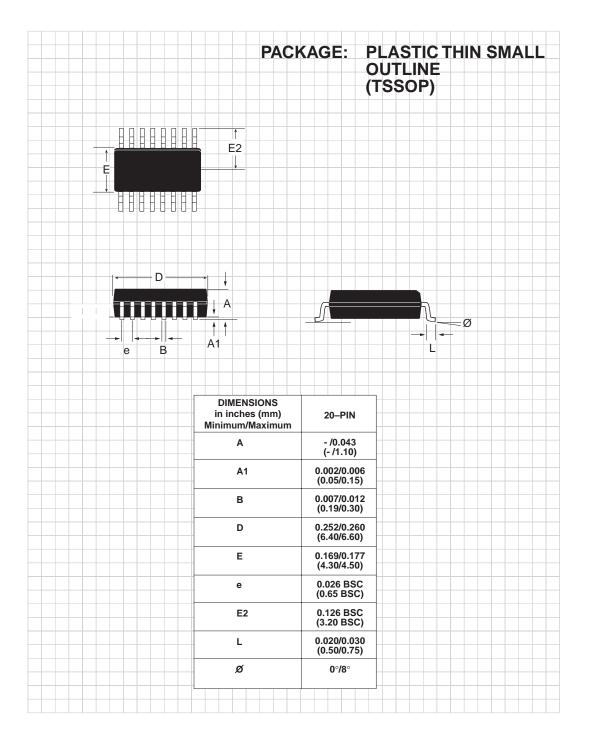
DEVICE PIN TESTED	HUMAN BODY MODEL	Air Discharge	IEC1000-4-2 Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	<u>+</u> 15kV	<u>+</u> 15kV	±8kV	4

Table 4. Transceiver ESD Tolerance Levels









ORDERING INFORMATION					
SP3223EHCA	Temperature Range           0°C to +70°C	20-pin PDIP 20-pin SSOP			
	0°C to +70°C				

Please consult the factory for pricing and availability on a Tape-On-Reel option.



SIGNAL PROCESSING EXCELLENCE

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