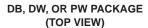
# SN74LVCC3245A-EP OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

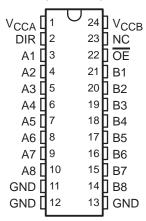
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- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree<sup>†</sup>
- Bidirectional Voltage Translator
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Control Inputs V<sub>IH</sub>/V<sub>IL</sub> Levels Are Referenced to V<sub>CCA</sub> Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17

#### ESD Protection Exceeds JESD 22

- 2000-V Human-Body Model (A114-A)
- 200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)





NC - No internal connection

### description/ordering information

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track  $V_{CCB}$ , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track  $V_{CCA}$ , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so the buses are isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

#### ORDERING INFORMATION

TA	PACKAGE	PACKAGET ORDERABLE PART NUMBER			
	SOIC - DW	Reel of 2000	CLVCC3245AIDWREP	LVCC3245A	
-40°C to 85°C	SSOP - DB	Reel of 2000	CLVCC3245AIDBREP	LH245AEP	
	TSSOP - PW	Reel of 2000	CLVCC3245AIPWREP	LH245AEP	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



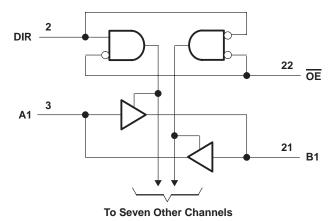
<sup>†</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

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### FUNCTION TABLE (each transceiver)

INP	UTS	ODED ATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CCA</sub> and V <sub>CCB</sub>	–0.5 V to 6 V
Input voltage range, V <sub>I</sub> : All A ports (see Note 1)	$-0.5 \text{ V}$ to $V_{\text{CCA}} + 0.5 \text{ V}$
All B ports (see Note 2)	$-0.5 \text{ V to V}_{CCB} + 0.5 \text{ V}$
Except I/O ports (see Note 1)	-0.5 V to V <sub>CCA</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Note 2): All A ports	-0.5 V to V <sub>CCA</sub> + 0.5 V
All B ports	$-0.5 \text{ V to V}_{CCB} + 0.5 \text{ V}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	
Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DB package	63°C/W
DW package	46°C/W
PW package	
Storage temperature range, T <sub>Stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. This value is limited to 4.6 V maximum.
  - 2. This value is limited to 6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



### SN74LVCC3245A-EP OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS SCAS773A – JUNE 2004 – REVISED MARCH 2005

### recommended operating conditions (see Note 4)

		VCCA	VCCB	MIN	NOM	MAX	UNIT
VCCA	Supply voltage			2.3	3.3	3.6	V
VCCB	Supply voltage			3	5	5.5	V
		2.3 V	3 V	1.7			
.,		2.7 V	3 V	2			.,
$V_{IHA}$	High-level input voltage	3 V	3.6 V	2			V
		3.6 V	5.5 V	2			
		2.3 V	3 V	2			
.,	USala Taras Caras Caras Caras Caras Caras	2.7 V	3 V	2			
VIHB	High-level input voltage	3 V	3.6 V	2			V
		3.6 V	5.5 V	3.85			
		2.3 V	3 V			0.7	
.,	Law law band water		3 V			0.8	V
$V_{ILA}$	Low-level input voltage	3 V	3.6 V			0.8	V
		3.6 V	5.5 V			0.8	
		2.3 V	3 V			0.8	V
.,	Lava lava Caractora Rama	2.7 V	3 V			0.8	
$V_{ILB}$	Low-level input voltage	3 V	3.6 V			0.8	V
		3.6 V	5.5 V			1.65	
		2.3 V	3 V	1.7			
V	High-level input voltage (control pins)	2.7 V	3 V	2			V
$V_{IH}$	(Referenced to V <sub>CCA</sub> )	3 V	3.6 V	2			V
		3.6 V	5.5 V	2			
		2.3 V	3 V			0.7	
V/	Low-level input voltage (control pins)	2.7 V	3 V			0.8	V
$V_{IL}$	(Referenced to V <sub>CCA</sub> )	3 V	3.6 V			0.8	V
		3.6 V	5.5 V			0.8	
$V_{IA}$	Input voltage			0		VCCA	V
$V_{IB}$	Input voltage			0		VCCB	V
$V_{OA}$	Output voltage			0		VCCA	V
VOB	Output voltage			0		VCCB	V

NOTE 4: All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### SN74LVCC3245A-EP OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS SCAS773A – JUNE 2004 – REVISED MARCH 2005

### recommended operating conditions (see Note 4) (continued)

		VCCA	VCCB	MIN	NOM	MAX	UNIT
		2.3 V	3 V			-8	
IOHA	High-level output current	2.7 V	3 V			-12	mA
		3.3 V	3 V			-24	
		2.3 V	3.3 V			-12	
IOHB	High-level output current	2.7 V	3.3 V			-12	mA
		3.3 V	3 V			-24	
		2.3 V	3 V			8	
IOLA	Low-level output current	2.7 V	3 V			12	mA
		3.3 V	3 V			24	
		2.3 V	3.3 V			12	
IOLB	Low-level output current	2.7 V	3.3 V			12	mA
		3.3 V	3 V			24	
Δt/Δν	Input transition rise or fall rate					10	ns/V
T <sub>A</sub>	Operating free-air temperature			-40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



### SN74LVCC3245A-EP OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS SCAS773A – JUNE 2004 – REVISED MARCH 2005

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCCA	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	3 V	3 V	2.9	3		
		$I_{OH} = -8 \text{ mA}$	2.3 V	3 V	2			
		10	2.7 V	3 V	2.2	2.5		
$V_{OHA}$		I <sub>OH</sub> = −12 mA	3 V	3 V	2.4	2.8		V
		04 4	3 V	3 V	2.2	2.6		
		I <sub>OH</sub> = -24 mA	2.7 V	4.5 V	2	2.3		
		$I_{OH} = -100 \mu\text{A}$	3 V	3 V	2.9	3		
		Jan. 12 mA	2.3 V	3 V	2.4			
Vонв		I <sub>OH</sub> = -12 mA	2.7 V	3 V	2.4	2.8		V
		Jan. 24 mA	3 V	3 V	2.2	2.6		
		I <sub>OH</sub> = -24 mA	2.7 V	4.5 V	3.2	4.2		
		$I_{OL} = 100 \mu\text{A}$	3 V	3 V			0.1	
		$I_{OL} = 8 \text{ mA}$	2.3 V	3 V			0.6	
VOLA		$I_{OL} = 12 \text{ mA}$	2.7 V	3 V		0.1	0.5	V
		la. 24 mA	3 V	3 V		0.2	0.5	
		I <sub>OL</sub> = 24 mA	2.7 V	4.5 V		0.2	0.5	
		$I_{OL} = 100 \mu\text{A}$	3 V	3 V			0.1	
N/		$I_{OL} = 12 \text{ mA}$	2.3 V	3 V			0.4	V
$V_{OLB}$			3 V	3 V		0.2	0.5	V
		I <sub>OL</sub> = 24 mA	3 V	4.5 V		0.2	0.5	
1.	Control inputs	W = Voos or CND	3.6 V	3.6 V		±0.1	±1	^
l <sub>l</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.0 V	5.5 V		±0.1	±1	μΑ
$loz^{\dagger}$	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or $V_{IH}$	3.6 V	3.6 V		±0.5	±5	μΑ
		A port = $V_{CCA}$ or GND, $I_{O} = 0$	3.6 V	Open		5	50	
ICCA	B to A	Brant V m CND I 0	0.01/	3.6 V		5	50	μΑ
		B port = $V_{CCB}$ or GND, $I_{O} = 0$	3.6 V	5.5 V		5	50	
		A	0.01/	3.6 V		5	50	
ICCB	A to B	A port = $V_{CCA}$ or GND, $I_{O} = 0$	3.6 V	5.5 V		8	80	μА
	A port	$\frac{V_L}{OE}$ = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, $\frac{V_C}{OE}$ at GND and DIR at V <sub>CCA</sub>	3.6 V	3.6 V		0.35	0.5	
ΔI <sub>CCA</sub> ‡	ŌĒ	V <sub>I</sub> = V <sub>CCA</sub> - 0.6 V, Other inputs at V <sub>CCA</sub> or GND, DIR at V <sub>CCA</sub>	3.6 V	3.6 V		0.35	0.5	mA
	DIR	$\frac{V_L}{OE}$ = V <sub>CCA</sub> - 0.6 V, Other inputs at V <sub>CCA</sub> or GND,	3.6 V	3.6 V		0.35	0.5	
ΔI <sub>CCB</sub> ‡	B port	$V_L$ = V <sub>CCB</sub> – 2.1 V, Other inputs at V <sub>CCB</sub> or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
Ci	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	Open	Open		4		pF
Cio	A or B ports	VO = VCCA/B or GND	3.3 V	5 V		18.5		pF



<sup>†</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V<sub>CC</sub>.

### SN74LVCC3245A-EP OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER			$V_{\text{CCA}} = 2.5 \text{ V} \\ \pm 0.2 \text{ V}, \\ V_{\text{CCB}} = 3.3 \text{ V} \\ \pm 0.3 \text{ V}$		V <sub>CCA</sub> = 2.7 V TO 3.6 V, V <sub>CCB</sub> = 5 V ± 0.5 V		V <sub>CCA</sub> = 2.7 V TO 3.6 V, V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> PHL	•	c c	1	9.4	1	6	1	7.1	
<sup>t</sup> PLH	А	В	1	9.1	1	5.3	1	7.2	ns
<sup>t</sup> PHL	В	٨	1	11.2	1	5.8	1	6.4	20
<sup>t</sup> PLH		Α	1	9.9	1	7	1	7.6	ns
tPZL	ŌĒ	^	1	14.5	1	9.2	1	9.7	
<sup>t</sup> PZH	OE	А	1	12.9	1	9.5	1	9.5	ns
t <sub>PZL</sub>	<u>OE</u>	c c	1	13	1	8.1	1	9.2	
<sup>t</sup> PZH	OE	В	1	12.8	1	8.4	1	9.9	ns
tPLZ	ŌĒ		1	7.1	1	7	1	6.6	
<sup>t</sup> PHZ	OE	А	1	6.9	1	7.8	1	6.9	ns
tpLZ	ŌĒ		1	8.8	1	7.3	1	7.5	
<sup>t</sup> PHZ	OE	В	1	8.9	1	7	1	7.9	ns

### operating characteristics, V<sub>CCA</sub> = 3.3 V, V<sub>CCB</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER				ONDITIONS	TYP	UNIT
O Bound discharge to a second second second		Outputs enabled	0 50	4 40 MH-	38	
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50,$	f = 10 MHz	4.5	pΕ

### power-up considerations†

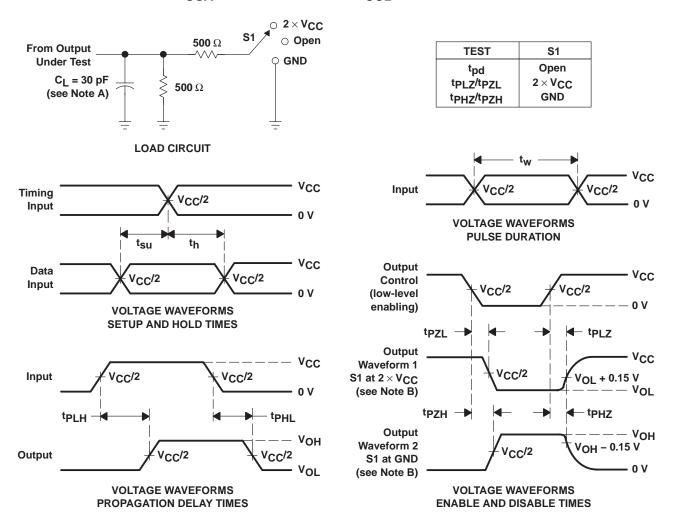
TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. To guard against such power-up problems, take these precautions:

- 1. Connect ground before any supply voltage is applied.
- 2. Power up the control side of the device (V<sub>CCA</sub> for all four of these devices).
- 3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
- 4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

<sup>†</sup> Refer to the TI application report, Texas Instruments Voltage-Level-Translation Devices, literature number SCEA021.



# PARAMETER MEASUREMENT INFORMATION FOR A PORT $V_{CCA}$ = 2.5 V $\pm$ 0.2 V AND $V_{CCB}$ = 3.3 V $\pm$ 0.3 V



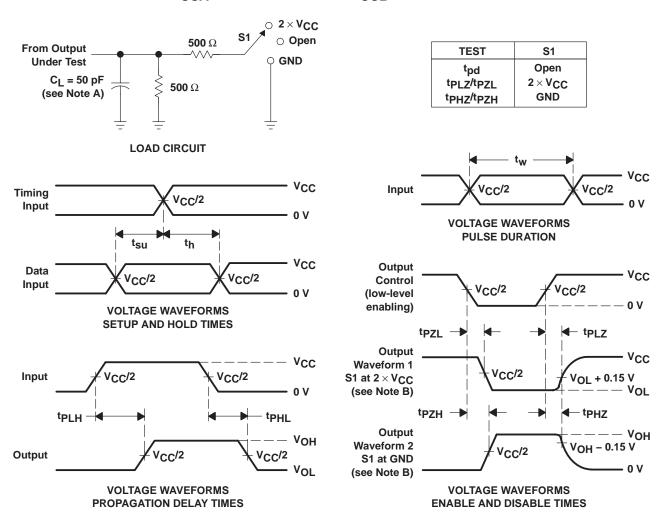
NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50~\Omega$ ,  $t_f \leq$  2 ns.  $t_f \leq$  2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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# PARAMETER MEASUREMENT INFORMATION FOR B PORT $V_{CCA}$ = 2.5 V $\pm$ 0.2 V AND $V_{CCB}$ = 3.3 V $\pm$ 0.3 V



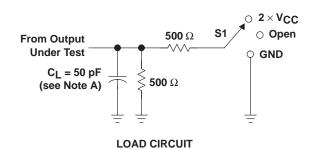
NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50~\Omega$ ,  $t_f \leq$  2 ns,  $t_f \leq$  2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

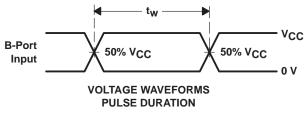
Figure 2. Load Circuit and Voltage Waveforms

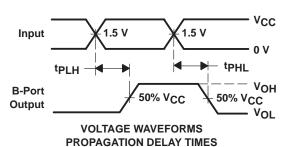


# PARAMETER MEASUREMENT INFORMATION FOR B PORT $V_{CCA} = 3.6 \text{ V}$ AND $V_{CCB} = 5.5 \text{ V}$

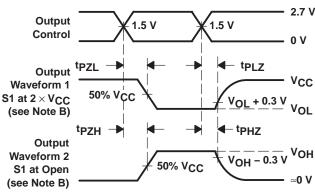


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	Open





**NONINVERTING OUTPUTS** 



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

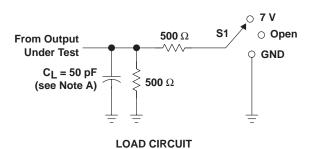
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

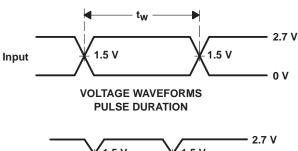
Figure 3. Load Circuit and Voltage Waveforms

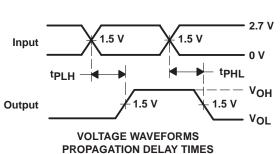
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# PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT $V_{CCA}$ AND $V_{CCB} = 3.6 \text{ V}$

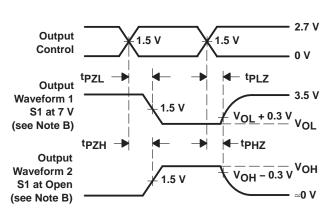


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	7 V
tPHZ/tPZH	Open





NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50~\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns,
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms







30-Jan-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CLVCC3245AIDBREP	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CLVCC3245AIDWREP	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CLVCC3245AIPWREP	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
V62/05602-01XE	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
V62/05602-01YE	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
V62/05602-01ZE	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### **PACKAGE OPTION ADDENDUM**

30-Jan-2012

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVCC3245A-EP:

Catalog: SN74LVCC3245A

www.ti.com

NOTE: Qualified Version Definitions:

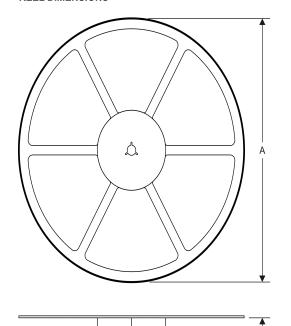
Catalog - TI's standard catalog product

### PACKAGE MATERIALS INFORMATION

www.ti.com 28-Jan-2012

### TAPE AND REEL INFORMATION

### **REEL DIMENSIONS**



### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVCC3245AIDBREP	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CLVCC3245AIDWREP	SOIC	DW	24	2000	330.0	24.4	10.85	15.8	2.7	12.0	24.0	Q1
CLVCC3245AIPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVCC3245AIDBREP	SSOP	DB	24	2000	346.0	346.0	33.0
CLVCC3245AIDWREP	SOIC	DW	24	2000	346.0	346.0	41.0
CLVCC3245AIPWREP	TSSOP	PW	24	2000	346.0	346.0	33.0

DW (R-PDSO-G24)

### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



PW (R-PDSO-G24)

### PLASTIC SMALL OUTLINE



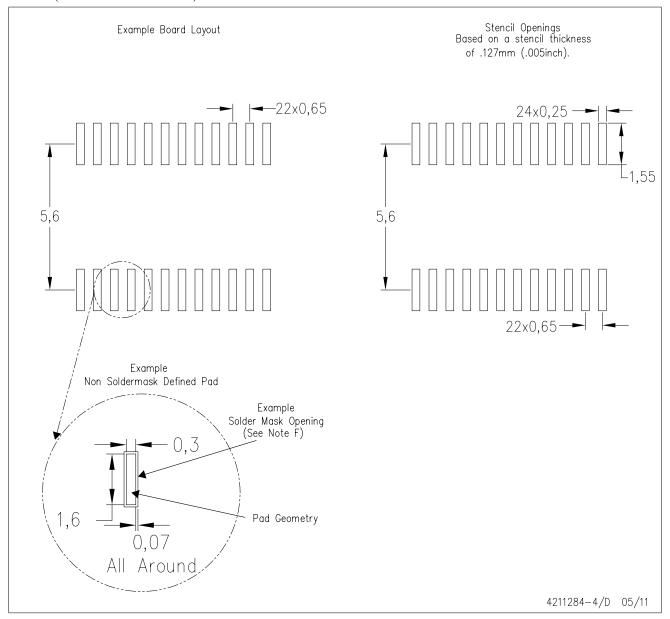
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



### PW (R-PDSO-G24)

### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### DB (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE

### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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