

# SDIO, UART, AND AUDIO VOLTAGE-TRANSLATION TRANSCEIVER

Check for Samples: TWL1200

#### **FEATURES**

- Level Translator
  - V<sub>CCA</sub> and V<sub>CCB</sub> Range of 1.1 V to 3.6 V
- Seamlessly Bridges 1.8-V/2.6-V
   Digital-Switching Compatibility Gap Between 2.6-V processors and Tl's Wi-Link (WL1271 and WL1273)

YFF PACKAGE (TOP VIEW)

		1	2	3	4	5	6	7	
Α			$\bigcirc$	$\circ$	$\circ$	$\circ$	$\circ$	$\circ$	
В		)	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
С		)	()	()	()	$\bigcirc$	$\bigcirc$	$\bigcirc$	
D		)	$\bigcirc$	$\bigcirc$	()	$\bigcirc$	$\bigcirc$	$\bigcirc$	
Е	(	)	()	()	()	()	$\bigcirc$	$\bigcirc$	
F		)	$\bigcirc$	$\bigcirc$	()	()	$\bigcirc$	$\bigcirc$	
G		)	()	()	()	()	()	$\bigcirc$	

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2500-V Human-Body Model (A114-B)
  - 250-V Machine Model (A115-A)
  - 1500-V Charged-Device Model (C101)

ZQC PACKAGE (TOP VIEW)

	1	2	3	4	5	6	7
Α	$\bigcirc$	()	$\bigcirc$	()	()	()	$\bigcirc$
В	()	()	()	()	()	()	()
С	()	()		()	()	()	()
D	()	()	()	()	()	()	()
Ε	()	()	()	()	()	()	$\bigcirc$
F	()	()	()	()	()	()	$\bigcirc$
G	()	()	()	()	()	()	$\bigcirc$

## **BGA PACKAGE TERMINAL ASSIGNMENTS**

	1	2	3	4	5	6	7
Α	SDIO_CLK(A)	SDIO_CMD(A)	AUDIO_CLK(A)	AUD_DIR	AUDIO_CLK(B)	SDIO_CMD(B)	SDIO_CLK(B)
В	SDIO_DATA3(A)	SDIO_DATA0(A)	AUDIO_F-SYN(A)	ŌĒ	AUDIO_F-SYN(B)	SDIO_DATA0(B)	SDIO_DATA3(B)
С	SDIO_DATA2(A)	SDIO_DATA1(A)		V <sub>CCA</sub>	V <sub>CCB</sub>	SDIO_DATA1(B)	SDIO_DATA2(B)
D	WLAN_EN(A)	WLAN_IRQ(A)	GND	V <sub>CCA</sub>	V <sub>CCB</sub>	WLAN_EN(B)	WLAN_IRQ(B)
E	CLK_REQ(A)	BT_EN(A)	GND	GND	GND	BT_EN(B)	CLK_REQ(B)
F	BT_UART_CTS(A)	BT_UART_RTS(A)	AUDIO_IN(A)	SLOW_CLK(B)	AUDIO_IN(B)	BT_UART_RTS(B)	BT_UART_CTS(B)
G	BT_UART_RX(A)	BT_UART_TX(A)	AUDIO_OUT(A)	SLOW_CLK(A)	AUDIO_OUT(B)	BT_UART_TX(B)	BT_UART_RX(B)

#### WCS PACKAGE TERMINAL ASSIGNMENTS

	1	2	3	4	5	6	7
Α	SDIO_CLK(A)	SDIO_CMD(A)	AUDIO_CLK(A)	AUD_DIR	AUDIO_CLK(B)	SDIO_CMD(B)	SDIO_CLK(B)
В	SDIO_DATA3(A)	SDIO_DATA0(A)	AUDIO_F-SYN(A)	ŌĒ	AUDIO_F-SYN(B)	SDIO_DATA0(B)	SDIO_DATA3(B)
С	SDIO_DATA2(A)	SDIO_DATA1(A)	NC <sup>(1)</sup>	V <sub>CCA</sub>	V <sub>CCB</sub>	SDIO_DATA1(B)	SDIO_DATA2(B)
D	WLAN_EN(A)	WLAN_IRQ(A)	GND	V <sub>CCA</sub>	V <sub>CCB</sub>	WLAN_EN(B)	WLAN_IRQ(B)
E	CLK_REQ(A)	BT_EN(A)	GND	GND	GND	BT_EN(B)	CLK_REQ(B)
F	BT_UART_CTS(A)	BT_UART_RTS(A)	AUDIO_IN(A)	SLOW_CLK(B)	AUDIO_IN(B)	BT_UART_RTS(B)	BT_UART_CTS(B)
G	BT_UART_RX(A)	BT_UART_TX(A)	AUDIO_OUT(A)	SLOW_CLK(A)	AUDIO_OUT(B)	BT_UART_TX(B)	BT_UART_RX(B)

(1) NC - No internal connection



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#### **DESCRIPTION/ORDERING INFORMATION**

The TWL1200 is an 19-bit voltage translator specifically designed to seamlessly bridge the 1.8-V/2.6-V digital-switching compatibility gap between 2.6-V baseband and the TI Wi-Link-6 (WL1271/3). It is optimized for SDIO, UART, and audio functions. The TWL1200 has two supply-voltage pins,  $V_{CCA}$  and  $V_{CCB}$ , that can be operated over the full range of 1.1 V to 3.6 V. The TWL1200 enables system designers to easily interface applications processors or digital basebands to peripherals operating at a different I/O voltage levels, such as the TI Wi-Link-6 (WL1271/3) or other SDIO/memory cards.

The TWL1200 is offered in both 48-ball 0.5-mm ball grid array (BGA) and 49-bump 0.4-mm wafer chip scale package (WCSP) packages. Low static power consumption and small package size make the TWL1200 an ideal choice for mobile-phone applications.

#### ORDERING INFORMATION(1)

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
40°C to 95°C	BGA MicroStar Junior™ – ZQC (Pb-free)	Tape and reel	TWL1200ZQCR	YW200
–40°C to 85°C	WCSP ™ – YFF (Pb-free)	Tape and reel	TWL1200YFFR	YW200

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

#### **TERMINAL FUNCTIONS**

	TERM	MINAL		
ZQC BALL NO.	YFF BUMP NO.	NAME	TYPE	DESCRIPTION
C4, D4	C4, D4	$V_{CCA}$	Power	A-side supply voltage (1.1 V to 3.6 V)
B2	B2	SDIO_DATA0(A)	I/O	Data bit 1 connected to baseband SDIO controller
C2	C2	SDIO_DATA1(A)	I/O	Data bit 2 connected to baseband SDIO controller
C1	C1	SDIO_DATA2(A)	I/O	Data bit 3 connected to baseband SDIO controller
B1	B1	SDIO_DATA3(A)	I/O	Data bit 4 connected to baseband SDIO controller
A2	A2	SDIO_CMD(A)	I/O	Command bit connected to baseband SDIO controller. Referenced to V <sub>CCA</sub> .
A6	A6	SDIO_CMD(B)	I/O	Command bit connected to SD/SDIO peripheral. Includes a 15-k $\Omega$ pullup resistor to $V_{CCB}$ .
D3, E3, E4, E5	D3, E3, E4, E5	GND		Ground
B6	В6	SDIO_DATA0(B)	I/O	Data bit 1 connected to SD/SDIO peripheral
C6	C6	SDIO_DATA1(B)	I/O	Data bit 2 connected to SD/SDIO peripheral
C7	C7	SDIO_DATA2(B)	I/O	Data bit 3 connected to SD/SDIO peripheral
В7	В7	SDIO_DATA3(B)	I/O	Data bit 4 connected to SD/SDIO peripheral
A1	A1	SDIO_CLK(A)	I	Clock signal connected to baseband SDIO controller. Referenced to V <sub>CCA</sub> .
A7	A7	SDIO_CLK(B)	0	Clock signal connected to SD/SDIO peripheral. Referenced to $V_{CCB}$ ; drive strength = 8 mA
C5, D5	C5, D5	V <sub>CCB</sub>	Pwr	B-side supply voltage (1.1 V to 3.6 V)
СЗ	C3	-	_	No ball (for ZQC) and No-Connect (for YFF)
B4	B4	ŌĒ	I	Output enable (active low)
A4	A4	AUD_DIR	I	Direction control signal for AUDIO_CLK and AUDIO_F-SYNC signals
G3	G3	AUDIO_OUT(A)	0	Connected to baseband audio subsystem; drive strength = 4 mA
G5	G5	AUDIO_OUT(B)	I	Connected to Wi-Link-6 PCM subsystem
D1	D1	WLAN_EN(A)	I	Connected to baseband SDIO controller
D6	D6	WLAN_EN(B)	0	Connected to SD/SDIO peripheral; drive strength = 2 mA
G2	G2	BT_UART_TX(A)	0	Connected to baseband UART subsystem; drive strength = 8 mA
G6	G6	BT_UART_TX(B)	ı	Connected to BT UART subsystem of Wi-Link-6
D2	D2	WLAN_IRQ(A)	0	Connected to baseband SDIO controller; drive strength = 4 mA



# **TERMINAL FUNCTIONS (continued)**

	TERI	MINAL		
ZQC BALL NO.	YFF BUMP NO.	NAME	TYPE	DESCRIPTION
D7	D7	WLAN_IRQ(B)	1	Connected to SD/SDIO peripheral
G4	G4	SLOW_CLK(A)	1	Low frequency 32-kHz clock connected to baseband device
F4	F4	SLOW_CLK(B)	0	Low frequency 32-kHz clock connected to Wi-Link-6 device; drive strength = 2 mA
G1	G1	BT_UART_RX(A)	1	Connected to baseband UART subsystem
G7	G7	BT_UART_RX(B)	0	Connected to BT UART subsystem of Wi-Link-6; drive strength = 8 mA
E1	E1	CLK_REQ(A)	0	Connected to baseband SDIO controller; drive strength = 4 mA
E7	E7	CLK_REQ(B)	1	Connected to SD/SDIO peripheral
F1	F1	BT_UART_CTS(A)	1	Connected to baseband UART subsystem
F3	F3	AUDIO_IN(A)	1	Connected to baseband audio subsystem
F5	F5	AUDIO_IN(B)	0	Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA
А3	A3	AUDIO_CLK(A)	I/O	Connected to baseband audio subsystem; drive strength = 4 mA
A5	A5	AUDIO_CLK(B)	I/O	Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA
E2	E2	BT_EN(A)	1	Connected to baseband UART subsystem
E6	E6	BT_EN(B)	0	Connected to BT UART subsystem of Wi-Link-6; drive strength = 2 mA
F7	F7	BT_UART CTS(B)	0	Connected to BT UART subsystem of Wi-Link-6; drive strength = 4 mA
F2	F2	BT_UART RTS(A)	0	Connected to baseband UART subsystem; drive strength = 4 mA
F6	F6	BT_UART RTS(B)	1	Connected to BT UART subsystem of Wi-Link-6
В3	В3	AUDIO_F-SYN(A)	I/O	Connected to baseband audio subsystem; drive strength = 4 mA
B5	B5	AUDIO_F-SYN(B)	I/O	Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA

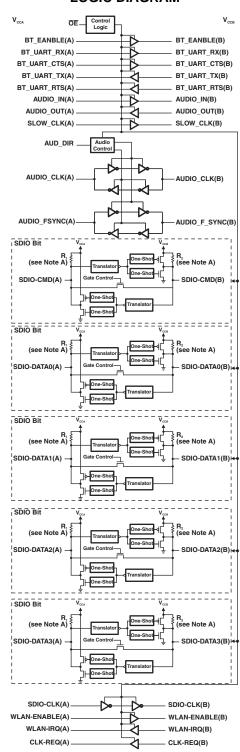
**Table 1. FUNCTION TABLE** 

CONTRO	L INPUTS	OPERATION
ŌE	AUD_DIR	
Н	Х	All outputs are Hi-Z
L	Н	AUDIO_CLK(A) to AUDIO_CLK(B) and AUDIO_F-SYNC(A) to AUDIO_F-SYNC(B)
L	L	AUDIO_CLK(B) to AUDIO_CLK(A) and AUDIO_F-SYNC(B) to AUDIO_F-SYNC(A)

Product Folder Link(s): TWL1200



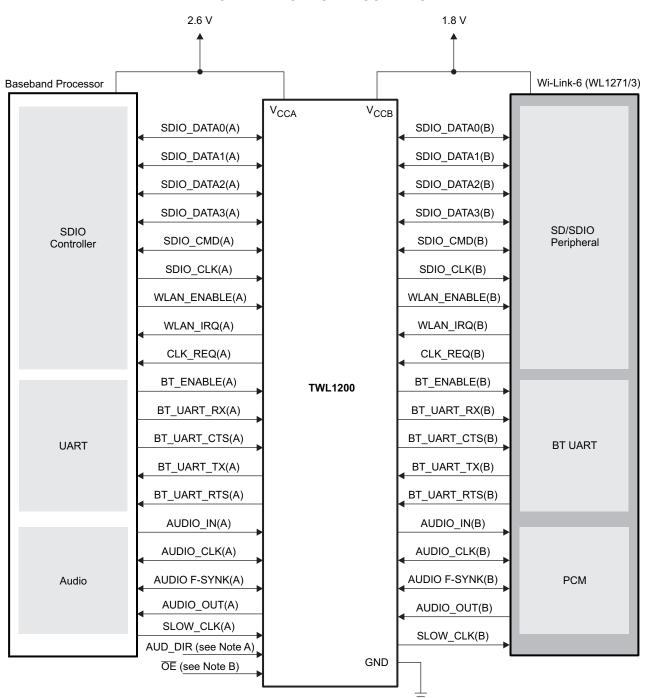
# **LOGIC DIAGRAM**



- A. R<sub>1</sub> and R<sub>2</sub> resistor values are determined based upon the logic level applied to the A port or B port as follows:
  - $R_1$  and  $R_2$  = 25 k $\Omega$  when a logic level low is applied to the A port or B port.
  - $R_1$  and  $R_2$  = 4 k $\Omega$  when a logic level high is applied to the A port or B port.
  - $R_1$  and  $R_2$  = 70 k $\Omega$  when the port is deselected (or in High-Z or 3-state).
- B.  $\overline{OE}$  controls all output buffers. When  $\overline{OE}$  = high, all outputs are Hi-Z.



#### TYPICAL APPLICATION BLOCK DIAGRAM



- A. AUD\_DIR must be biased to determine audio direction (see Function Table for properly establishing the bias).
- B.  $\overline{OE}$  is an active-low pin that must be grounded to 0 V to enable operation of the TWL1200 device.



# ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
$V_{CCA}$	Supply voltage range		-0.5	4.6	V	
$V_{CCB}$	Supply voltage range		-0.5	4.6	V	
		I/O ports (A port)	-0.5	4.6	V	
$V_{I}$	Input voltage range	I/O ports (B port)	-0.5	4.6		
		Control inputs	-0.5	4.6		
V	Voltage range applied to any output in the high-impedance or power-off	A port	-0.5	4.6	V	
Vo	state (2)	B port	-0.5	4.6		
V	Valtage value and indicate any systems in the bight on law state (2)	A port	-0.5	4.6	4.6 V	
Vo	Voltage range applied to any output in the high or low state (2)	B port	-0.5	4.6 4.6	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA	
Io	Continuous output current			±50	mA	
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA	
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating" conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### THERMAL IMPEDANCE RATINGS

			UNIT
۵	Package thermal impedance <sup>(1)</sup>	ZQC package 171.6	°C/W
$\Theta_{JA}$	rackage thermal impedance V	YFF package 75	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.



# RECOMMENDED OPERATING CONDITIONS(1)

			V <sub>CCI</sub>	V <sub>cco</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.1	3.6	V
V <sub>CCB</sub>	Supply voltage				1.1	3.6	V
.,	LP ale Level Count on the sec	Buffer type	4.4.)//- 0.0.)/	4.4.7/1- 0.0.7/	V <sub>CCI</sub> × 0.65	3.6	
$V_{IH}$	High-level input voltage	OE and AUD_DIR	1.1 V to 3.6 V	1.1 V to 3.6 V	1.1 3. 1.	3.6	V
V <sub>IH</sub>	High-level input voltage	Switch type	1.1 V to 3.6 V	1.1 V to 3.6 V	V <sub>CCI</sub> - 0.2	V <sub>CCI</sub>	V
V <sub>IL</sub>	Low-level input voltage	Buffer type and Control Logic	1.1 V to 3.6 V	1.1 V to 3.6 V	0	V <sub>CCI</sub> × 0.35	V
		OE and AUD_DIR			0	0 V <sub>CCI</sub> × 0.35 0 V <sub>CCA</sub> × 0.35 0 0.15 0 3.6 0 V <sub>CCO</sub> 0 3.6 -0.5 -1	
$V_{IL}$ (2)	Low-level input voltage	Switch type	1.1 V to 3.6 V	1.1 V to 3.6 V	0	0.15	V
VI	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	$V_{CCO}$	V
		3-state			0	3.6	v
				1.1 V to 1.3 V		-0.5	
				1.4 V to 1.6 V		-1	mA
$I_{OH}$	High-level output current			1.65 V to 1.95 V		-2	
				2.3 V to 2.7 V		-4	
				3 V to 3.6 V		-8	
				1.1 V to 1.3 V		0.5	
				1.4 V to 1.6 V		1	
$I_{OL}$	Low-level output current			1.65 V to 1.95 V		2	mA
				2.3 V to 2.7 V		4	
				3 V to 3.6 V		8	
Δt/Δν	Input transition rise or fall ra	ate				5	ns/V
T <sub>A</sub>	Operating free-air temperat	ure			-40	85	°C

All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. Note, the max  $V_{IL}$  value is provided to ensure that a valid  $V_{OL}$  is maintained. The  $V_{OL}$  value is the  $V_{IL}$  + the voltage-drop across the pass-gate transistor. (1)

Product Folder Link(s): TWL1200



# **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(1)</sup> MAX	UNIT
	A port	$I_{OH} = -100 \mu A$	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{\rm CCO}-0.2$		
	(Buffer-type output,	$I_{OH} = -8 \text{ mA}$	1.65 V	1.65 V	1.2		
/ <sub>~</sub>	8-mA drive)	IOH = -0 IIIA	2.5 V	2.5 V	1.97		V
/ <sub>OH</sub>	A port	$I_{OH} = -100 \mu A$	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{\text{CCO}} - 0.2$		V
	(Buffer-type output,	$I_{OH} = -4 \text{ mA}$	1.65 V	1.65 V	1.2		
	4-mA drive)	IOH = -4 IIIA	2.5 V	2.5 V	1.97		
,	A port		1.65 V	1.65 V	1.5		.,
∕он	(Switch-type outputs)	$I_{OH} = -20 \mu A$	2.5 V	2.5 V	2.3		V
-	A port	I <sub>OL</sub> = 100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V		0.2	
	(Buffer-type output,		1.65 V	1.65 V		0.45	
,	8-mA drive)	$I_{OL} = 8 \text{ mA}$	2.5 V	2.5 V		0.55	.,
√ <sub>OL</sub>	A port	I <sub>OL</sub> = 100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V		0.2	V
	(Buffer-type output,	1 - 4 0	1.65 V	1.65 V		0.45	
	4-mA drive)	$I_{OL} = 4 \text{ mA}$	2.5 V	2.5 V		0.55	
	A port	$I_{OL} = 220 \mu A, V_{IN} = 0.15 V$	1.65 V	1.65 V		0.45	
V <sub>OL</sub>	(Switch-type outputs)	$I_{OL} = 300 \ \mu A, \ V_{IN} = 0.15 \ V$	2.5 V	2.5 V		0.55	V
	B port (Buffer-type output,	I <sub>OH</sub> = -100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V	V <sub>CC0</sub> - 0.2		
_			1.65 V	1.65 V	1.2		
	8-mA drive)	$I_{OH} = -8 \text{ mA}$	2.5 V	2.5 V	1.97		
	B port	I <sub>OH</sub> = -100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V	V <sub>CC0</sub> - 0.2		
	(Buffer-type output, 4-mA drive)		1.65 V	1.65 V	1.2		
/ <sub>OH</sub>		$I_{OH} = -4 \text{ mA}$	2.5 V	2.5 V	1.97		V
OII	B port	I <sub>OH</sub> = -100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{CC0} - 0.2$		
	(Buffer-type output,	I <sub>OH</sub> = -2 mA	1.65 V	1.65 V	1.2		
	2-mA drive)		2.5 V	2.5 V	1.97		
	B port		1.65 V	1.65 V	1.5		
	(Switch-type outputs)	$I_{OH} = -20 \mu A$	2.5 V	2.5 V	2.3		
	B port	I <sub>OL</sub> = 100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V		0.2	
	(Buffer-type output,	1 0 00	1.65 V	1.65 V		0.45	
	8-mA drive)	$I_{OL} = 8 \text{ mA}$	2.5 V	2.5 V		0.55	
	B port	I <sub>OL</sub> = 100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V		0.2	:
	(Buffer-type output,	1 4 50	1.65 V	1.65 V		0.45	
/ <sub>OL</sub>	4-mA drive)	$I_{OL} = 4 \text{ mA}$	2.5 V	2.5 V		0.55	V
OL.	B port	I <sub>OL</sub> = 100 μA	1.1 V to 3.6 V	1.1 V to 3.6 V		0.2	!
	(Buffer-type output,	1 2 m 4	1.65 V	1.65 V		0.45	
	2-mA drive)	$I_{OL} = 2 \text{ mA}$	2.5 V	2.5 V		0.55	
	B port	$I_{OL} = 220 \mu A, V_{IN} = 0.15 V$	1.65 V	1.65 V		0.45	
	(Switch-type outputs)	$I_{OL} = 300 \mu A, V_{IN} = 0.15 V$	2.5 V	2.5 V		0.55	<u> </u>
l		V <sub>I</sub> = V <sub>CCA</sub> or GND	1.1 V to 3.6 V	1.1 V to 3.6 V		±1	μA
		Switch-type I/O are open and all	1.1 V to 3.6 V	1.1 V to 3.6 V		15	
CCA		other inputs are biased at either	3.6 V	0 V		14	μΑ
CCA		V <sub>CC</sub> or GND	0 V	3.6 V			

<sup>(1)</sup> All typical values are at  $T_A = 25$ °C.



over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN TYP <sup>(1)</sup> MAX	UNIT
		Switch-type I/O are open and all	1.1 V to 3.6 V	1.1 V to 3.6 V	15	
$I_{CCB}$		other inputs are biased at either	3.6 V	0 V	-12	μΑ
	14					
I <sub>CCA</sub> +	- I <sub>CCB</sub>	$V_I = V_{CCI}$ or GND, $I_O = 0$	1.1 V to 3.6 V	1.1 V to 3.6 V	30	μΑ
C <sub>io</sub>	Auto-Dir (SDIO lines)	V <sub>I</sub> = V <sub>CCI</sub>			5.5	pF
	Bi-Dir buffer	V <sub>I</sub> = V <sub>CCX</sub> or GND			4.5	
_	AUD_DIR / OE	$V_I = V_{CCA}$ or GND			4	"F
Ci	Buffer	$V_I = V_{CCX}$ or GND			4	pF
	2-mA buffer	$V_I = V_{CCX}$ or GND			5	
Co	4-mA buffer	$V_I = V_{CCX}$ or GND			5	pF
	8-mA buffer	$V_I = V_{CCX}$ or GND			6	

# **OUTPUT DRIVE STRENGTH**

2 mA	4 mA	8 mA
WLAN_EN(B)	AUDIO_OUT(A)	SDIO_CLK(B)
SLOW_CLK(B)	WLAN_IRQ(A)	BT_UART_TX(A)
BT_EN(B)	CLK_REQ(A)	BT_UART_RX(B)
	AUDIO_IN(B)	
	AUDIO_CLK(A)	
	BT_UART CTS(B)	
	BT_UART RTS(A)	
	AUDIO_F-SYNC(A)	

Product Folder Link(s): TWL1200



# TIMING REQUIREMENTS

 $V_{CCA} = 2.5 V \pm 0.2 V$ 

over recommended operating free-air temperature range (unless otherwise noted)

		, <del>g</del>		V <sub>CCB</sub> = 1.8 V ± 0.15 V	UNIT
				MIN MAX	
	Data rate	CDIO CMD	Push-pull driving	60	Mbps
		SDIO_CMD Open-drain driving		1	Mbps
		SDIO_CLK	SDIO_CLK		MHz
		SDIO_DATAx	Push-pull driving	60	Mbps
		SDIO_CMD	Push-pull driving	17	ns
	t <sub>W</sub> Pulse duration	SDIO_CIVID	Open-drain driving	1	μs
ιW		SDIO_CLK	Push-pull driving	10	ns
		SDIO_DATAx	Fusii-puii driving	17	ns

# **TIMING REQUIREMENTS**

 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 

over recommended operating free-air temperature range (unless otherwise noted)

			,	V <sub>CCB</sub> = 1.8 V ± 0.15 V	UNIT
				MIN MA	Х
		SDIO_CMD	Push-pull driving	(	0 Mbps
	Data rate	SDIO_CIVID	Open-drain driving		Mbps 1
		SDIO_CLK	Duck pull driving	Ę	0 MHz
		SDIO_DATAx	Push-pull driving	(	0 Mbps
		SDIO CMD	Push-pull driving	17	ns
	Pulse duration	SDIO_CIVID	Open-drain driving	1	μs
ıW	t <sub>W</sub> Pulse duration	SDIO_CLK	Duck pull driving	10	ns
		SDIO_DATAx	Push-pull driving	17	ns



# SWITCHING CHARACTERISTICS $V_{CCA} = 2.5 V \pm 0.2 V$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CCB</sub> = ± 0.1		UNIT	
	(1141 01)	Push-pull driving		MIN	MAX		
			Push-pull driving		7		
	SDIO_CMD(A)	SDIO_CMD(B)	Open-drain driving (H-to-L)	1.1	7		
			Open-drain driving (L-to-H)	30	510		
			Push-pull driving		7		
	SDIO_CMD(B)	SDIO_CMD(A)	Open-drain driving (H-to-L)	1	7.5		
•			Open-drain driving (L-to-H)	30	515	no	
t <sub>pd</sub>	SDIO_CLK(A)	SDIO_CLK(B)	Push-pull driving	1	6.5	ns	
	SDIO_DATAx(A)	SDIO_DATAx(B)	Duck hull driving	1	7		
	SDIO_DATAx(B)	SDIO_DATAx(A)	Push-pull driving	1	7		
	Buffered input	2-mA drive strength output	Push-pull driving	1	7.6		
	Buffered input	4-mA drive strength output	Push-pull driving	1	7		
	Buffered input	8-mA drive strength output	Push-pull driving	1	6.5		
		2-mA drive strength output	Push-pull driving		16		
	05	4-mA drive strength output	Push-pull driving		19	ns	
t <sub>en</sub>	OE	8-mA drive strength output	Push-pull driving		18		
		Switch-type output	Push-pull driving		1	μs	
		2-mA drive strength output	Push-pull driving		17		
	0.5	4-mA drive strength output	Push-pull driving		16.5	ns	
t <sub>dis</sub>	OE	8-mA drive strength output	Push-pull driving		16	•	
		Switch-type outputs	Push-pull driving		1	μs	
			Push-pull driving	1	5		
t <sub>rA</sub>	SDIO_0	CMD(A) rise time	Open-drain driving	15	420	ns	
	SDIO_D	ATAx(A) rise time	Push-pull driving	1	4.7	•	
		• •	Push-pull driving	1	9.7		
	SDIO_0	CMD(B) rise time	Open-drain driving	15	420	•	
t <sub>rB</sub>	SDIO	CLK(B) rise time		0.5	6	+ 1	
		ATAx(B) rise time	Push-pull driving	1	9.7		
			Push-pull driving	0.7	8.3		
t <sub>fA</sub>	SDIO_	CMD(A) fall time	Open-drain driving	1.6		ns	
1/4	SDIO D	DATAx(A) fall time	Push-pull driving		1.1 7 30 510 7 1 7.5 30 515 1 6.5 1 7 1 7.6 1 7 1 6.5 1 6.5 1 7 1 6.5 16 17 1 6.5 16 17 1 7 1 6.5 16 17 1 7 1 6.5 16 17 1 7 1 6.5 16 17 1 7 1 7 1 7 1 7 1 7 1 7 1 7 1 7 1 7		
			Push-pull driving				
	SDIO_	CMD(B) fall time	Open-drain driving	1.6		-	
t <sub>fB</sub>	SDIO	CLK(B) fall time				ns	
		DATAx(B) fall time	Push-pull driving		-		
		h-A to Ch-B skew	Push-pull driving				
t <sub>sk(O)</sub>		h-B to Ch-A skew	Push-pull driving			ns	
-5k(O)		annel-to-clock skew	Push-pull driving				
			Push-pull driving	+			
	S	SDIO_CMD	Open-drain driving	+		Mbps	
Max data rate		SDIO_CLK	opon diam diving	_		MHz	
		DIO_DATAx	Push-pull driving			Mbp	

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# SWITCHING CHARACTERISTICS $V_{\text{CCA}} = 3.3 \ V \pm 0.3 \ V$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	TEST CONDITIONS	V <sub>CCB</sub> = ± 0.1	1.8 V 5 V	UNIT
	(INFOT)	(001701)		MIN	MAX	
			Push-pull driving		7	
	SDIO_CMD(A)	SDIO_CMD(B)	Open-drain driving (H-to-L)	1.1	7	İ
	ARAMETER	Open-drain driving (L-to-H) 30		510		
			Push-pull driving		7	İ
	SDIO_CMD(B) SDIO_CMD(A)		Open-drain driving (H-to-L)	1	7.5	
			Open-drain driving (L-to-H)	30	515	
<sup>L</sup> pd	SDIO_CLK(A)	SDIO_CLK(B)	Push-pull driving	1	6.5	ns
	SDIO_DATAx(A)	SDIO_DATAx(B)	Duck hull driving	1	7	İ
	SDIO_DATAx(B)	SDIO_DATAx(A)	Push-pull driving	1	7	İ
	Buffered input	2-mA drive strength output	Push-pull driving	1	7.6	ĺ
	Buffered input	4-mA drive strength output	Push-pull driving	1	7	ĺ
	Buffered -nput	8-mA drive strength output	Push-pull driving	1	6.5	ĺ
		2-mA drive strength output	Push-pull driving		16	
	05	4-mA drive strength output	Push-pull driving		19	ns
t <sub>en</sub>	OE	8-mA drive strength output	Push-pull driving		19	ĺ
		Switch-type output	Push-pull driving		1	μs
		2-mA drive strength output	Push-pull driving		17	
	05	4-mA drive strength output	Push-pull driving		16	ns
t <sub>dis</sub>	ÜE	8-mA drive strength output	Push-pull driving		16	ĺ
		Switch-type output	Push-pull driving		1	μs
	2010	2142(4)	Push-pull driving	1	4.25	
t <sub>rA</sub>	SDIO_0	CMD(A) rise time	Open-drain driving	15	420	ns
	SDIO_D	ATAx(A) rise time	Push-pull driving	1	4.25	ĺ
	0010	OMP(D) size (izaz	Push-pull driving	1	9.5	
	2DIO_0	CMD(B) rise time	Open-drain driving	15	420	ĺ
t <sub>rB</sub>	SDIO_	CLK(B) rise time	D 1 11 11 11	0.5	5.9	ns
	SDIO_D	ATAx(B) rise time	Push-pull driving	1	9.6	ĺ
	0010		Push-pull driving	0.7	8.2	
t <sub>fA</sub>	2010_	CMD(A) fall time	Open-drain driving	1.6	15 420 1 4.25 1 9.5 15 420 0.5 5.9 1 9.6 0.7 8.2	
	SDIO_D	OATAx(A) fall time	Push-pull driving	1	7 1.1 7 30 510 7 1 7.5 30 515 1 6.5 1 7 1 7.6 1 7 1 6.5 1 6.5 1 7 1 6.5 1 6.5 1 7 1 4.25 1 1 4.25 1 420 0.5 5.9 1 9.6 0.7 8.2 1.6 8.2	ĺ
	0010		Push-pull driving	1	9.2	
	SDIO_	CMD(B) fall time	Open-drain driving	1.6	10.8	ĺ
t <sub>fB</sub>	SDIO_	CLK(B) fall time	D 1 11 11 11	0.5	5.2	ns
	SDIO_D	ATAx(B) fall time	Pusn-pull driving	1	9.8	ĺ
	SDIO C	h-A to Ch-B skew	Push-pull driving		0.4	
t <sub>sk(O)</sub>	SDIO C	h-B to Ch-A skew	Push-pull driving		0.4	ns
` ,	SDIO Cha	annel-to-Clock skew	Push-pull driving		1.3	
		ADIO OMB	Push-pull driving		60	
	S	SDIO_CMD	Open-drain driving		1	Mbps
Max data rate	(	SDIO_CLK			50	MHz
		DIO_DATAx	Push-pull driving			Mbps



# **OPERATING CHARACTERISTICS**

 $T_{\rm A} = 25^{\circ}{\rm C}$ 

	PARAMETE	R	TEST CONDITIONS	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	UNIT	
Enabled		C <sub>pd</sub> input side		18.3	20.3		
DATAy and CMD	Enabled	C <sub>pd</sub> output side	$C_L = 0,$ f = 10 MHz,	18.25	19.52		
DATAx and CMD	Disabled	C <sub>pd</sub> input side	$t_r = t_0 \text{ MHZ},$ $t_r = t_f = 1 \text{ ns}$	0.8	0.8	pF	
	Disabled	C <sub>pd</sub> output side		0.1	0.1		
	Enabled	C <sub>pd</sub> input side		0.6	0.9		
Clock	Enabled	C <sub>pd</sub> output side	$C_L = 0$ ,	8.8	10.1	~F	
Clock	Disabled	C <sub>pd</sub> input side	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	pF	
	Disabled	C <sub>pd</sub> output side		0.1	0.1		
	Enabled	C <sub>pd</sub> input side		0.6	1.0	pF	
		C <sub>pd</sub> output side	$C_L = 0$ ,	7.1	7.9		
2-mA buffer	Disabled	C <sub>pd</sub> input side	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1		
	Disabled	C <sub>pd</sub> output side		0.1	0.1		
	Enabled	C <sub>pd</sub> input side		0.6	1.0	pF	
A A b W - n		C <sub>pd</sub> output side	$C_L = 0$ ,	7.6	8.6		
4-mA buffer	Dischile d	C <sub>pd</sub> input side	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1		
	Disabled	C <sub>pd</sub> output side	1 1 -	0.1	0.1		
	Cashiad	C <sub>pd</sub> input side		0.6	1.0		
0 1 4	Enabled	C <sub>pd</sub> output side	$C_L = 0$ ,	8.8	10.1		
8-mA buffer	Dischile d	C <sub>pd</sub> input side	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	pF	
	Disabled	C <sub>pd</sub> output side	' '	0.1	0.1		
	E a a la la al	C <sub>pd</sub> input side		0.6	0.95		
4 4 1/0	Enabled	C <sub>pd</sub> output side	$C_L = 0$ ,	8.2	9.1	pF	
4-mA I/O	Disabled	C <sub>pd</sub> input side	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1		
	Disabled	C <sub>pd</sub> output side	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0.1	0.1	1	

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#### TYPICAL CHARACTERISTICS

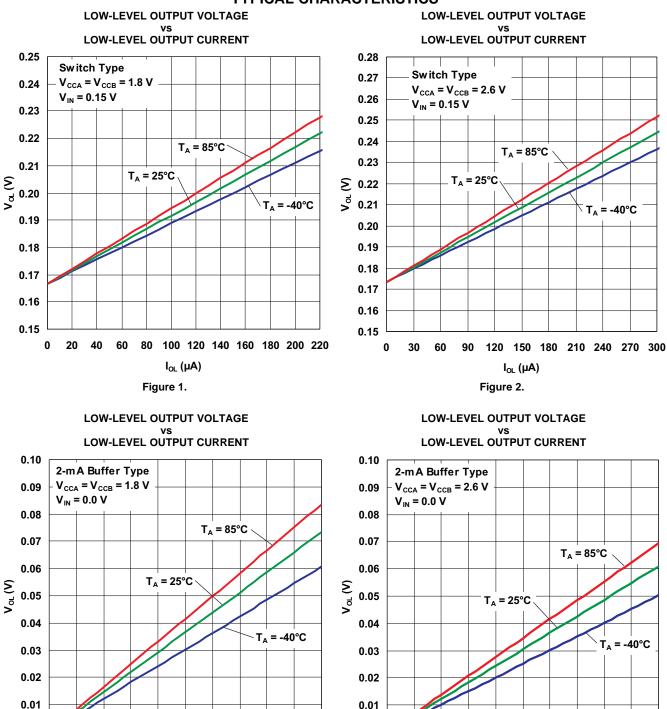


Figure 3.

0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0

 $I_{OL}(mA)$ 

Figure 4.

 $I_{OL}(mA)$ 

0.8 1.0 1.2 1.4 1.6 1.8

2.0

0.00

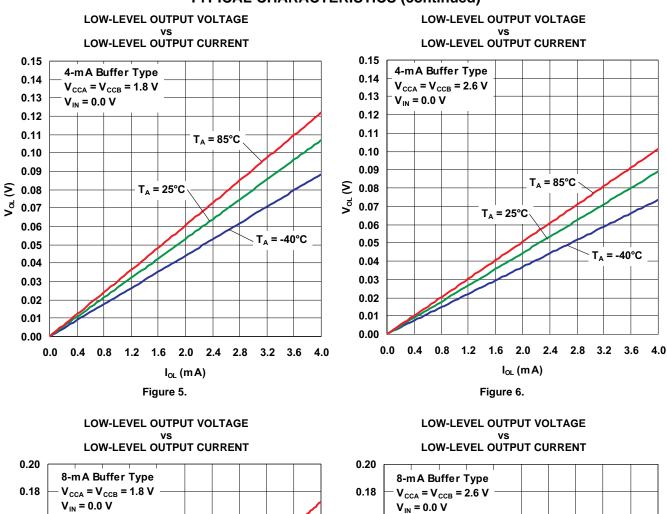
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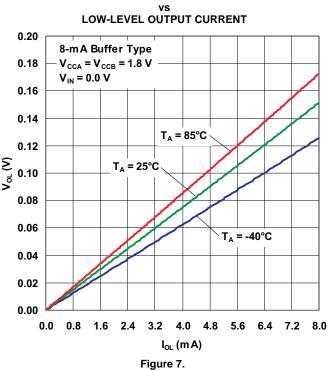
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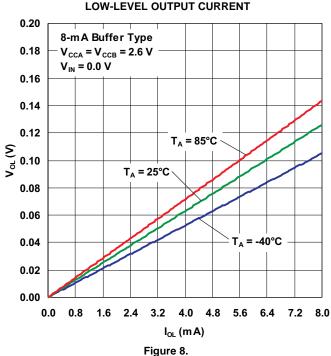
0.2 0.4

0.6











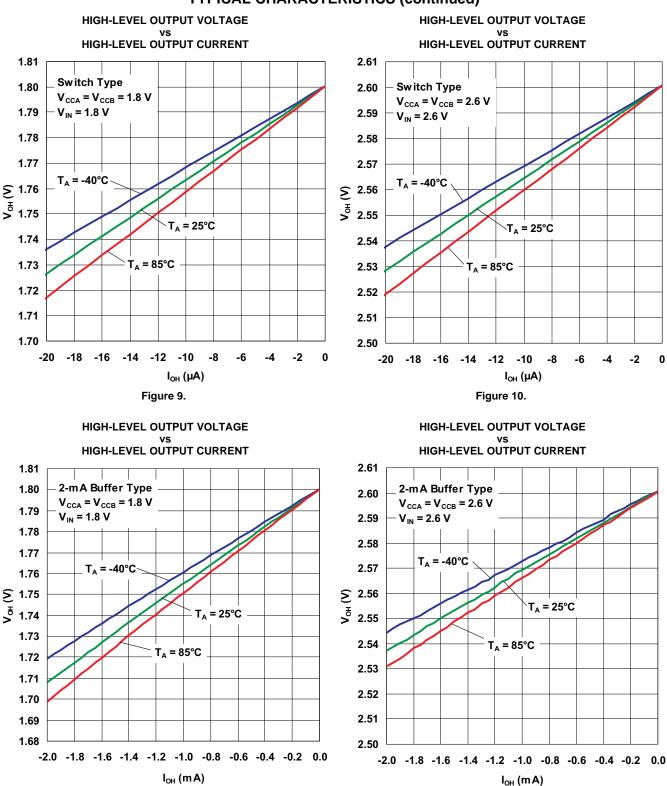
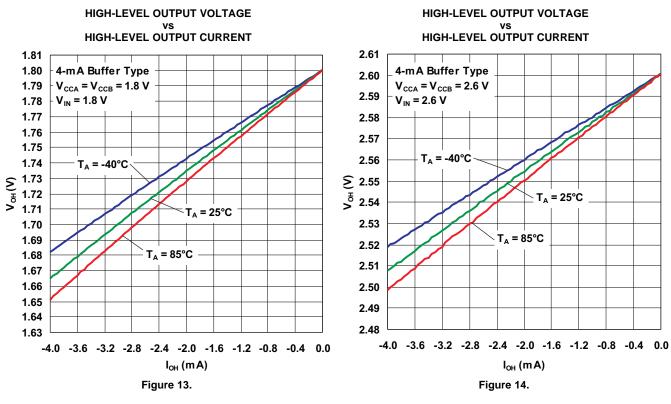


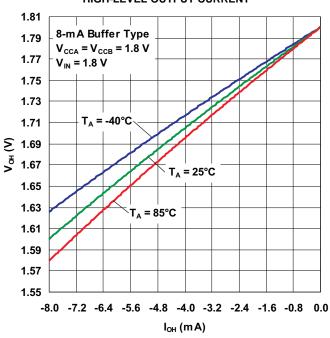
Figure 11.

Figure 12.





# HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT



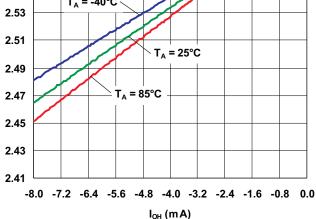
 $\begin{array}{c|c}
 & V_{IN} = 2.6 \text{ V} \\
\hline
2.55 & & & \\
\hline
2.53 & & & \\
\hline
& & \\
& & \\
\hline
& & \\
& & \\
\hline
& & \\
& & \\
\hline
& & \\
& & \\
\hline
& & \\
& & \\
\hline
& & \\
& & \\
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& & \\
\end{array}$   $\begin{array}{c|c}
 & & \\
\hline
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\end{array}$   $\begin{array}{c|c}
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& & \\
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& & \\
\hline
& & \\
\end{array}$   $\begin{array}{c|c}
 & & \\
\hline
& & \\
\hline
& & \\
\hline
& & \\
\hline
& & \\
\end{array}$ 

8-mA Buffer Type

 $V_{CCA} = V_{CCB} = 2.6 V$ 

2.61

2.59



**HIGH-LEVEL OUTPUT VOLTAGE** 

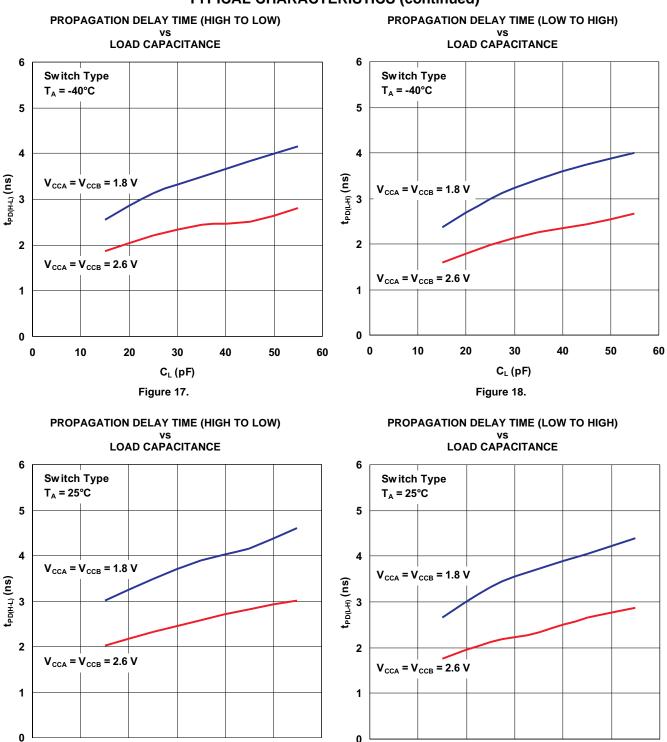
**HIGH-LEVEL OUTPUT CURRENT** 

Figure 15.

Figure 16.

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20

30

C<sub>L</sub> (pF)

Figure 19.

40

50

40

50

60

0

10

60

0

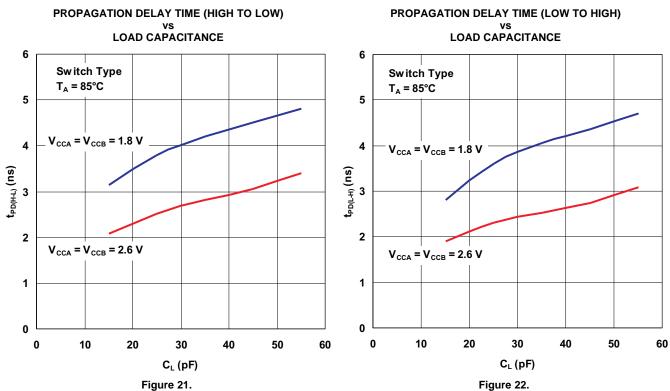
10

20

30

C<sub>L</sub> (pF) Figure 20.







# Typical Application Wiring for TWL1200 When Connecting to the WL1271

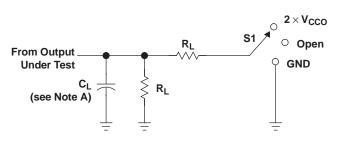
## Table 2. WL1271+TWL1200 Interface

HOST (MSM)	PIN NAME	BALL NO.	TYPE		TYPE	BALL NO.	PIN NAME	WL1271 COB
	VCCA	C4	Power (3.0 V)		Power (1.8 V)	C5	VCCB	
	VCCA	D4	Power (3.0 V)		Power (1.8 V)	D5	VCCB	
	SDIO_DATA0(A)	B2	I/O ↔		1/0 ↔	В6	SDIO_DATA0(B)	K4
	SDIO_DATA1(A)	C2	I/O ↔		1/0 ↔	C6	SDIO_DATA1(B)	J4
	SDIO_DATA2(A)	C1	I/O ↔		1/0 ↔	C7	SDIO_DATA2(B)	J3
	SDIO_DATA3(A)	B1	I/O ↔		1/0 ↔	В7	SDIO_DATA3(B)	J5
	SDIO_CMD(A)	A2	1/0 ↔		1/0 ↔	A6	SDIO_CMD(B)	L3
	SDIO_CLK(A)	A1	l →		O →	A7	SDIO_CLK(B)	М3
	WLAN_EN(A)	D1	l →		O →	D6	WLAN_EN(B)	J2
	WLAN_IRQ(A)	D2	0 ←		I ←	D7	WLAN_IRQ(B)	G4
	CLK_REQ(A)	E1	0 ←		I ←	E7	CLK_REQ(B)	F5
	BT_EN(A)	E2	l →		O →	E6	BT_EN(B)	G5
	BT_UART_RX(A)	G1	l →	TWL1200	O →	G7	BT_UART_RX(B)	G7
	BT_UART_CTS(A)	F1	l →		O →	F7	BT_UART_CTS(B)	E11
	BT_UART_TX(A)	G2	0 ←		I ←	G6	BT_UART_TX(B)	G8
	BT_UART_RTS(A)	F2	0 ←		I ←	F6	BT_UART_RTS(B)	G11
	AUDIO_IN(A)	F3	I →		1/0 ↔	F5	AUDIO_IN(B)	F6
	AUDIO_CLK(A)	А3	1/0 ↔		1/0 ↔	A5	AUDIO_CLK(B)	F8
	AUDIO_F-SYN(A)	В3	I/O ↔		1/0 ↔	B5	AUDIO_F-SYN(B)	H11
	AUDIO_OUT(A)	G3	0 ←		I ←	G5	AUDIO_OUT(B)	F7
	SLOW_CLK(A)	G4	I →		O →	F4	SLOW_CLK(B)	K9
	AUD_DIR	A4	I →		GND	D3	GND	
	ŌĒ	B4	active low			E3	GND	
						E4	GND	
						E5	GND	

 $V_{\text{CCA}}$ 



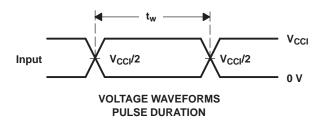
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>pd</sub> t <sub>PLZ</sub> /t <sub>PZL</sub> t <sub>PHZ</sub> /t <sub>PZH</sub>	Open 2 × V <sub>CCO</sub> GND

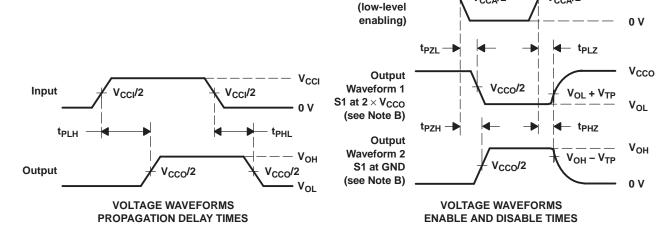
# LOAD CIRCUIT FOR BUFFER-TYPE OUTPUTS

V <sub>CCO</sub>	CL	R <sub>L</sub>	V <sub>TP</sub>
1.8 V $\pm$ 0.15 V	15 pF	<b>2 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	<b>2 k</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	<b>2 k</b> Ω	0.3 V



V<sub>CCA</sub>/2

V<sub>CCA</sub>/2



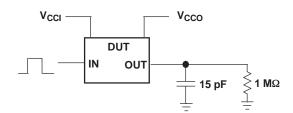
Output Control

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $dv/dt \geq 1 V/ns$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{Pl,7}$  and  $t_{PH7}$  are the same as  $t_{dis}$ .
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H.  $V_{CCI}$  is the  $\overline{V_{CC}}$  associated with the input port.
  - I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

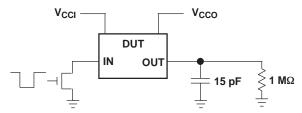
Figure 23. Push-Pull Buffered Direction Control Load Circuit and Voltage Waveform



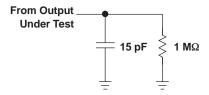
#### PARAMETER MEASUREMENT INFORMATION (continued)



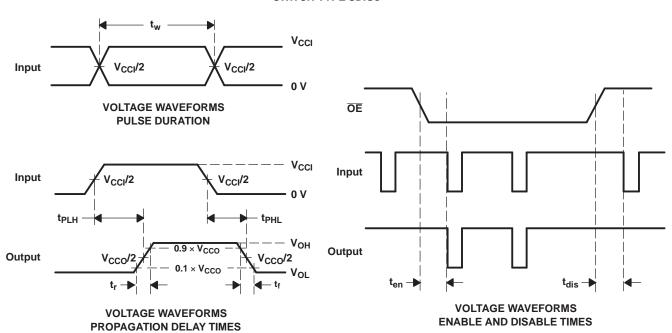
DATA RATE, PULSE DURATION, PROPAGATION DELAY,
OUTPUT RISE AND FALL TIME MEASUREMENT USING
A PUSH-PULL DRIVER



DATA RATE, PULSE DURATION, PROPAGATION DELAY,
OUTPUT RISE AND FALL TIME MEASUREMENT USING
AN OPEN-DRAIN DRIVER



#### LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT – SWITCH-TYPE SDIOs



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $dv/dt \geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
- I. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 24. Auto-Direction Control Load Circuit and Voltage Waveform

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#### **APPLICATION CIRCUIT EXAMPLES**

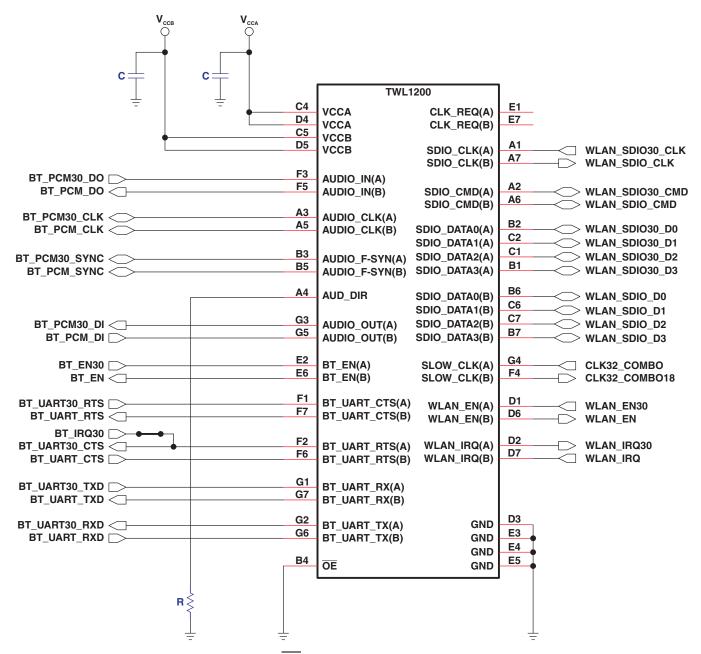


Figure 25. Application Circuit Example, OE Connection With Audio\_CLK and Audio\_F-SYNC Channels Established From B Side to A Side



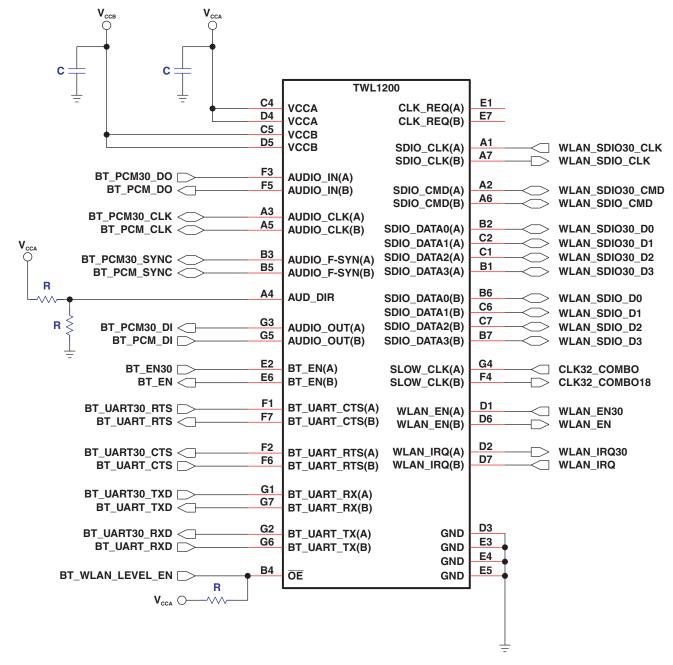


Figure 26. Application Circuit Example, With Voltage Divider for AUD\_DIR Connection



#### PRINCIPLES OF OPERATION

#### **Applications**

The TWL1200 device has been designed to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels between a host processor and the Texas Instruments Wi-Link-6 WLAN/BT/FM products. It is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

#### **Architecture**

The BT/UART and PCM/Audio subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength.

The SDIO lines comprise a semi-buffered auto-direction-sensing based translator architecture (see Figure 27) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

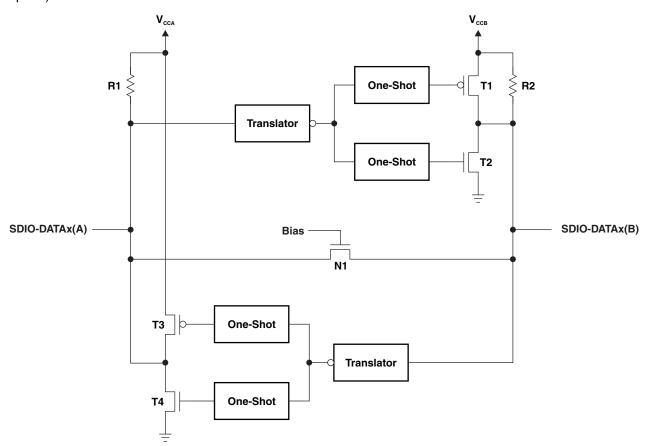


Figure 27. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the "switch-type" voltage translation function:

- 1. Integrated pullup resistors to provide dc-bias and drive capabilities
- 2. An N-channel pass-gate transistor topology (with a high R<sub>ON</sub> of ~300 Ω) that ties the A-port to the B-port
- 3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports



For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The  $V_{GATE}$  gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high signal rising-edge, the O.S. circuits turn on the PMOS transistors ( $T_1$ ,  $T_3$ ) and its associated driver output resistance of the driver is decreased to approximately 50  $\Omega$  to 70  $\Omega$  during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors ( $T_2$ ,  $T_4$ ) and its associated driver output resistance of the driver is decreased to approximately 50  $\Omega$  to 70  $\Omega$  during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic  $I_{CC}$  and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both High or both Low) for the one-shot to trigger again. In a DC state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the "smart pullup resistors" that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R<sub>PU1</sub> and R<sub>PU2</sub> values are 25 kΩ when the output is driving a low
- R<sub>PU1</sub> and R<sub>PU2</sub> values are 4 kΩ when the output is driving a high
- $R_{PU1}$  and  $R_{PU2}$  values are 70 k $\Omega$  when the device is disabled via the  $\overline{OE}$  pin or by pulling the either  $V_{CCA}$  or  $V_{CCB}$  to 0 V.

The reason for using these "smart" pullup resistors is to allow the TWL1200 to realize a lower static power consumption (when the I/Os are low), support lower  $V_{OL}$  values for the same size pass-gate transistor, and improved simultaneous switching performance.

#### **Input Driver Requirements**

The continuous dc-current "sinking" capability is determined by the external system-level driver interfaced to the SDIO pins. Since the high bandwidth of these bidirectional SDIO circuits necessitates the need for a port to quickly change from an input to an output (and vice-vera), they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the smart pullup resistor values.

The fall time  $(t_{fA}, t_{fB})$  of a signal depends on the edge rate and output impedance of the external device driving the SDIO I/Os, as well as the capacitive loading on these lines.

Similarly, the  $t_{pd}$  and max data rates also depend on the output impedance of the external driver. The values for  $t_{fA}$ ,  $t_{fB}$ ,  $t_{pd}$ , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50  $\Omega$ .

# **Output Load Considerations**

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic  $I_{\rm CC}$ , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TWL1200 SDIO output sees, so it is recommended that this lumped-load capacitance be considered and kept below 75 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Product Folder Link(s): TWL1200



# **Package Dimensions**

The dimensions for the YFF package are shown in Table 3. See the package drawing at the end of this data sheet.

**Table 3. YFF Package Dimensions** 

Packaged Device	D	E
TWL1200YFFR	2.76 ± 0.03 mm	2.76 ± 0.03 mm

Product Folder Link(s): TWL1200



21-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TWL1200YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Add to cart
TWL1200ZQCR	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Add to cart

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
		Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TWL1200YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
TWL1200ZQCR	BGA MI CROSTA R JUNI OR	ZQC	48	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1

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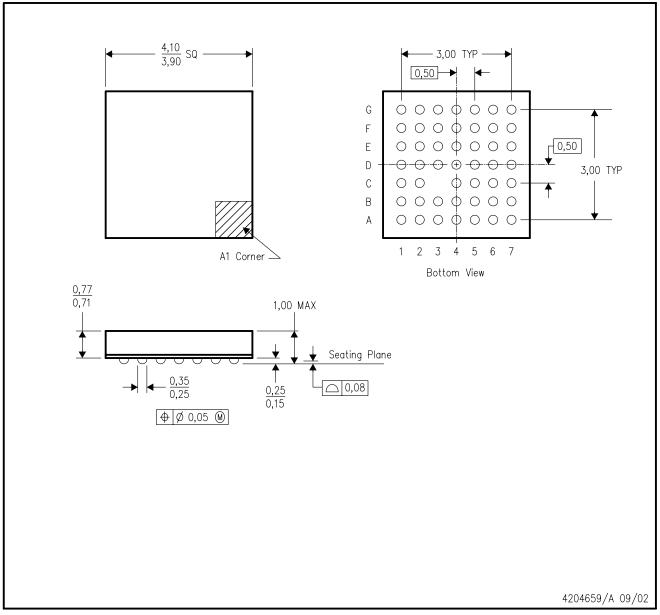


#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TWL1200YFFR	DSBGA	YFF	49	3000	210.0	185.0	35.0	
TWL1200ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	340.5	338.1	20.6	

# ZQC (S-PBGA-N48)

# PLASTIC BALL GRID ARRAY



NOTES:

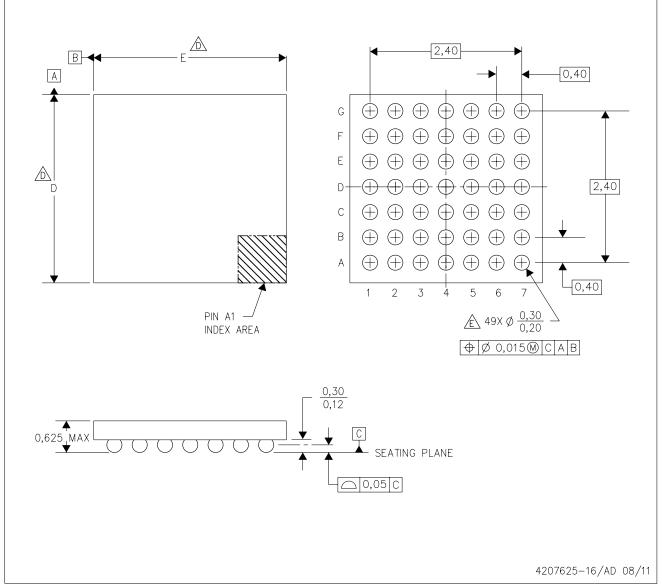
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ BGA configuration
- D. Falls within JEDEC MO-225
- E. This package is lead-free.

MicroStar Junior is a trademark of Texas Instruments.



YFF (R-XBGA-N49)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  - E. Reference Product Data Sheet for array population. 7 x 7 matrix pattern is shown for illustration only.
  - F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments



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