





# Precision, Gain of 0.2 Level Translation DIFFERENCE AMPLIFIER

## **FEATURES**

- GAIN OF 0.2 TO INTERFACE ±10V SIGNALS TO SINGLE-SUPPLY ADCs
- GAIN ACCURACY: ±0.024% (max)
- WIDE BANDWIDTH: 1.5MHz
- HIGH SLEW RATE: 15V/µs
- LOW OFFSET VOLTAGE: ±100µV
- LOW OFFSET DRIFT:  $\pm 1.5 \mu V/^{\circ}C$
- SINGLE-SUPPLY OPERATION DOWN TO 1.8V

## **APPLICATIONS**

- INDUSTRIAL PROCESS CONTROLS
- INSTRUMENTATION
- DIFFERENTIAL TO SINGLE-ENDED CONVERSION
- AUDIO LINE RECEIVERS

# DESCRIPTION

The INA159 is a high slew rate, G = 1/5 difference amplifier consisting of a precision op amp with a precision resistor network. The gain of 1/5 makes the INA159 useful to couple  $\pm$ 10V signals to single-supply analog-to-digital converters (ADCs), particularly those operating on a single +5V supply. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. Excellent temperature coefficient of resistance (TCR) tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on a total of +1.8V to +5.5V single or split supplies. The INA159 reference input uses two resistors for easy mid-supply or reference biasing.

The difference amplifier is the foundation of many commonly-used circuits. The INA159 provides this circuit function without using an expensive external precision resistor network. The INA159 is available in an MSOP-8 surface-mount package and is specified for operation over the extended industrial temperature range,  $-40^{\circ}$ C to  $+125^{\circ}$ C.

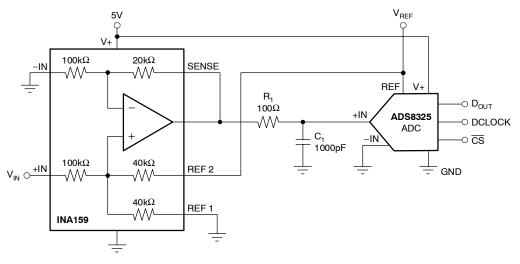


Figure 1. Typical Application

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#### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage+5.5V
Signal Input Terminals (–IN and +IN), Voltage $\ldots \ldots \pm 30V$
Reference (REF 1 and REF2) and Sense Pins
Current
Voltage
Output Short Circuit Continuous
Operating Temperature40°C to +150°C
Storage Temperature65°C to +150°C
Junction Temperature
ESD Rating
Human Body Model 4000V
Charged Device Model 1000V

<sup>(1)</sup> Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

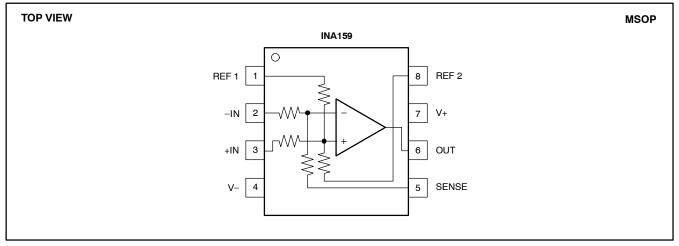
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### **ORDERING INFORMATION(1)**

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA159	MSOP-8	DGK	CJB

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

### **PIN CONFIGURATIONS**



## ELECTRICAL CHARACTERISTICS: V<sub>S</sub> = +5V

Boldface limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ .

At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{REF} = 5V$ , unless otherwise noted.

			INA1		IA159		
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE <sup>(1)</sup>		RTO					
Initial <sup>(1)</sup>	Vos	$V_{S} = \pm 2.5 V$ , Reference and Input Pins Grounded		±100	±500	μV	
vs Temperature				±1.5		μ <b>V</b> /° <b>C</b>	
vs Power Supply	PSRR	$V_{S} = \pm 0.9V$ to $\pm 2.75V$		±20	±100	μV/V	
Reference Divider Accuracy	/ <sup>(2)</sup>			±0.002	±0.024	%	
over Temperature				±0.002		%	
INPUT IMPEDANCE <sup>(3)</sup>							
Differential				240		kΩ	
Common-Mode				60		kΩ	
INPUT VOLTAGE RANGE		RTI					
Common-Mode Voltage	V <sub>CM</sub>						
Range	V CM						
Positive				17.5		V	
Negative				-12.5		V	
Common-Mode Rejection	CMRR	$V_{CM}$ = -10V to +10V, $R_{S}$ = 0 $\Omega$	80	96		dB	
Ratio	OWN IT I	VCM = 10V to 110V, 115 = 022	00				
over Temperature				94		dB	
OUTPUT VOLTAGE NOISE <sup>(4)</sup>		RTO					
f = 0.1Hz to 10Hz				10		$\mu V_{PP}$	
f = 10kHz				30		nV/√Hz	
GAIN		$V_{REF2}$ = 4.096V, $R_L$ Connected to GND,					
		$(V_{IN+}) - (V_{IN-}) = -10V$ to +10V, $V_{CM} = 0V$					
Initial	G			0.2		V/V	
Error				±0.005	±0.024	%	
vs Temperature				±1		ppm/°C	
Nonlinearity				±0.0002		% of FS	
OUTPUT							
Voltage, Positive		$V_{REF2}$ = 4.096V, $R_L$ Connected to GND	(V+) – 0.1	(V+) – 0.02		V	
Voltage, Negative		$V_{REF2}$ = 4.096V, $R_L$ Connected to GND	(V–) + 0.048	(V–) + 0.01		V	
Current Limit, Continuous to Co	ommon		о <b>т</b> .	±60		mA	
Capacitive Load			See Type	cal Characteris	Stic	pF	
Open-Loop Output Impedance	Ro	$f = 1MHz, I_0 = 0$		110		Ω	
FREQUENCY RESPONSE							
Small-Signal Bandwidth		–3dB		1.5		MHz	
Slew Rate	SR			15		V/µs	
Settling Time, 0.01%	t <sub>S</sub>	4V Output Step, $C_L = 100 pF$		1		μs	
Overload Recovery Time		50% Overdrive		250		ns	
POWER SUPPLY				_			
Specified Voltage Range	Vs			+5		V	
Operating Voltage Range			+1.8		+5.5	V	
Quiescent Current	Ι <sub>Q</sub>	$I_{O}$ = 0mA, $V_{S}$ = ±2.5V, Reference and Input Pins Grounded		1.1	1.5	mA	
TEMPERATURE RANGE							
Specified Range			-40		+125	°C	
Operating Range			-40		+150	°C	
Storage Range			-65		+150	°C	
Thermal Resistance	$\theta_{\sf JA}$						
MSOP-8		Surface-Mount		150		°C/W	

<sup>(1)</sup> Includes effects of amplifier input bias and offset currents.

(2) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 2.

 $^{(3)}\,$  Internal resistors are ratio matched but have  $\pm 20\%$  absolute value.

<sup>(4)</sup> Includes effects of amplifier input current noise and thermal noise contribution of resistor network.





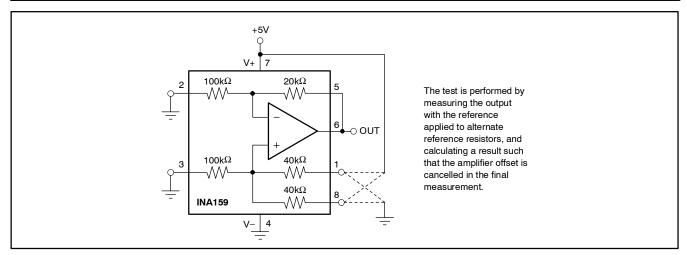
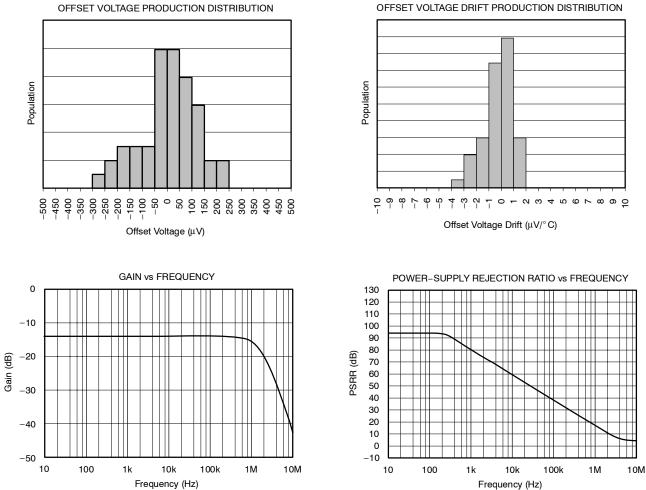


Figure 2. Test Circuit for Reference Divider Accuracy

### **TYPICAL CHARACTERISTICS**

At  $T_A = +25^{\circ}$ C,  $R_L = 10k\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{REF} = 5V$ , unless otherwise noted.

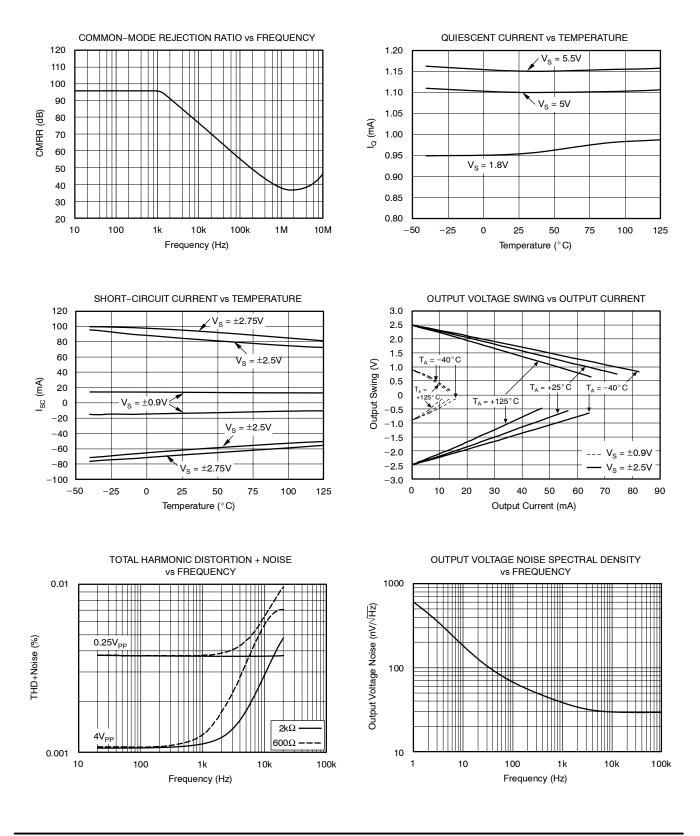


OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

## TYPICAL CHARACTERISTICS (continued)

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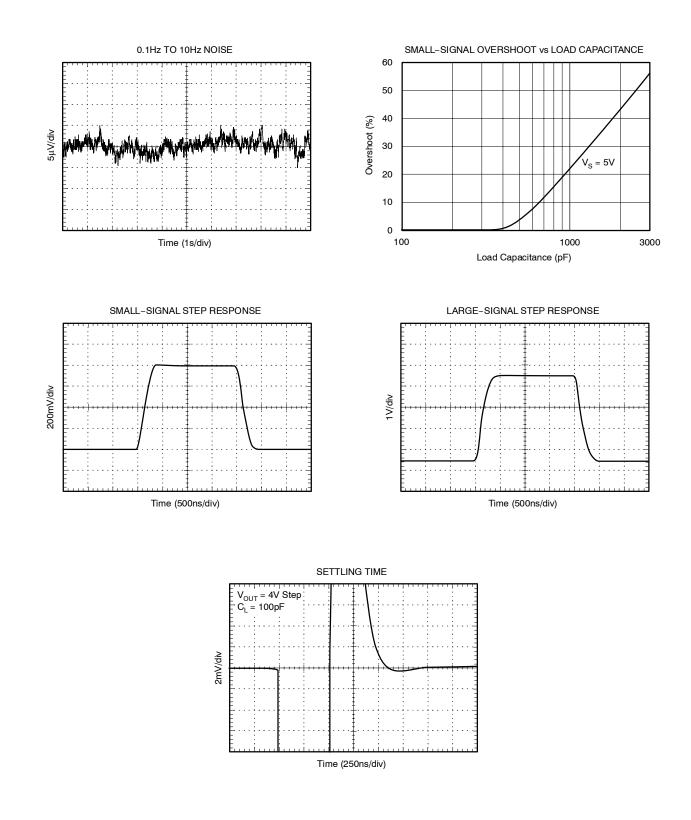
At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{REF} = 5V$ , unless otherwise noted.





### **TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{REF} = 5V$ , unless otherwise noted.





## **APPLICATION INFORMATION**

The internal op amp of the INA159 has a rail-to-rail common-mode voltage capability at its inputs. A rail-to-rail op amp allows the use of  $\pm 10V$  inputs into a circuit biased to 1/2 of a 5V reference (2.5V quiescent output). The inputs to the op amp will swing from approximately 400mV to 3.75V in this application.

The unique input topology of the INA159 eliminates the input offset transition region typical of most rail-to-rail complementary stage operational amplifiers. This allows the INA159 to provide superior glitch- and transition-free performance over the entire common-mode range.

Good layout practice includes the use of a  $0.1 \mu F$  bypass capacitor placed closely across the supply pins.

#### **COMMON-MODE RANGE**

The common-mode range of the INA159 is a function of supply voltage and reference. Where both pins, REF1 and REF2, are connected together:

$$V_{CM+} = (V+) + 5[(V+) - V_{REF}]$$
(1)

$$V_{CM-} = (V-) - 5[V_{REF} - (V-)]$$
 (2)

Where one REF pin is connected to the reference, and the other pin grounded (1/2 reference connection):

$$V_{CM+} = (V+) + 5[(V+) - (0.5V_{REF})]$$
 (3)

$$V_{CM-} = (V-) - 5[(0.5V_{REF}) - (V-)]$$
 (4)

Some typical values are shown in Table 1.

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# Table 1. Common-Mode Range For Various Supply and Reference Voltages

REF 1 and REF 2 Connected Together								
V+	V-	V <sub>REF</sub>	V <sub>CM+</sub>	V <sub>CM-</sub>				
5	0	3	15	–15				
5	0	2.5	17.5	-12.5				
5	0	1.25	23.75	-6.25				
1/2 Reference	1/2 Reference Connection							
V+	V-	V <sub>REF</sub>	V <sub>CM+</sub>	V <sub>CM-</sub>				
5	0	5	17.5	-12.5				
5	0	4.096	19.76	-10.24				
5	0	2.5	23.75	-6.25				
3.3	0	3.3	11.55	-8.25				
3.3	0	2.5	13.55	-6.25				
3.3	0	1.25	16.675	-3.125				



## Table 2. Input and Output Relationships for Various Reference and Connection Combinations

V <sub>REF</sub> (V)	REF CONNECTION	V <sub>OUT</sub> for V <sub>IN</sub> = 0 (V)	LINEAR V <sub>IN</sub> RANGE (V)	USEFUL V <sub>OUT</sub> SWING (V)
5	5V V+	2.5	+10 0 -10	4.5 (±2V swing) 0.5
4.096		2.048	+10 0 -10	4.048 (±2V swing) 0.048
3.3		1.65	+10 0 -7.885	3.65 (–1.577V, +2V swing) 0.048
2.5		1.25	+10 (also +5) 0 -6 (also -5)	3.25 (–1.2V, +2V swing) 0.048
1.8		0.9	+10 0 -4.26	2.9 (–0.852V, +2V swing) 0.048
2.5	5V V+ -IN 100kΩ 20kΩ SENSE	2.5	+10 0 -10	4.5 (±2V swing) 0.5
1.8	V <sub>IN</sub> O <sup>+IN</sup> 100kΩ 40kΩ REF 2 O V <sub>REF</sub>	1.8	+10 0 -8.76	3.8 (-1.752V, +2V swing) 0.048
1.2	$\frac{40 k\Omega}{M}$ REF 1	1.2	+10 0 -5.76	3.2 (-1.15V, +2V swing) 0.048



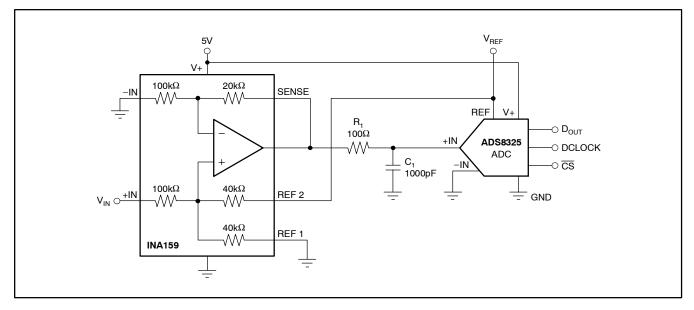


Figure 3. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs

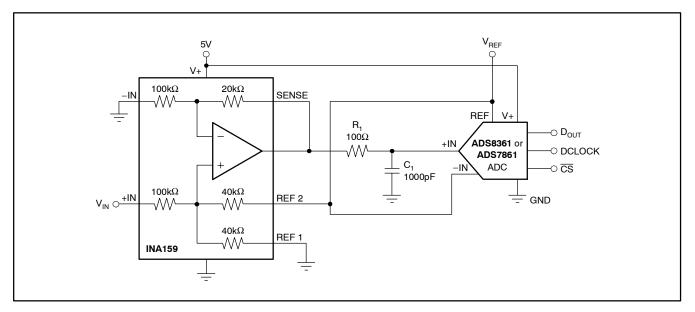
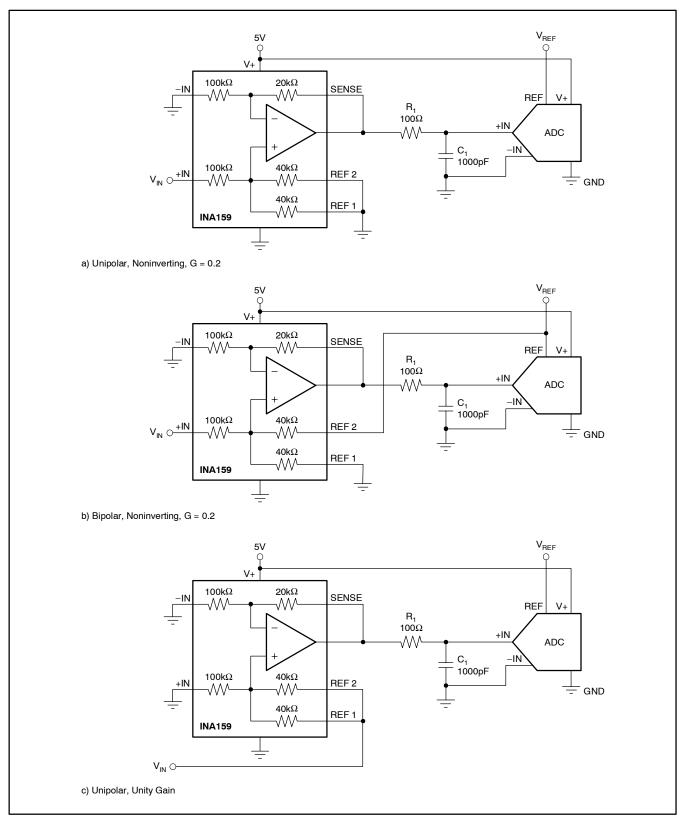


Figure 4. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs with Pseudo-Differential Inputs (such as the ADS7861 and ADS8361)









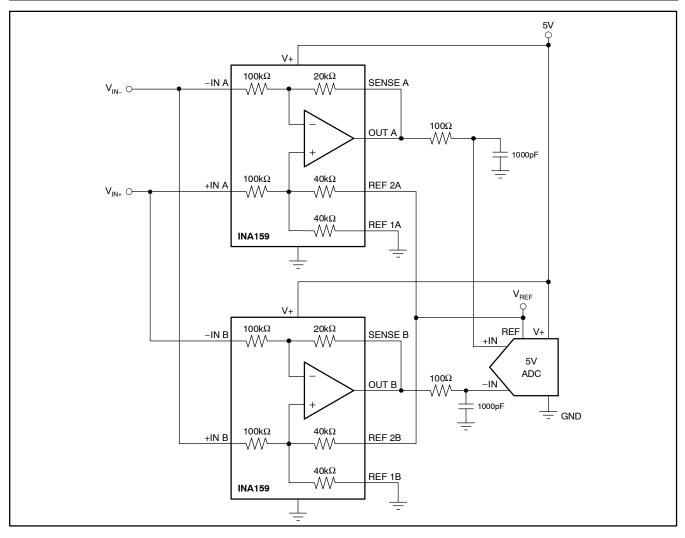


Figure 6. Differential ADC Drive

### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
INA159AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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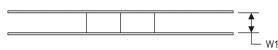
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### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

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TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA159AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA159AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

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## PACKAGE MATERIALS INFORMATION

12-Dec-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA159AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
INA159AIDGKT	MSOP	DGK	8	250	210.0	185.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



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