# The RF Sub-Micron MOSFET Line **RF Power Field Effect Transistors**N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large—signal, common—source amplifier applications in 28 volt base station equipment.

- Typical Performance at 945 MHz, 28 Volts
   Output Power 45 Watts PEP
   Power Gain 19 dB
   Efficiency 41% (Two Tones)
   IMD –31 dBc
- Integrated ESD Protection
- Guaranteed Ruggedness @ Load VSWR = 5:1, @ 28 Vdc, 945 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large—Signal Impedance Parameters
- Dual—Lead Boltdown Plastic Package Can Also Be Used As Surface Mount.
- TO-272 Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.
- TO-270 Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

## MRF9045MR1 MRF9045MBR1

945 MHz, 45 W, 28 V LATERAL N-CHANNEL BROADBAND RF POWER MOSFETs



### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	65	Vdc
Gate-Source Voltage	V <sub>GS</sub>	+15, -0.5	Vdc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	177 1.18	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Junction Temperature	TJ	175	°C

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case		0.85	°C/W

#### **ESD PROTECTION CHARACTERISTICS**

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

#### MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating	
Per JESD 22-A113	3	

 $NOTE - \underline{\textbf{CAUTION}}$  - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6



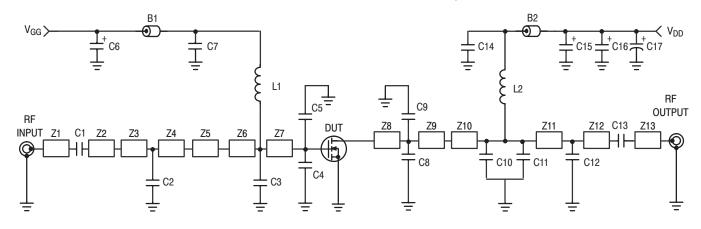


**ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	<u> </u>			-	•
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 65 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	_	10	μAdc
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	_	_	1	μAdc
Gate-Source Leakage Current (V <sub>GS</sub> = 5 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	_		1	μAdc
N CHARACTERISTICS	<u> </u>			ļ	
Gate Threshold Voltage (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 150 μAdc)	V <sub>GS(th)</sub>	2	2.8	4	Vdc
Gate Quiescent Voltage (V <sub>DS</sub> = 28 Vdc, I <sub>D</sub> = 350 mAdc)	V <sub>GS(Q)</sub>	3	3.7	5	Vdc
Drain–Source On–Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 1 Adc)	V <sub>DS(on)</sub>	_	0.22	0.4	Vdc
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 3 Adc)	9fs	_	4	_	S
YNAMIC CHARACTERISTICS				-	•
Input Capacitance ( $V_{DS}$ = 28 Vdc $\pm$ 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc)	C <sub>iss</sub>	_	70	_	pF
Output Capacitance ( $V_{DS} = 28 \text{ Vdc} \pm 30 \text{ mV(rms)ac} @ 1 \text{ MHz}, V_{GS} = 0 \text{ Vdc}$ )	C <sub>oss</sub>	_	38	_	pF
Reverse Transfer Capacitance ( $V_{DS} = 28 \text{ Vdc} \pm 30 \text{ mV(rms)ac} @ 1 \text{ MHz}, V_{GS} = 0 \text{ Vdc}$ )	C <sub>rss</sub>	_	1.7	_	pF
UNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system	m)	-			•
Two-Tone Common-Source Amplifier Power Gain (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 45 W PEP, I <sub>DQ</sub> = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G <sub>ps</sub>	17	19	_	dB
Two–Tone Drain Efficiency $(V_{DD}=28\ Vdc,\ P_{out}=45\ W\ PEP,\ I_{DQ}=350\ mA,\ f1=945.0\ MHz,\ f2=945.1\ MHz)$	η	38	41	_	%
3rd Order Intermodulation Distortion $(V_{DD} = 28 \text{ Vdc}, P_{out} = 45 \text{ W PEP}, I_{DQ} = 350 \text{ mA}, f1 = 945.0 \text{ MHz}, f2 = 945.1 \text{ MHz})$	IMD	_	-31	-28	dBc
Input Return Loss $(V_{DD} = 28 \text{ Vdc}, P_{out} = 45 \text{ W PEP}, I_{DQ} = 350 \text{ mA}, \\ f1 = 945.0 \text{ MHz}, f2 = 945.1 \text{ MHz})$	IRL	_	-14	-9	dB
Two–Tone Common–Source Amplifier Power Gain ( $V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G <sub>ps</sub>	_	19	_	dB
Two–Tone Drain Efficiency $(V_{DD} = 28 \text{ Vdc}, P_{out} = 45 \text{ W PEP}, I_{DQ} = 350 \text{ mA}, \\ f1 = 930.0 \text{ MHz}, f2 = 930.1 \text{ MHz} \text{ and } f1 = 960.0 \text{ MHz}, \\ f2 = 960.1 \text{ MHz})$	η	_	41	_	%
3rd Order Intermodulation Distortion (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 45 W PEP, I <sub>DQ</sub> = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	_	<del>-</del> 31	_	dBc
Input Return Loss (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 45 W PEP, I <sub>DQ</sub> = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	_	-13	_	dB

Z2

## Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Surface Mount	Z3	0.14" x 0.32" Microstrip
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	<b>Z</b> 4	0.47" x 0.32" Microstrip
C2, C8	2.7 pF Chip Capacitors, B Case	<b>Z</b> 5	0.16" x 0.32" x 0.62" Taper
C3	3.9 pF Chip Capacitor, B Case	Z6	0.18" x 0.62" Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	<b>Z</b> 7	0.56" x 0.62" Microstrip
C6, C15, C16	10 μF, 35 V Tantalum Surface Mount Capacitors	Z8	0.33" x 0.32" Microstrip
C10	2.2 pF Chip Capacitor, B Case	Z9	0.14" x 0.32" Microstrip
C11	4.7 pF Chip Capacitor, B Case	Z10	0.36" x 0.08" Microstrip
C12	1.2 pF Chip Capacitor, B Case	Z11	1.01" x 0.08" Microstrip
C17	220 μF, 50 V Electrolytic Capacitor	Z12	0.15" x 0.08" Microstrip
L1, L2	12.5 nH Inductors	Z13	0.29" x 0.08" Microstrip
Z1	0.20" x 0.08" Microstrip		

0.57" x 0.12" Microstrip

Figure 1. MRF9045MR1 930-960 MHz Broadband Test Circuit Schematic

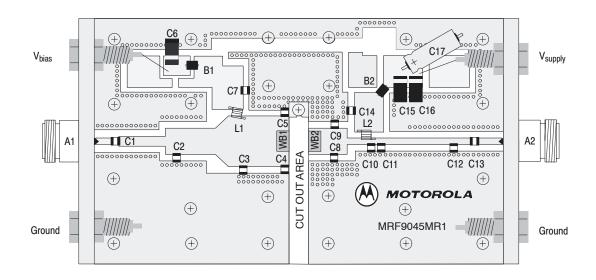
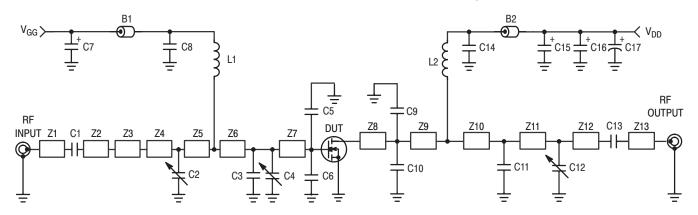


Figure 2. MRF9045MR1 930-960 MHz Broadband Test Circuit Component Layout



B1	Short Ferrite Bead	Z1	0.260" x 0.060" Microstrip
B2	Long Ferrite Bead	Z2	0.240" x 0.060" Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors, B Case	Z3	0.500" x 0.100" Microstrip
C2	0.4–2.5 pF Variable Capacitor, Johanson Gigatrim	Z4	0.215" x 0.270" Microstrip
C3	3.6 pF Chip Capacitor, B Case	Z5	0.315" x 0.270" Microstrip
C4	0.8-8.0 pF Variable Capacitor, Johanson Gigatrim	Z6	0.160" x 0.270" x 0.520" Taper
C5, C6, C9, C10	10 pF Chip Capacitors, B Case	<b>Z</b> 7	0.285" x 0.520" Microstrip
C7, C15, C16	10 μF, 35 V Tantalum Chip Capacitors	Z8	0.140" x 0.270" Microstrip
C11	7.5 pF Chip Capacitor, B Case	Z9	0.450" x 0.270" Microstrip
C12	0.6–4.5 pF Variable Capacitor, Johanson Gigatrim	Z10	0.250" x 0.060" Microstrip
C17	220 μF Electrolytic Chip Capacitor	Z11	0.720" x 0.060" Microstrip
L1, L2	12.5 nH Surface Mount Inductors	Z12	0.490" x 0.060" Microstrip
WB1, WB2	10 mil Brass Wear Blocks	Z13	0.290" x 0.060" Microstrip
		Board	Taconic RF–35–0300, $\varepsilon_r$ = 3.5

Figure 3. MRF9045MBR1 930-960 MHz Broadband Test Circuit Schematic

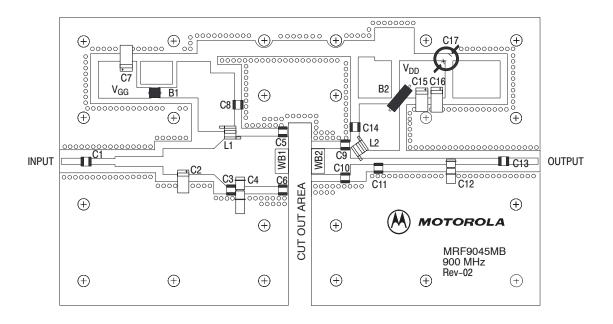


Figure 4. MRF9045MBR1 930-960 MHz Broadband Test Circuit Component Layout

#### TYPICAL CHARACTERISTICS

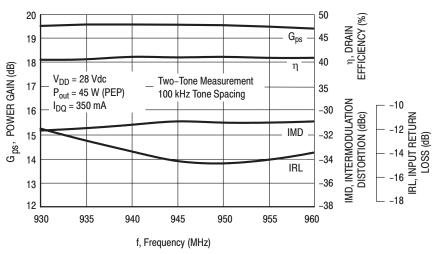


Figure 5. Class AB Broadband Circuit Performance

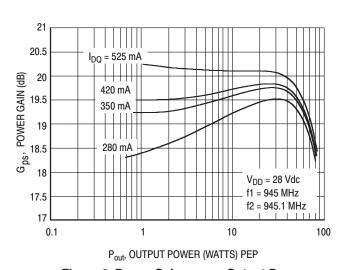


Figure 6. Power Gain versus Output Power

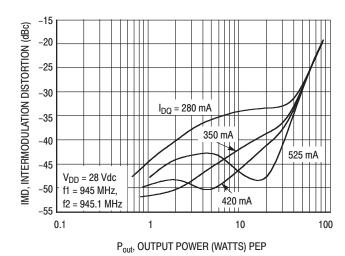


Figure 7. Intermodulation Distortion versus
Output Power

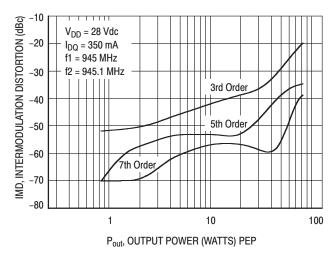


Figure 8. Intermodulation Distortion Products versus Output Power

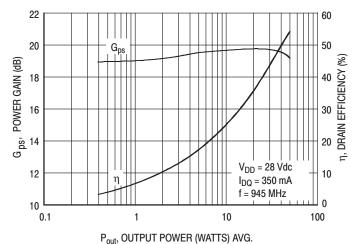


Figure 9. Power Gain and Efficiency versus Output Power

#### TYPICAL CHARACTERISTICS

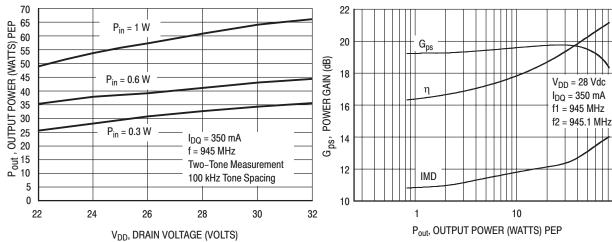


Figure 10. Output Voltage versus Supply Voltage (MRF9045MR1)

Figure 11. Power Gain, Efficiency and IMD versus Output Power (MRF9045MBR1)

60

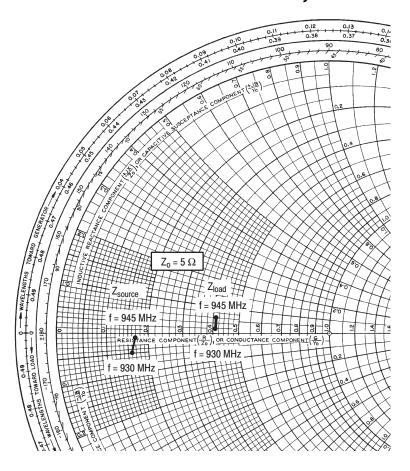
IMD, INTERMODULATION DISTORTION (dBc)

η, DRAIN EFFICIENCY (%)

0

-60

100



 $V_{DD}$  = 28 V,  $I_{DQ}$  = 350 mA,  $P_{out}$  = 45 W (PEP)

f MHz	$\mathbf{Z_{source}}_{\Omega}$	$\mathbf{Z_{load}}_{\Omega}$
930	0.81 – j0.25	2.03 + j0.09
945	0.85 – j0.05	2.03 + j0.28

 $Z_{source}$  = Test circuit impedance as measured from gate to ground.

Z<sub>load</sub> = Test circuit impedance as measured from drain to ground.

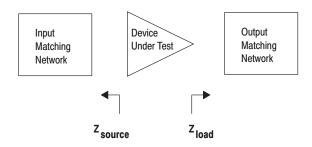
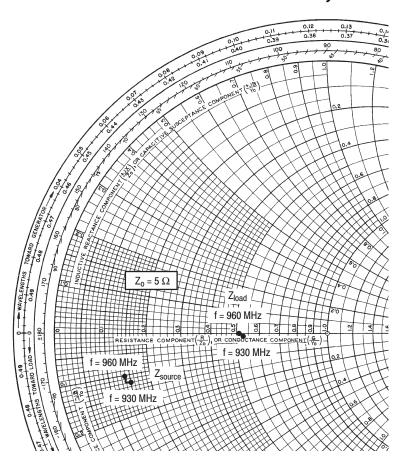


Figure 12. Series Equivalent Input and Output Impedance (MRF9045MR1)



 $V_{DD}$  = 28 V,  $I_{DQ}$  = 350 mA,  $P_{out}$  = 45 W (PEP)

f MHz	$\mathbf{Z_{source}}_{\Omega}$	$oldsymbol{Z_{load}}{\Omega}$	
930	0.75 – j0.6	2.65 – j0.05	
945	0.72 - j0.6	2.60 — j0.05	
960	0.70 – j0.5	2.55 – j0.02	

Test circuit impedance as measured from gate to ground.

 $Z_{load}$ Test circuit impedance as measured from drain to ground.

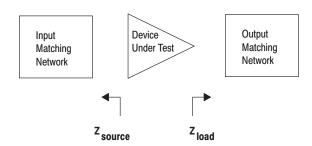
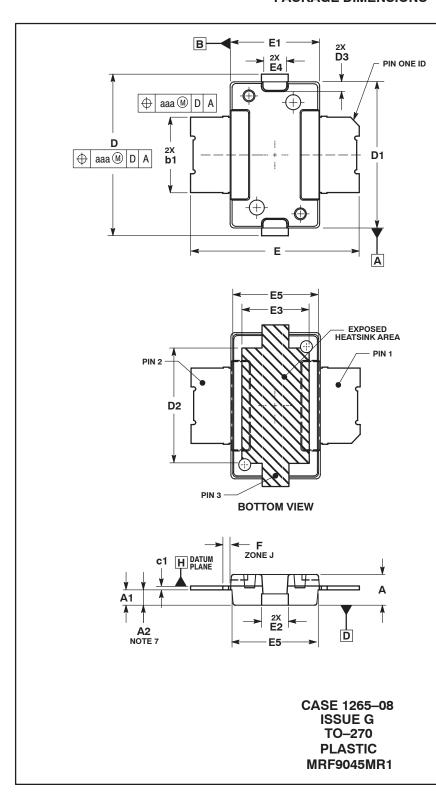


Figure 13. Series Equivalent Input and Output Impedance (MRF9045MBR1)

#### PACKAGE DIMENSIONS



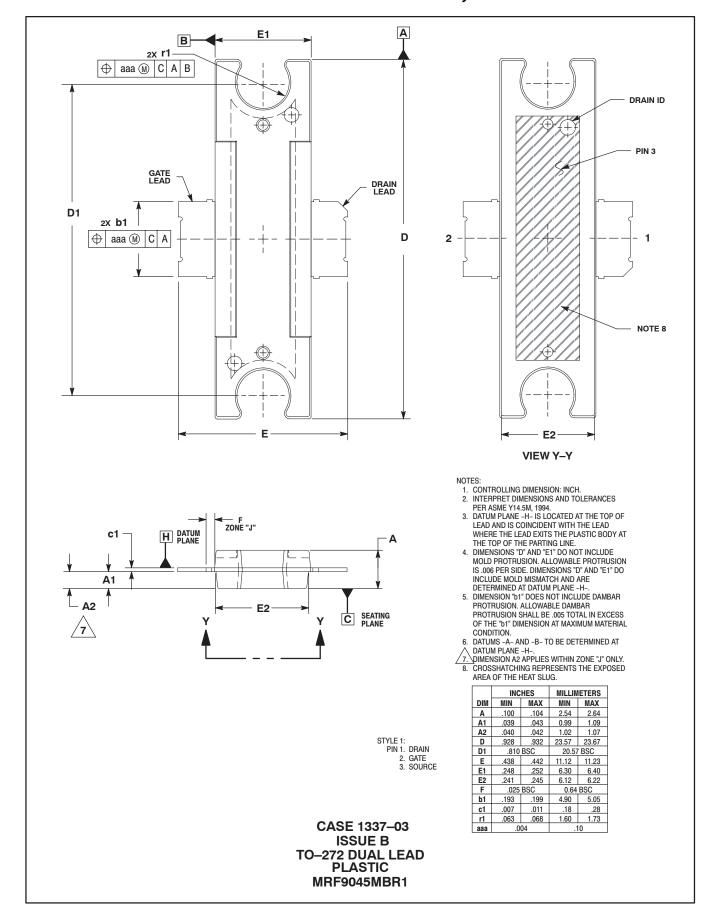
- NOTES:
  1. CONTROLLING DIMENSION: INCH.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
- 4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETER-
- MINED AT DATUM PLANE -H-.

  5. DIMENSION 61 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. DATUMS -A- AND -B- TO BE DETERMINED AT
- DATUM PLANE -H-.
  DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
- DIMENSIONS "D" AND "E2" DO NOT INCLUDE
  MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETER-MINED AT DATUM PLANE -D-

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	.078	.082	1.98	2.08
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.416	.424	10.57	10.77
D1	.378	.382	9.60	9.70
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.436	.444	11.07	11.28
E1	.238	.242	6.04	6.15
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
E5	.231	.235	5.87	5.97
F	.025	BSC	0.64 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
aaa	.0	04	0.10	

STYLE 1: PIN 1. DRAIN

- 2. GATE 3. SOURCE



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