

BLF6G15L-40BRN

Power LDMOS transistor

Rev. 2 — 12 November 2010

Product data sheet

1. Product profile

1.1 General description

40 W LDMOS power transistor for base station applications at frequencies from 1450 MHz to 1550 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25^\circ\text{C}$ in a class-AB production test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	1476 to 1511	28	2.5	22.0	13.0	-45 [1]

[1] Test signal: 3GPP test model 1, 64 DPCH; PAR = 7.5 dB at probability of 0.01% on CCDF carrier; carrier spacing 5 MHz.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical 2-carrier W-CDMA performance at frequencies of 1476 MHz and 1511 MHz, a supply voltage of 28 V and an I_{Dq} of 330 mA:
 - ◆ Average output power = 2.5 W
 - ◆ Power gain = 22.0 dB
 - ◆ Efficiency = 13.0 %
 - ◆ ACPR = -45 dBc
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1450 MHz to 1550 MHz)
- Internally matched for ease of use
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC.
- Integrated current sense



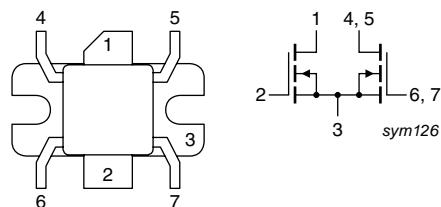
1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 1450 MHz to 1550 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source	[1]	
4, 5	sense drain		
6, 7	sense gate		



[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
BLF6G15L-40BRN	-	flanged ceramic package; 2 mounting holes; 6 leads		SOT1112A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+11	V
$V_{GS(\text{sense})}$	sense gate-source voltage		-0.5	+9	V
I_D	drain current		-	11	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Type	Unit
$R_{th(j\text{-case})}$	thermal resistance from junction to case	$T_{case} = 80 \text{ °C}; P_L = 2.5 \text{ W (CW)}$	1.6	K/W

6. Characteristics

Table 6. Characteristics $T_j = 25^\circ\text{C}$ per section; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$V_{\text{GS}} = 0 \text{ V}; I_D = 0.59 \text{ mA}$	65	-	-	V
$V_{\text{GS}(\text{th})}$	gate-source threshold voltage	$V_{\text{DS}} = 10 \text{ V}; I_D = 59 \text{ mA}$	1.4	1.9	2.4	V
I_{Dq}	quiescent drain current	sense transistor: $I_{\text{DS}} = 5.1 \text{ mA}; V_{\text{DS}} = 12 \text{ V}$ main transistor: $V_{\text{DS}} = 28 \text{ V}$	280	330	380	mA
I_{DSS}	drain leakage current	$V_{\text{GS}} = 0 \text{ V}; V_{\text{DS}} = 28 \text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{\text{GS}} = V_{\text{GS}(\text{th})} + 3.75 \text{ V}; V_{\text{DS}} = 10 \text{ V}$	8.8	10	-	A
I_{GSS}	gate leakage current	$V_{\text{GS}} = 11 \text{ V}; V_{\text{DS}} = 0 \text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{\text{DS}} = 10 \text{ V}; I_D = 2.9 \text{ A}$	2.7	4.3	-	S
$R_{\text{DS}(\text{on})}$	drain-source on-state resistance	$V_{\text{GS}} = V_{\text{GS}(\text{th})} + 3.75 \text{ V}; I_D = 2.06 \text{ A}$	0.09	0.25	0.39	Ω

7. Application information

Table 7. 2-carrier W-CDMA RF performance

Class-AB production test circuit; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; $f_1 = 1473.4 \text{ MHz}$; $f_2 = 1478.4 \text{ MHz}$; $f_3 = 1508.4 \text{ MHz}$; $f_4 = 1513.4 \text{ MHz}$; RF performance at $V_{\text{DS}} = 28 \text{ V}$; $I_{\text{Dq}} = 330 \text{ mA}$; $T_{\text{case}} = 25^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{\text{L}(\text{AV})}$	average output power		-	2.5	-	W
G_p	power gain	$P_{\text{L}(\text{AV})} = 2.5 \text{ W}$	19.8	22.0	-	dB
RL_{in}	input return loss	$P_{\text{L}(\text{AV})} = 2.5 \text{ W}$	10	15	-	dB
η_{D}	drain efficiency	$P_{\text{L}(\text{AV})} = 2.5 \text{ W}$	11	13	-	%
ACPR	adjacent channel power ratio	$P_{\text{L}(\text{AV})} = 2.5 \text{ W}$	-	-45	-40	dBc

Table 8. 1 carrier W-CDMA PAR performance

Class-AB production test circuit; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; $f_1 = 1510.9 \text{ MHz}$; RF performance at $V_{\text{DS}} = 28 \text{ V}$; $I_{\text{Dq}} = 330 \text{ mA}$; $T_{\text{case}} = 25^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_0	output peak-to-average ratio	$P_{\text{L}(\text{AV})} = 10 \text{ W}$ at 0.01 % probability on CCDF	5.3	6.0	-	dB

7.1 Ruggedness in class-AB operation

The BLF6G15L-40BRN is capable of withstanding a load mismatch corresponding to $\text{VSWR} = 10 : 1$ through all phases under the following conditions: $V_{\text{DS}} = 28 \text{ V}$; $I_{\text{Dq}} = 330 \text{ mA}$; $P_{\text{L}} = 30 \text{ W}$; $f = 1475 \text{ MHz}$ (CW).

7.2 Impedance information

Table 9. Typical impedance per section

$I_{Dq} = 330 \text{ mA}$; main transistor $V_{DS} = 28 \text{ V}$

f (MHz)	Z_S ^[1] (Ω)	Z_L ^[1] (Ω)
1480	$3.2 - j6.3$	$4.6 - j4.5$
1510	$4.4 - j6.5$	$4.6 - j4.5$

[1] Z_S and Z_L defined in [Figure 1](#).

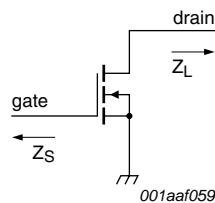
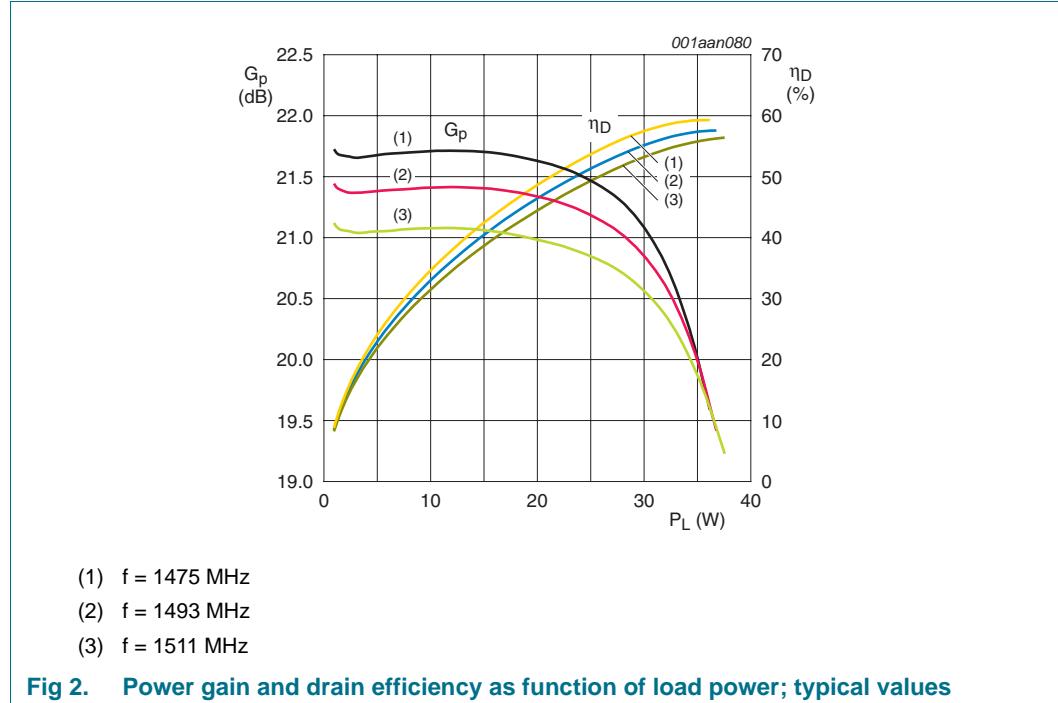


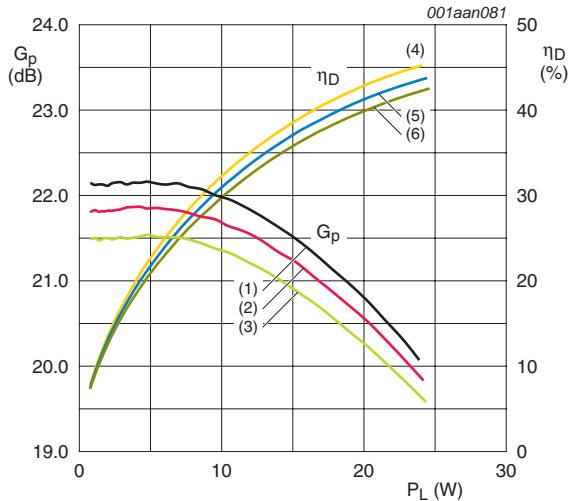
Fig 1. Definition of transistor impedance

7.3 Graphs

7.3.1 CW



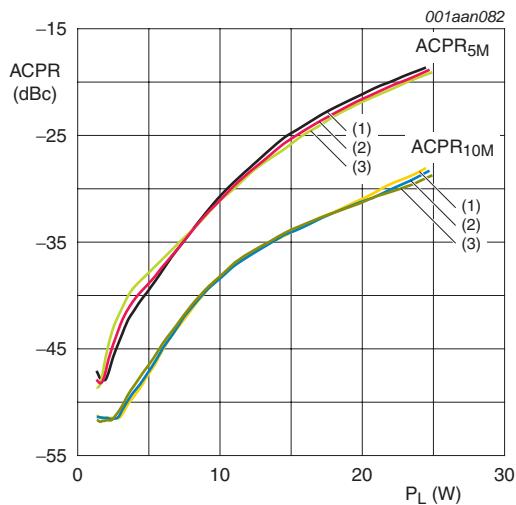
7.3.2 2C-WCDMA (5 MHz spacing)



3GPP, test model 1; 64 DPCH, PAR = 7.5 dB at 0.01 % probability per carrier. 5 MHz carrier spacing.

- (1) $f = 1475$ MHz
- (2) $f = 1493$ MHz
- (3) $f = 1511$ MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values

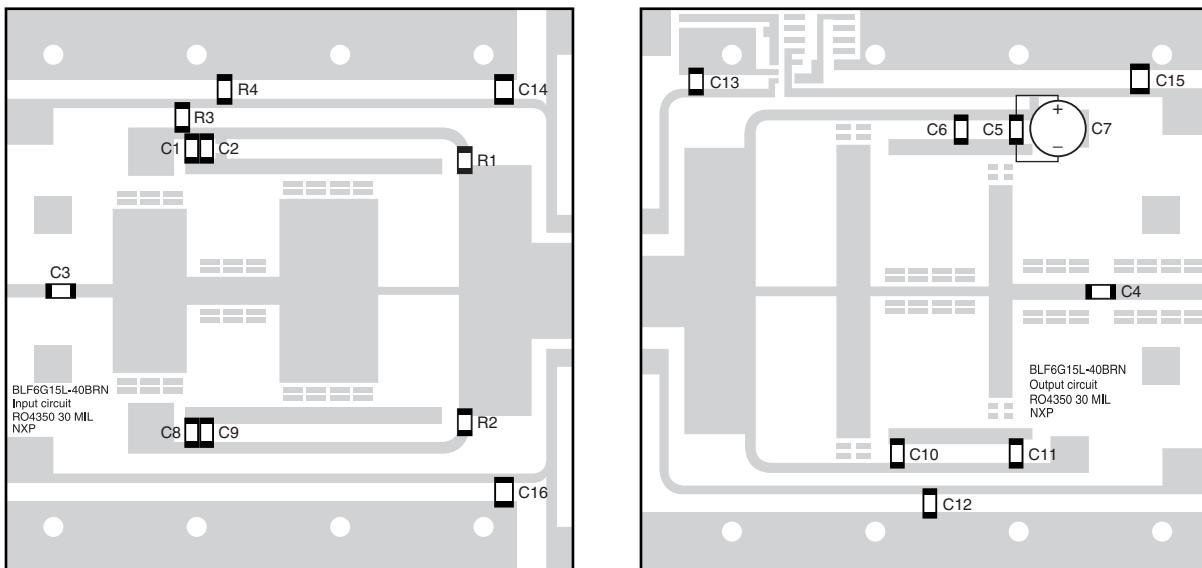


3GPP, test model 1; 64 DPCH, PAR = 7.5 dB at 0.01 % probability per carrier. 5 MHz carrier spacing.

- (1) $f = 1475$ MHz
- (2) $f = 1493$ MHz
- (3) $f = 1511$ MHz

Fig 4. Adjacent channel power ratio as a function of load power; typical values

8. Test information



014aab103

Printed-Circuit Board (PCB): Rogers RO4350; $\epsilon_r = 3.5$ F/m; thickness = 0.762 mm; thickness copper plating = 35 μm .

The vias can be as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See [Table 10](#) for list of components.

Fig 5. Component layout

Table 10. List of components

See [Figure 5](#) for component layout.

Component	Description	Value	Remarks
C1, C8	multilayer ceramic chip capacitor	68 pF	[1]
C2, C6, C9	multilayer ceramic chip capacitor	160 pF	[1]
C3, C4	multilayer ceramic chip capacitor	24 pF	[2]
C5, C11	multilayer ceramic chip capacitor	47 pF	[1]
C7	electrolytic capacitor	470 μF ; 63 V	
C10	multilayer ceramic chip capacitor	15 pF	[1]
C12	multilayer ceramic chip capacitor	43 pF	[1]
C13	multilayer ceramic chip capacitor	20 pF	[1]
C14, C15	multilayer ceramic chip capacitor	1 μF	Murata 0603
C16	multilayer ceramic chip capacitor	100 pF	
R1, R2	chip resistor	15 Ω	Philips 0603
R3	chip resistor	820 Ω	Philips 0603
R4	chip resistor	1.8 k Ω	Philips 0603

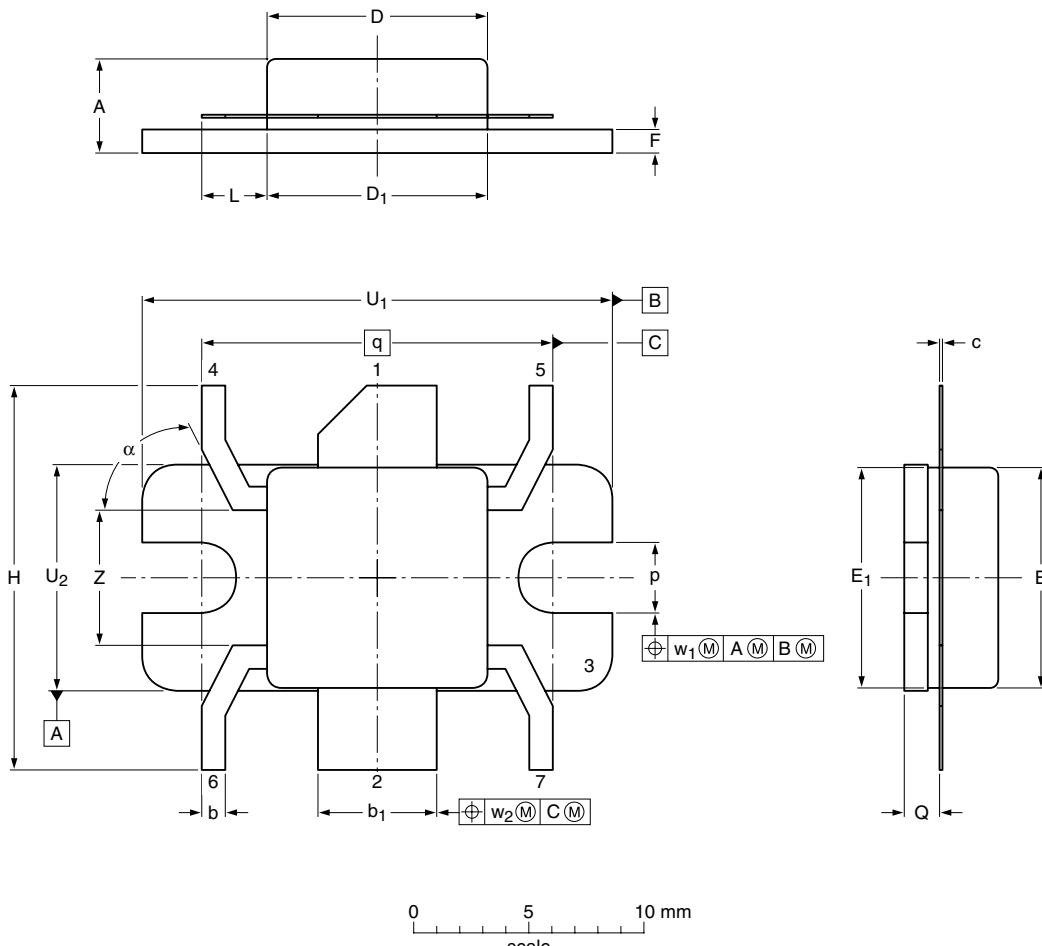
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 800B or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 6 leads

SOT1112A



Dimensions

Unit ⁽¹⁾	A	b	b ₁	c	D	D ₁	E	E ₁	F	H	L	p	Q ⁽²⁾	q	U ₁	U ₂	w ₁	w ₂	Z	α
mm max	4.65	1.14	5.26	0.18	9.65	9.65	9.65	9.65	1.14	17.12	3.00	3.30	1.70	20.45	9.91	0.25	0.51	5.97	64°	
mm nom	3.76	0.89	5.00	0.10	9.40	9.40	9.40	9.40	0.89	16.10	2.69	2.92	1.45	15.24	20.19	9.65	0.25	0.51	5.72	62°
inches max	0.183	0.045	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.674	0.118	0.130	0.067	0.805	0.39	0.235	0.01	0.02	0.225	64°
inches nom	0.148	0.035	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.634	0.106	0.115	0.057	0.795	0.38	0.225	0.01	0.02	0.225	62°

Note

1. millimeter dimensions are derived from the original inch dimensions.

2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1112a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1112A					09-10-12	10-02-02

Fig 6. Package outline SOT1112A

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
DPCCH	Dedicated Physical Channel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G15L-40BRN v.2	20101112	Product data sheet	-	BLF6G15L-40BRN v.1
Modifications:	• Data sheet status changed from Preliminary sheet to Product data			
BLF6G15L-40BRN v.1	20100914	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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