

# BLL6G1214L-250

LDMOS L-band radar power transistor

Rev. 1 — 16 February 2012

Preliminary data sheet

## 1. Product profile

### 1.1 General description

250 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

**Table 1. Test information**

Typical RF performance at  $T_{case} = 25^\circ\text{C}$ ;  $t_p = 1\text{ ms}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 150\text{ mA}$ ; in a class-AB production test circuit.

Test signal	f (GHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	t <sub>r</sub> (ns)	t <sub>f</sub> (ns)
pulsed RF	1.2 to 1.4	36	250	15	45	15	5

### 1.2 Features and benefits

- Typical pulsed RF performance at a frequency of 1.2 GHz to 1.4 GHz, a supply voltage of 36 V, an  $I_{Dq}$  of 150 mA, a  $t_p$  of 1 ms with  $\delta$  of 10 %:
  - ◆ Output power = 250 W
  - ◆ Power gain = 15 dB
  - ◆ Efficiency = 45 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

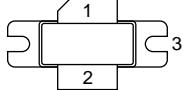
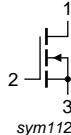
### 1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source	[1]	 

[1] Connected to flange

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package			Version
	Name	Description		
BLL6G1214L-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads		SOT502A

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	89	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$I_D$	drain current		-	59	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 85^\circ\text{C}$ ; $P_L = 250 \text{ W}$	0.244	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85^\circ\text{C}$ ; $P_L = 250 \text{ W}$	[1]	
		$t_p = 1000 \mu\text{s}$ ; $\delta = 10\%$	0.124	K/W
		$t_p = 100 \mu\text{s}$ ; $\delta = 10\%$	0.059	K/W
		$t_p = 200 \mu\text{s}$ ; $\delta = 10\%$	0.077	K/W
		$t_p = 300 \mu\text{s}$ ; $\delta = 10\%$	0.088	K/W
		$t_p = 100 \mu\text{s}$ ; $\delta = 20\%$	0.078	K/W

[1]  $Z_{th(j-c)}$  values are calculated from results obtained with ANSYS simulations and confirmed with IR measurements during development stage. During production: guaranteed by design.

## 6. Characteristics

**Table 6. DC Characteristics**

$T_j = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}$ ; $I_D = 3.36 \text{ mA}$	91.5	-	105.5	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 20 \text{ V}$ ; $I_D = 336 \text{ mA}$	1.4	1.9	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 42 \text{ V}$	-	-	4.2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V}$ ; $V_{DS} = 10 \text{ V}$	50	59	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11 \text{ V}$ ; $V_{DS} = 0 \text{ V}$	-	-	420	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}$ ; $I_D = 336 \text{ mA}$	51.6	-	-	mS
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V}$ ; $I_D = 11.7 \text{ A}$	-	-	127	$\text{m}\Omega$
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 40 \text{ V}$ ; $f = 1 \text{ MHz}$	-	285	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 40 \text{ V}$ ; $f = 1 \text{ MHz}$	-	90	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 40 \text{ V}$ ; $f = 1 \text{ MHz}$	-	3	-	pF

**Table 7. RF characteristics**

Test signal: pulsed RF;  $t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ ; RF performance at  $V_{DS} = 36 \text{ V}$ ;  $I_{Dq} = 150 \text{ mA}$ ;  $T_{case} = 25^\circ\text{C}$ ; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage		-	-	36	V
$I_{Dq}$	quiescent drain current	No RF applied	-	150	-	mA
$P_L$	output power		250	-	-	W
$f_{range}$	frequency range		1200	-	1400	MHz
$t_p$	pulse duration	$\delta = 10\%$	-	-	1	ms
		$\delta = 20\%$	-	-	100	$\mu\text{s}$

**Table 7. RF characteristics ...continued**

Test signal: pulsed RF;  $t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ ; RF performance at  $V_{DS} = 36 \text{ V}$ ;  $I_{Dq} = 150 \text{ mA}$ ;  $T_{case} = 25^\circ\text{C}$ ; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\eta_D$	drain efficiency		42	45	-	%
$t_r$	rise time	$P_L = 250 \text{ W}$	[1]	-	-	200 ns
$t_f$	fall time	$P_L = 250 \text{ W}$	[1]	-	-	200 ns
$G_p$	power gain		13	15	-	dB
$P_{droop(pulse)}$	pulse droop power		-	-	0.6	dB
$RL_{in}$	input return loss		-	-	-8	dB

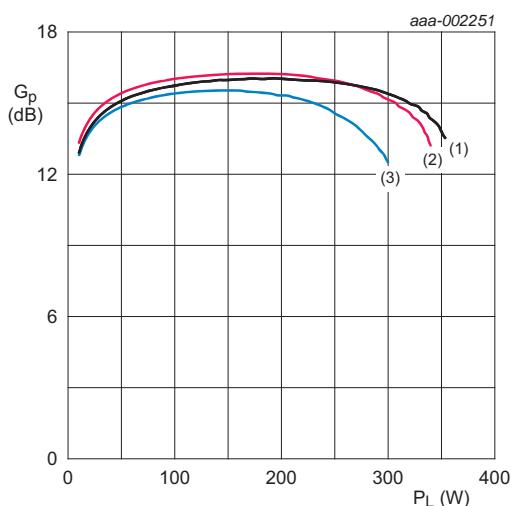
[1] The rise and fall time of the input circuit will be 5 ns maximum.

## 6.1 Ruggedness in class-AB operation

The BLL6G1214L-250 is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 36 \text{ V}$ ;  $I_{Dq} = 150 \text{ mA}$ ;  $P_L = 250 \text{ W}$ ;  $t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ .

## 7. Application information

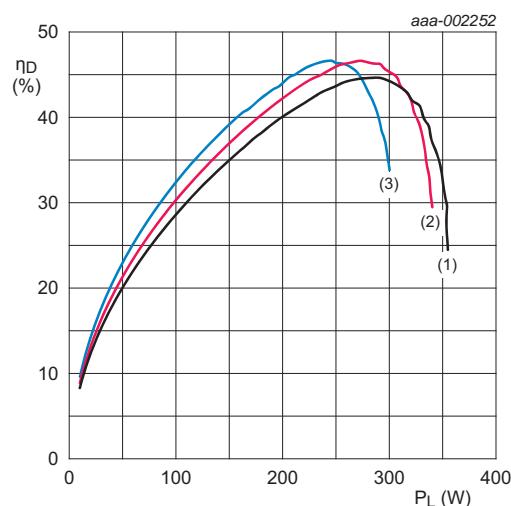
### 7.1 Graphs



$t_p = 100 \mu\text{s}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

- (1)  $f = 1200 \text{ MHz}$
- (2)  $f = 1300 \text{ MHz}$
- (3)  $f = 1400 \text{ MHz}$

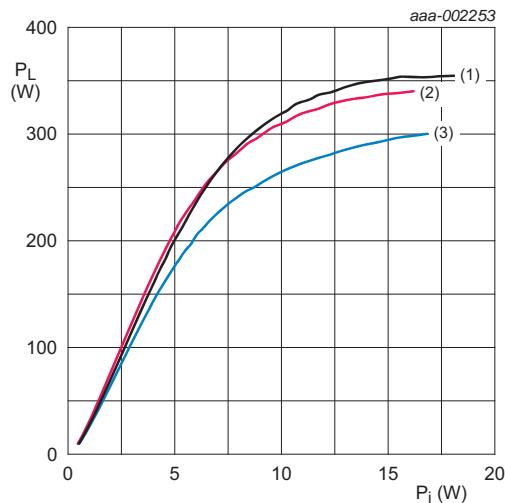
**Fig 1. Power gain as a function of output power; typical values**



$t_p = 100 \mu\text{s}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

- (1)  $f = 1200 \text{ MHz}$
- (2)  $f = 1300 \text{ MHz}$
- (3)  $f = 1400 \text{ MHz}$

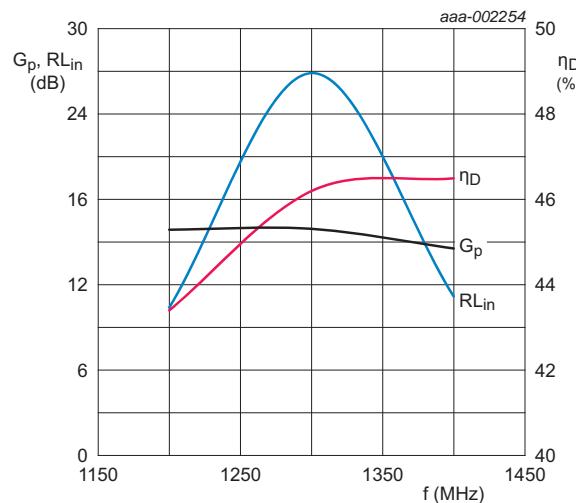
**Fig 2. Drain efficiency as a function of output power; typical values**



$t_p = 100 \mu\text{s}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

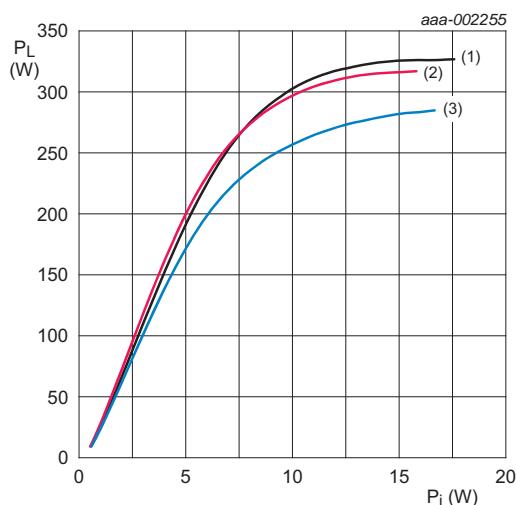
(1)  $f = 1200 \text{ MHz}$   
 (2)  $f = 1300 \text{ MHz}$   
 (3)  $f = 1400 \text{ MHz}$

**Fig 3.** Output power as a function of input power; typical values



$P_L = 250 \text{ W}$ ;  $t_p = 100 \mu\text{s}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

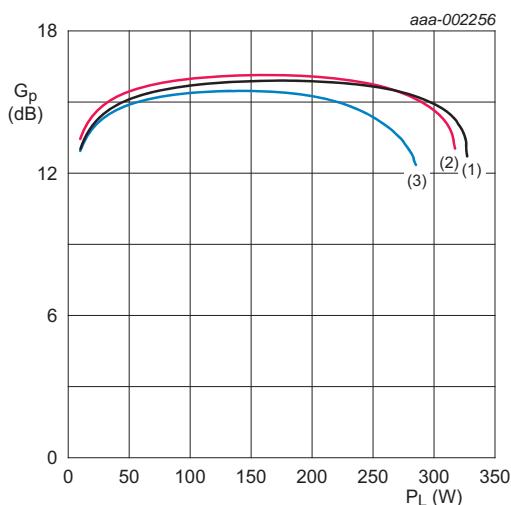
**Fig 4.** Power gain, input return loss and drain efficiency as function of frequency; typical values



$t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

(1)  $f = 1200 \text{ MHz}$   
 (2)  $f = 1300 \text{ MHz}$   
 (3)  $f = 1400 \text{ MHz}$

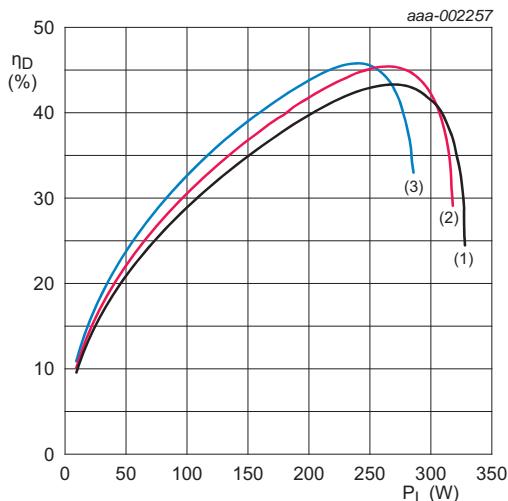
**Fig 5.** Output power as a function of input power; typical values



$t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

(1)  $f = 1200 \text{ MHz}$   
 (2)  $f = 1300 \text{ MHz}$   
 (3)  $f = 1400 \text{ MHz}$

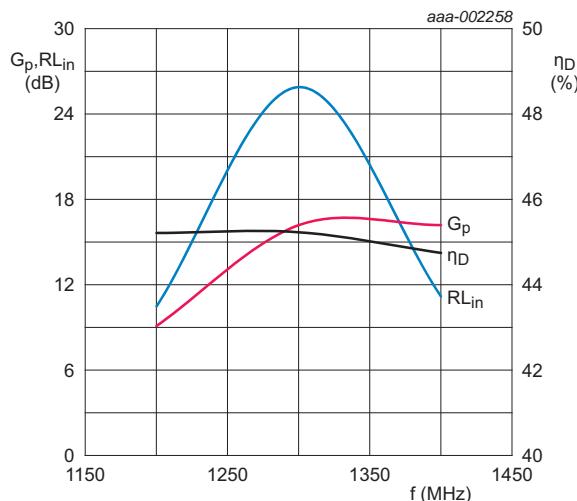
**Fig 6.** Power gain as a function of output power; typical values



$t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

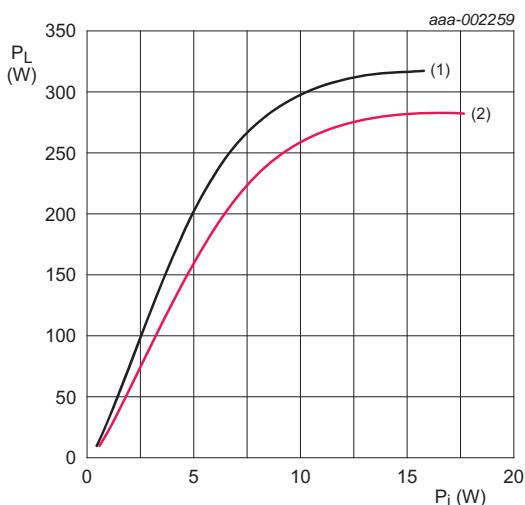
- (1)  $f = 1200 \text{ MHz}$
- (2)  $f = 1300 \text{ MHz}$
- (3)  $f = 1400 \text{ MHz}$

**Fig 7. Drain efficiency as a function of output power; typical values**



$P_L = 250 \text{ W}$ ;  $t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ ;  $T_h = 25^\circ\text{C}$ .

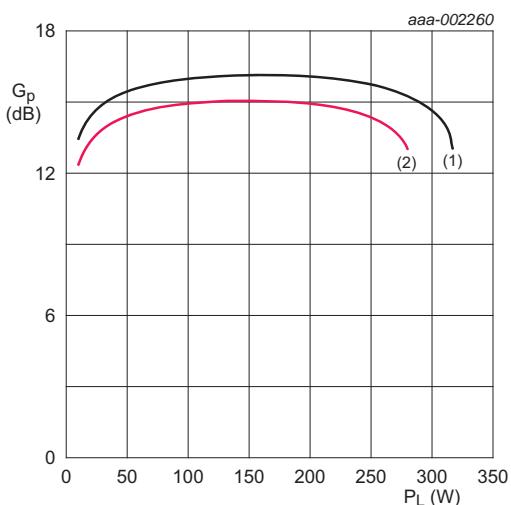
**Fig 8. Power gain, input return loss and drain efficiency as function of frequency; typical values**



$f = 1300 \text{ MHz}$ ;  $t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ .

- (1)  $T_h = 25^\circ\text{C}$
- (2)  $T_h = 85^\circ\text{C}$

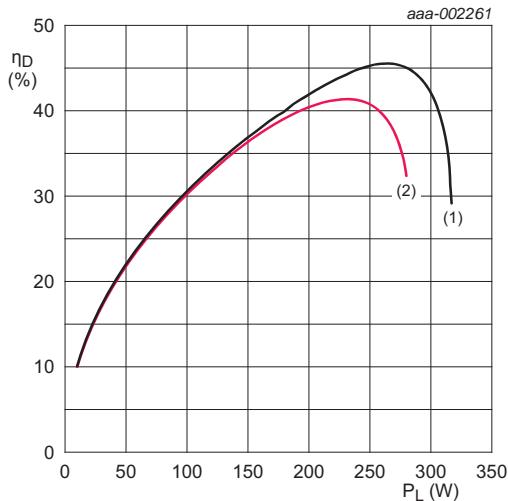
**Fig 9. Output power as a function of input power; typical values**



$f = 1300 \text{ MHz}$ ;  $t_p = 1 \text{ ms}$ ;  $\delta = 10\%$ .

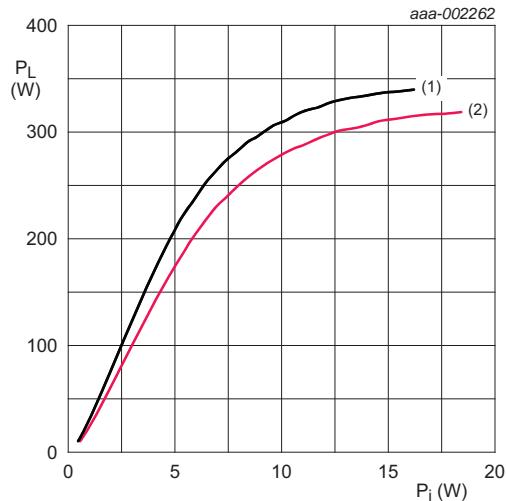
- (1)  $T_h = 25^\circ\text{C}$
- (2)  $T_h = 85^\circ\text{C}$

**Fig 10. Power gain as a function of output power; typical values**



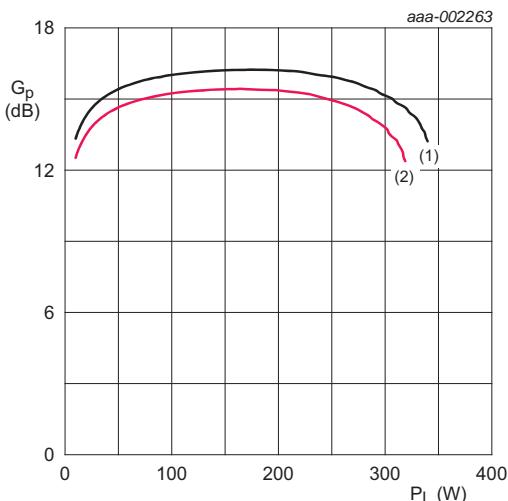
**Fig 11. Drain efficiency as a function of output power; typical values**

$f = 1300\text{ MHz}; t_p = 1\text{ ms}; \delta = 10\text{ \%}.$   
(1)  $T_h = 25\text{ }^\circ\text{C}$   
(2)  $T_h = 85\text{ }^\circ\text{C}$



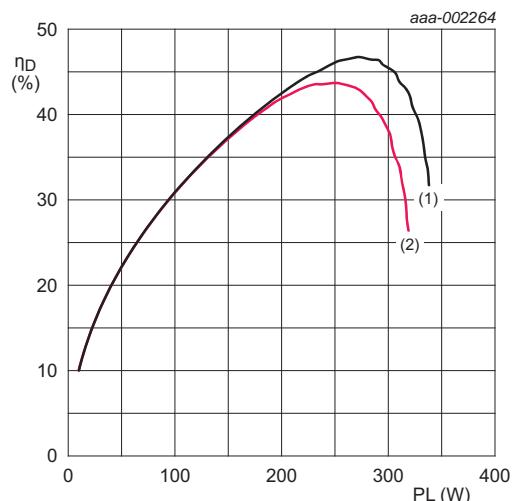
**Fig 12. Output power as a function of input power; typical values**

$f = 1300\text{ MHz}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ \%}.$   
(1)  $T_h = 25\text{ }^\circ\text{C}$   
(2)  $T_h = 85\text{ }^\circ\text{C}$



**Fig 13. Power gain as a function of output power; typical values**

$f = 1300\text{ MHz}; t_p = 1\text{ ms}; \delta = 10\text{ \%}.$   
(1)  $T_h = 25\text{ }^\circ\text{C}$   
(2)  $T_h = 85\text{ }^\circ\text{C}$



**Fig 14. Drain efficiency as a function of output power; typical values**

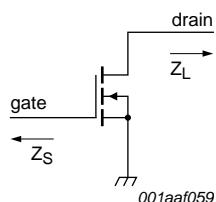
$f = 1300\text{ MHz}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ \%}.$   
(1)  $T_h = 25\text{ }^\circ\text{C}$   
(2)  $T_h = 85\text{ }^\circ\text{C}$

## 7.2 Impedance information

**Table 8. Typical impedance**

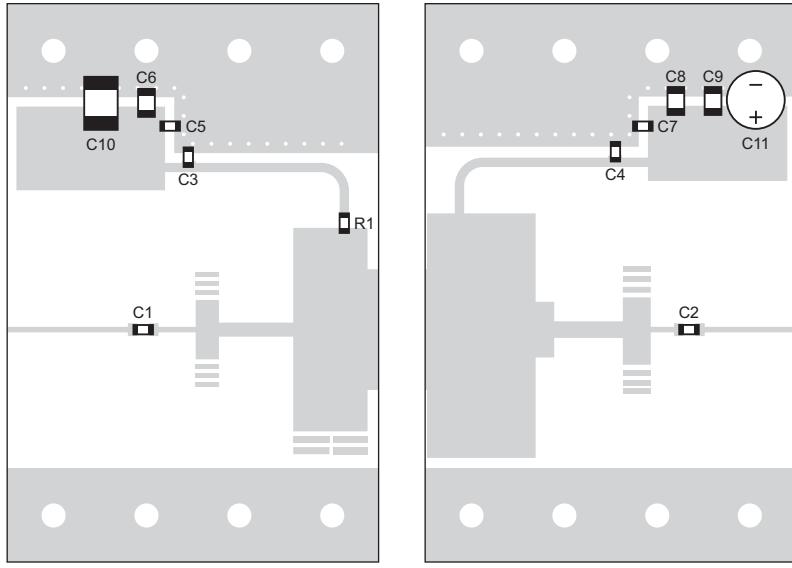
Typical values unless otherwise specified.

f GHz	$Z_S$ $\Omega$	$Z_L$ $\Omega$
1.2	$1.077 - j2.78$	$1.288 - j1.014$
1.3	$1.352 - j2.949$	$1.139 - j1.086$
1.4	$1.881 - j2.640$	$1.038 - j1.132$



**Fig 15. Definition of transistor impedance**

## 7.3 Circuit information



Printed-Circuit Board (PCB): Duroid 6010;  $\epsilon_r = 10.15$ ; thickness = 0.64 mm;  
thickness copper plating = 35  $\mu\text{m}$ .

See [Table 9](#) for a list of components.

**Fig 16. Component layout for application circuit**

**Table 9. List of components**For test circuit see [Figure 16](#).

Component	Description	Value	Remarks
C1, C2, C3, C4, C7	multilayer ceramic chip capacitor	56 pF	<a href="#">[1]</a>
C5, C8	multilayer ceramic chip capacitor	200 pF	<a href="#">[2]</a>
C6, C9	multilayer ceramic chip capacitor	1 nF	<a href="#">[3]</a>
C10	multilayer ceramic chip capacitor	10 µF; 20 V	
C11	electrolytic capacitor	22 µF; 63 V	
R1	SMD resistor	10 Ω	0603

[1] American Technical Ceramics type 100A or capacitor of same quality.

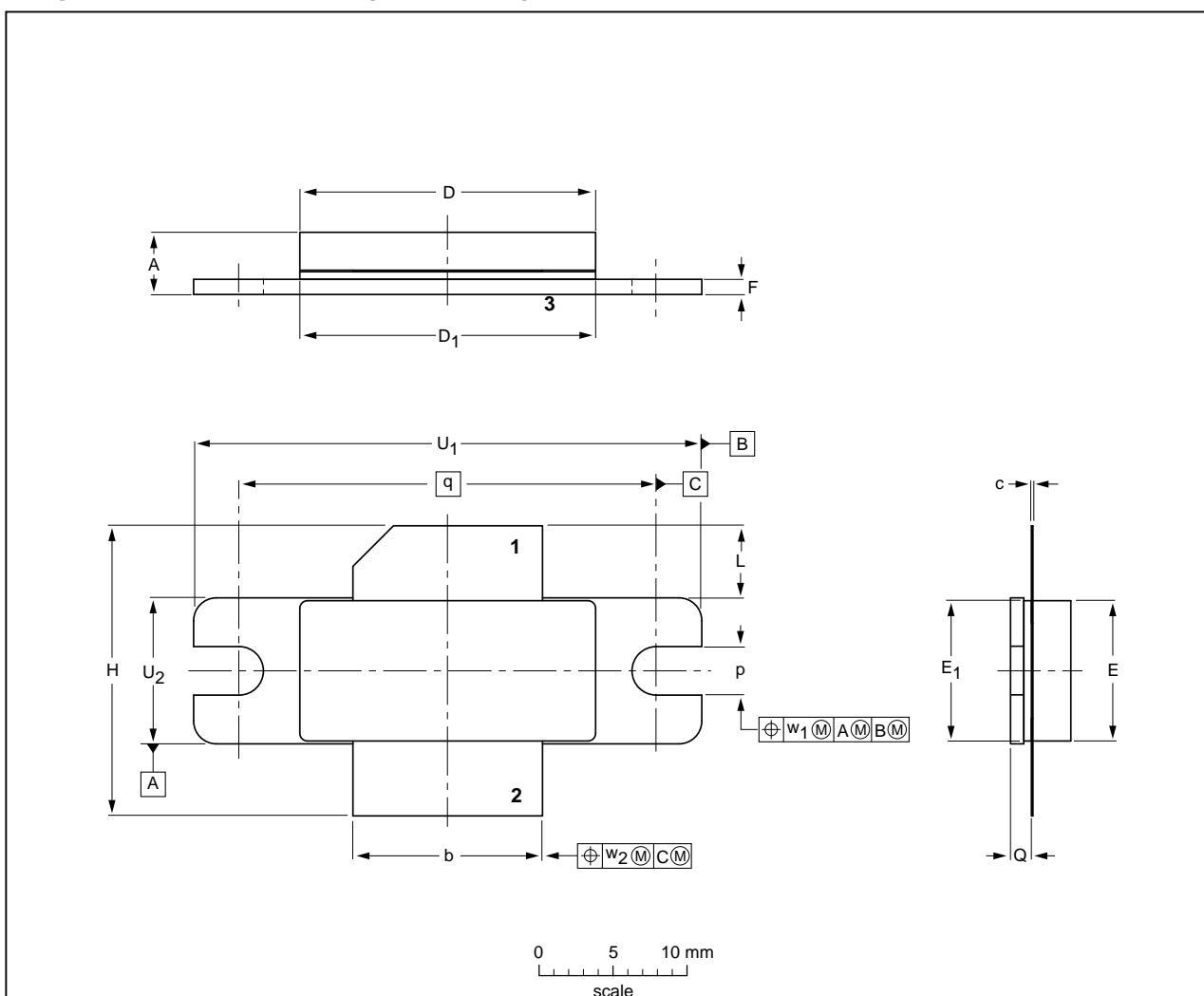
[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 700A or capacitor of same quality.

## 8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94 31.12	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100 1.057	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						-99-12-28 03-01-10

Fig 17. Package outline SOT502A

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
DC	Direct Current
ESD	ElectroStatic Discharge
IR	InfraRed
L-band	Long wave band
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6G1214L-250 v.1	20120216	Preliminary data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 14. Contents

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<b>1</b>	<b>Product profile</b>	<b>1</b>
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
<b>2</b>	<b>Pinning information</b>	<b>2</b>
<b>3</b>	<b>Ordering information</b>	<b>2</b>
<b>4</b>	<b>Limiting values</b>	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b>	<b>3</b>
<b>6</b>	<b>Characteristics</b>	<b>3</b>
6.1	Ruggedness in class-AB operation	4
<b>7</b>	<b>Application information</b>	<b>4</b>
7.1	Graphs	4
7.2	Impedance information	8
7.3	Circuit information	8
<b>8</b>	<b>Package outline</b>	<b>10</b>
<b>9</b>	<b>Handling information</b>	<b>11</b>
<b>10</b>	<b>Abbreviations</b>	<b>11</b>
<b>11</b>	<b>Revision history</b>	<b>11</b>
<b>12</b>	<b>Legal information</b>	<b>12</b>
12.1	Data sheet status	12
12.2	Definitions	12
12.3	Disclaimers	12
12.4	Trademarks	13
<b>13</b>	<b>Contact information</b>	<b>13</b>
<b>14</b>	<b>Contents</b>	<b>14</b>

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