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3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION

FEATURES

- Qualified for Automotive Applications
- ESD Protection for RS-232 Bus Pins
 - ±15-kV Human Body Model (HBM)
 - ±8 kV (IEC61000-4-2, Contact Discharge)
 - ±15 kV (IEC61000-4-2, Air-Gap Discharge)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- · Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current: 300 μA (Typ)
- External Capacitors: 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- Pin Compatible to Alternative High-Speed Device (1 Mbit/s): TRSF3232E

PW PACKAGE (TOP VIEW) \square V_{cc} C1+ ___ 16 15 C1- 🖂 14 C2+ ____ 13 C2- ____ 5 12 V− ___ ☐ DIN1 11 DOUT2 ___ 10 RIN2 ___ 9

DESCRIPTION

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate.

ORDERING INFORMATION⁽¹⁾

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP - PW	Reel of 2000	TRS3232EQPWRQ1	RS32EQ

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTION TABLES

Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	Н
Н	L

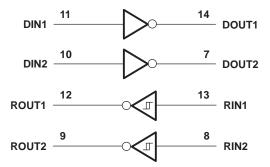
(1) H = high level, L = low level

Each Receiver⁽¹⁾

INPUT RIN	OUTPUT ROUT
L	Н
Н	L
Open	Н

(1) H = high level, L = low level, Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)





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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range (2)		−0.3 V to 6 V	
V+	Positive output supply voltage range (2)		–0.3 V to 7 V	
V-	Negative output supply voltage range ⁽²⁾		0.3 V to -7 V	
V+ - V-	Supply voltage difference ⁽²⁾		13 V	
V	Input voltage range	Drive	Drivers	−0.3 V to 6 V
V _I	input voltage range	Receivers	–25 V to 25 V	
\/	Output valtage reserve	Drivers	-13.2 V to 13.2 V	
Vo	Output voltage range	Receivers	-0.3 V to V _{CC} + 0.3 V	
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾		108°C/W	
T_{J}	Operating virtual-junction temperature		150°C	
T _{stg}	Storage temperature range		–65°C to 150°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

See Figure 4

			MIN	NOM	MAX	UNIT
\/	Cumply yeltore	V _{CC} = 3.3 V	3	3.3	3.6	V
V _{CC}	Supply voltage	V _{CC} = 5 V	4.5	5	5.5	V
\/	Driver high-level input voltage, DIN	V _{CC} = 3.3 V	2		5.5	V
V _{IH}	Diver high-lever input voltage, Div	V _{CC} = 5 V	2.4		3.3 3.6 5 5.5	V
V_{IL}	Driver low-level input voltage, DIN		0		0.8	V
V_{I}	Receiver input voltage		-25		25	V
T _A	Operating free-air temperature		-40		125	ç

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

ELECTRICAL CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN TYP ⁽²⁾	MAX	UNIT
I _{CC}	Supply current	No load, V _{CC} = 3.3 V or 5 V	0.3	1	mΑ

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

All voltages are with respect to network GND.

Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. The package thermal impedance is calculated in accordance with JESD 51-7.

All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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DRIVER SECTION

ELECTRICAL CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND, DIN = GND	5	5.4		٧
V_{OL}	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND, DIN = V_{CC}	- 5	-5.4		V
I_{IH}	High-level input current	$V_I = V_{CC}$		±0.01	±1	μΑ
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μΑ
(3)	Short-circuit output current	$V_{CC} = 3.6 \text{ V}, V_{O} = 0 \text{ V}$		±35	±60	~ ^
I _{OS} (3)	Short-circuit output current	$V_{CC} = 5.5 \text{ V}, V_{O} = 0 \text{ V}$		±35	±60	mA
r _o	Output resistance	V_{CC} , V+, and V- = 0 V, V_{O} = ±2 V	300	10M		Ω

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

SWITCHING CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT	
Maximum data rate $ C_L = 1000 \text{ pF}, \ R_L = 3 \text{ k}\Omega, \ \text{One DOUT switching}, $ See Figure 1		150	250		kbit/s			
t _{sk(p)}	Pulse skew ⁽³⁾	C_L = 150 pF to 2500 pF, R_L = 3 k Ω to 7 k Ω , See Figure 2			300		ns	
CD(+*)	Slew rate, transition region	$R_L = 3 k\Omega$ to $7 k\Omega$,	C _L = 150 pF to 1000 pF	6		30	1//	
SR(tr)	(see Figure 1)	$V_{CC} = 3.3 \text{ V}$ $C_L = 150 \text{ pF to } 2500 \text{ pF}$		$V_{CC} = 3.3 \text{ V}$ $C_L = 150 \text{ pF to } 2500 \text{ pF}$	4		30	V/μs

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

ESD PROTECTION

		TYP	UNIT
	Human-Body Model (HBM)	±15	
Driver outputs (DOUTx)	outputs (DOUTx) IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	

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All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25 ^{\circ}\text{C}$. Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

SLLS964-MARCH 2009 www.ti.com

RECEIVER SECTION

ELECTRICAL CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$	V _{CC} - 0.6	V _{CC} - 0.1		V
V_{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V	Decitive going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 5 V		1.8	2.4	V
V	No notice acioni in out through ald coltano	V _{CC} = 3.3 V	0.6	1.2		V
V _{IT} _	Negative-going input threshold voltage	V _{CC} = 5 V	0.8	1.5		V
V_{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

SWITCHING CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

	PARAMETER	TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C 450 pF	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	$C_L = 150 \text{ pF}$	300	ns
t _{sk(p)}	Pulse skew ⁽³⁾		300	ns

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V. (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. (3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

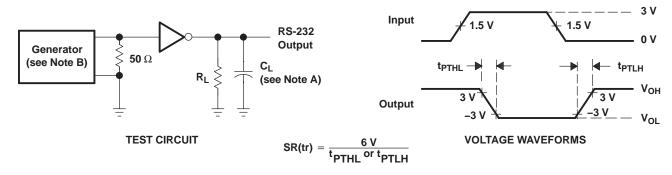
ESD PROTECTION

		TYP	UNIT
	Human-Body Model (HBM)	±15	
Receiver inputs (RINx)	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	

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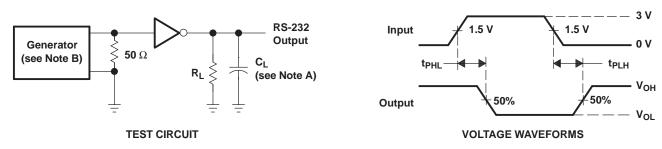
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_f \le 10$ ns.

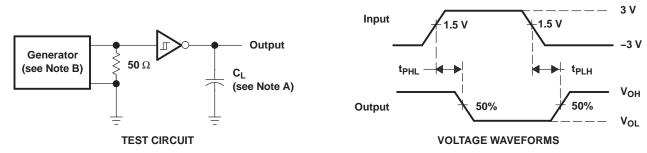
Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



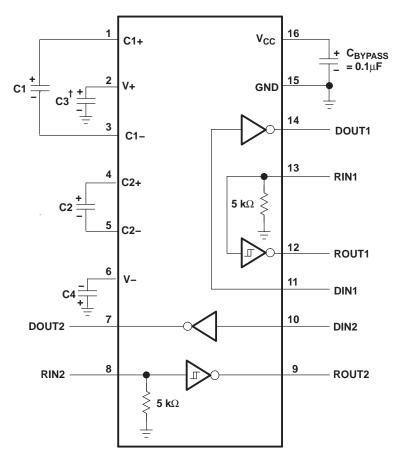
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50~\Omega$, 50% duty cycle, $t_f \le 10$ ns. $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

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APPLICATION INFORMATION



 $^{^{\}dagger}$ C3 can be connected to $V_{CC}\, or \, GND.$

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, C4	
$\begin{array}{c} \textbf{3.3 V} \pm \textbf{0.3 V} \\ \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{3 V to 5.5 V} \end{array}$	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF	

Figure 4. Typical Operating Circuit and Capacitor Values

PACKAGE OPTION ADDENDUM

www.ti.com 13-Apr-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Pa	ackage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TRS3232EQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TRS3232E-Q1:

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



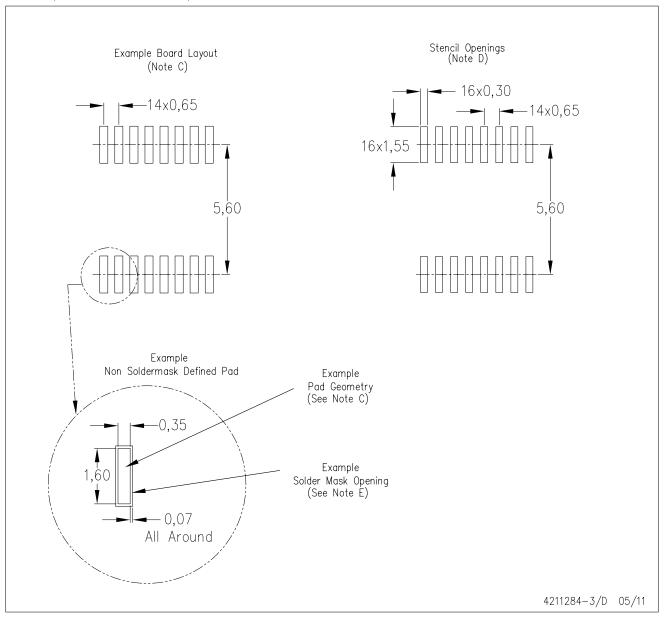
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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