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3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION

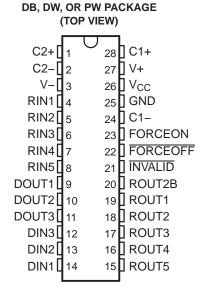
Check for Samples: TRS3243E

FEATURES

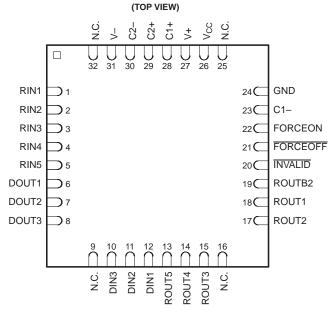
- Single-Chip and Single-Supply Interface for IBM™ PC/AT™ Serial Port
- **ESD Protection for RS-232 Bus Pins**
 - ±15-kV Human-Bodv Model (HBM)
 - ±8-kV IEC61000-4-2, Contact Discharge
 - ±15-kV IEC61000-4-2, Air-Gap Discharge
- Meets or Exceeds Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- **Always-Active Noninverting Receiver Output** (ROUT2B)
- Designed to Transmit at a Data Rate up to 500 kbit/s
- Low Standby Current . . . 1 µA Typ
- External Capacitors . . . 4 × 0.1 µF
- Accepts 5-V Logic Input With 3.3-V Supply
- **Designed to Be Interchangeable With Industry** Standard '3243E Devices
- **Serial-Mouse Driveability**
- **Auto-Powerdown Feature to Disable Driver** Outputs When No Valid RS-232 Signal Is Sensed
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- Laptops
- Palmtop PCs
- **Hand-Held Equipment**



QFN PACKAGE



N.C. - Not internally connected

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DESCRIPTION/ORDERING INFORMATION

The TRS3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 µs. INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 5 for receiver input levels.

The TRS3243EC is characterized for operation from 0°C to 70°C. The TRS3243EI is characterized for operation from –40°C to 85°C.

T _A	PAG	CKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DB	Reel of 2000	TRS3243ECDBR	TRS3243EC
000 +- 7000	SOP – DW	Reel of 2000	TRS3243ECDWR	TRS3243EC
0°C to 70°C	TSSOP - PW	Reel of 2000	TRS3243ECPWR	RS43EC
	QFN – RHB	Reel of 2000	TRS3243ECRHBR	RS43EC
	SSOP – DB	Reel of 2000	TRS3243EIDBR	TRS3243ECI
4000 1- 0500	SOP – DW	Reel of 2000	TRS3243EIDWR	TRS3243ECI
–40°C to 85°C	TSSOP - PW	Reel of 2000	TRS3243EIPWR	RS43EI
	QFN – RHB	Reel of 2000	TRS3243EIRHBR	RS43EI

Table 1. ORDERING INFORMATION

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



FUNCTION TABLES

Each Driver⁽¹⁾

		INPUTS		OUTPUT	
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	DRIVER STATUS
X	X	L	X	Z	Powered off
L	Н	Н	X	Н	Normal operation with
Н	Н	Н	X	L	auto-powerdown disabled
L	L	Н	Yes	Н	Normal operation with
Н	L	Н	Yes	L	auto-powerdown enabled
X	L	Н	No	Z	Powered off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

INP	UTS		OUTPUT	DECENTED STATUS
RIN	FORCEON	FORCEOFF	ROUT	RECEIVER STATUS
Х	Х	L	Z	Powered off
L	Х	Н	Н	
Н	Х	Н	L	Normal operation with auto-powerdown disabled/enabled
Open	Х	Н	Н	auto powerdown disabled/enabled

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

ROUT2B and Outputs INVALID (1)

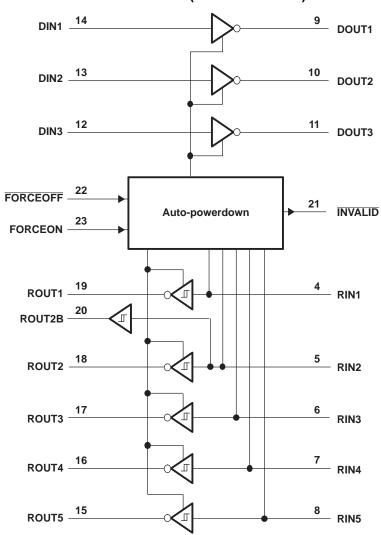
	INPUTS			OUTPUTS		
VALID RIN RS-232 LEVEL	RIN2	FORCEON	FORCEOFF	INVALID	ROUT2B	OUTPUT STATUS
Yes	L	X	X	Н	L	
Yes	Н	X	X	Н	Н	Alwaya active
Yes	Open	Х	Х	Н	L	Always active
No	Open	Х	Х	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

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LOGIC DIAGRAM (POSITIVE LOGIC)



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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽²⁾		-0.3	6	V
V+	Positive output supply voltage range (2)		-0.3	7	V
V-	Negative output supply voltage range ⁽²⁾	Negative output supply voltage range ⁽²⁾		-7	V
V+ - V-	Output supply voltage difference ⁽²⁾			13	V
	Leave to the management	Driver (FORCEOFF, FORCEON)	-0.3	6	
VI	Input voltage range	Receiver	-25	25	V
M	Output valtage vana	Driver	-13.2	25 13.2	V
Vo	Output voltage range	Receiver (INVALID)	-0.3	V _{CC} + 0.3	V
		DB package		62	
θ_{JA}	Package thermal impedance (3) (4)	DW package		46	°C/W
	PW package			62	
	Lead temperature 1,6 mm (1/16 in) from cas	e for 10 s		260	°C
T _{stg}	Storage temperature range		-65	150	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltages are with respect to network GND.

Recommended Operating Conditions⁽¹⁾

See Figure 6

				MIN	NOM	MAX	UNIT
	Cupply valtage		V _{CC} = 3.3 V	3	3.3	3.6	V
	Supply voltage		$V_{CC} = 5 V$	4.5	5	5.5	V
V	Driver and central high level input valtage	ontrol high-level input voltage DIN, FORCEOFF, FORCEON	$V_{CC} = 3.3 \text{ V}$	2			V
V _{IH}	Driver and control high-level input voltage		$V_{CC} = 5 V$	2.4			V
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON				0.8	V
V_{I}	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0		5.5	V
V_{I}	Receiver input voltage			-25		25	V
т			TRS3243EC	0		70	°C
T _A	Operating free-air temperature		TRS3243EI	-40		85	C

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PAR	AMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
II	Input leakage current	FORCEOFF, FORCEON			±0.01	±1	μΑ
		Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC}		0.3	1	mA
	Supply current	Powered off	No load, FORCEOFF at GND		1	10	
Icc	(T _A = 25°C)	Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded, All DIN are grounded		1	10	μΑ

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

The package thermal impedance is calculated in accordance with JESD 51-7.



DRIVER SECTION

Electrical Characteristics (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at $R_L = 3 \text{ k}\Omega$ to GND	5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at $R_L = 3 \text{ k}\Omega$ to GND	- 5	-5.4		V
Vo	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC} , 3- $k\Omega$ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5			V
I _{IH}	High-level input current	$V_I = V_{CC}$		±0.01	±1	μΑ
$I_{\rm IL}$	Low-level input current	V _I at GND		±0.01	±1	μΑ
V_{hys}	Input hysteresis				±1	V
	Short-circuit output current ⁽³⁾	$V_{CC} = 3.6 \text{ V}, \qquad V_{O} = 0 \text{ V}$			±60	A
Ios	Short-circuit output current	$V_{CC} = 5.5 \text{ V},$ $V_{O} = 0 \text{ V}$			±6U	mA
r _O	Output resistance	V_{CC} , V+, and V- = 0 V, $V_{O} = \pm 2 \text{ V}$	300	10M		Ω
I _{off}	Output leakage current	$\overline{\text{FORCEOFF}} = \text{GND}, \qquad \qquad \text{V}_{\text{O}} = \pm 12 \text{ V}, \qquad \text{V}_{\text{CC}} = 0 \text{ to } 5.5 \text{ V}$			±25	μΑ

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

Switching Characteristics(1)

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST	CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	C _L = 1000 pF, One DOUT switching,	$R_L = 3 \text{ k}\Omega$ See Figure 1	250	500		kbit/s
t _{sk(p)}	Pulse skew ⁽³⁾	$C_L = 150 \text{ pF to } 2500 \text{ pF},$	$R_L = 3 \text{ k}\Omega$ to 7 k Ω , See Figure 2		100		ns
	Slew rate, transition region	$V_{CC} = 3.3 \text{ V},$	C _L = 150 pF to 1000 pF	6		30	
SR(tr)	(see Figure 1)	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$ PRR = 250 kbit/s	C _L = 150 pF to 2500 pF	4		30	V/µs

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
	НВМ	±15	
Driver outputs (pins 9–11)	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	

All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25 ^{\circ}\text{C}$.

Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

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RECEIVER SECTION

Electrical Characteristics (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.6$	V _{CC} – 0.1		V
V_{OL}	Low-level output voltage	I _{OH} = 1.6 mA			0.4	V
\/	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 5 V		1.9	2.4	V
\/	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
V_{IT-}	Negative-going input threshold voltage	V _{CC} = 5 V	0.8	1.4		V
V_{hys}	Input hysteresis (V _{IT+} – V _{IT-})			0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	μΑ
ri	Input resistance	$V_I = \pm 3 \text{ V or } \pm 25 \text{ V}$	3	5	7	kΩ

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	150	ns
t _{PHL}	Propagation delay time, high- to low-level output		150	ns
t _{en}	Output enable time	C_L = 150 pF, R_L = 3 k Ω , See Figure 4	200	ns
t _{dis}	Output disable time		200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	50	ns

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
	НВМ	±15	
Driver outputs (pins 4–8)	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	

Product Folder Link(s): TRS3243E



AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{IT+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}		2.7	V
V _{IT-(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-2.7		V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-0.3	0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} - 0.6		V
V _{OL}	INVALID low-level output voltage	$I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

Switching Characteristics

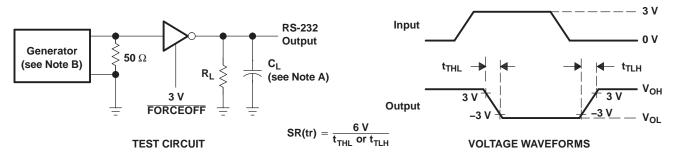
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t _{valid}	Propagation delay time, low- to high-level output	V _{CC} = 5 V	1	μs
t _{invalid}	Propagation delay time, high- to low-level output	V _{CC} = 5 V	30	μs
t _{en}	Supply enable time	V _{CC} = 5 V	100	μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.



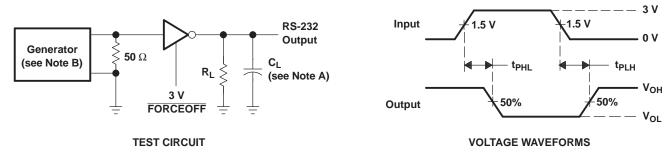
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50 \ \Omega$, 50% duty cycle, $t_r \le 10 \ ns$.

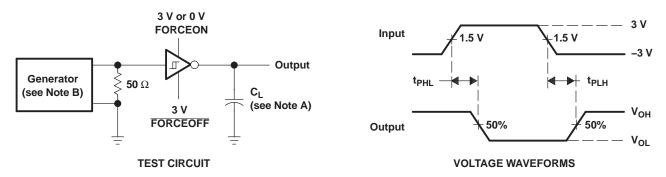
Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω , 50% duty cycle, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



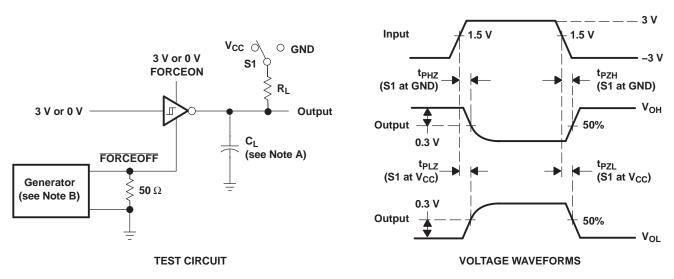
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω , 50% duty cycle, $t_r \le$ 10 ns, $t_f \le$ 10 ns.

Figure 3. Receiver Propagation Delay Times



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_f \le 10$ ns. $t_f \le 10$ ns.

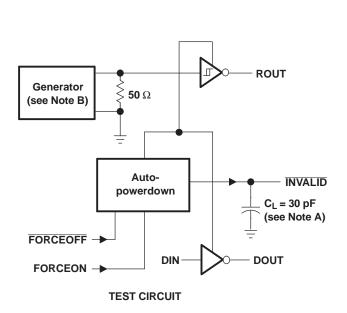
C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

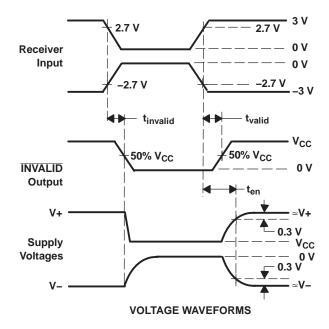
D. t_{PZL} and t_{PZH} are the same as t_{en}.

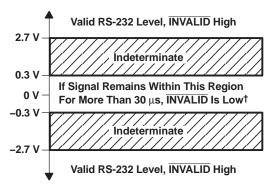
Figure 4. Receiver Enable and Disable Times



PARAMETER MEASUREMENT INFORMATION







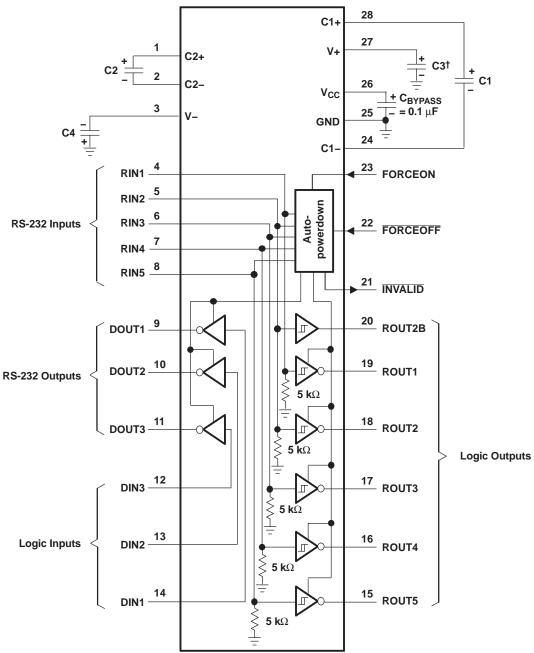
 $^{^{\}dagger}$ Auto-powerdown disables drivers and reduces supply current to 1 $\mu A.$

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns. $t_f \le 10$ ns.

Figure 5. INVALID Propagation Delay Times and Supply Enabling Time





 $^{^{\}dagger}$ C3 can be connected to $V_{CC}\, or \, GND.$

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4		
$\begin{array}{c} \textbf{3.3 V} \pm \textbf{0.3 V} \\ \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{3 V to 5.5 V} \end{array}$	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF		

Figure 6. Typical Operating Circuit and Capacitor Values



ESD Protection

TI TRS3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV in all states: normal operation, shutdown, and powered down. The TRS3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The TRS3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

- ±15-kV Human-Body Model (HBM)
- ±15-kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ±8-kV IEC61000-4-2, Contact Discharge

ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 7, while Figure 8 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k Ω resistor.

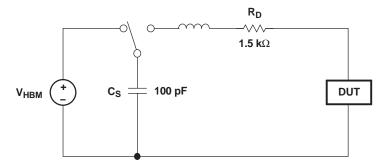


Figure 7. HBM ESD Test Circuit

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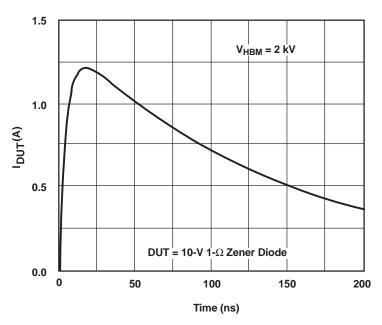


Figure 8. Typical HBM Current Waveform

IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The TRS3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

Figure 9 shows the IEC61000-4-2 model, and Figure 10 shows the current waveform for the corresponding ±8-kV contact-discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ±15-kV (Level 4) air-gap discharge test involves approaching the DUT with an already energized probe.

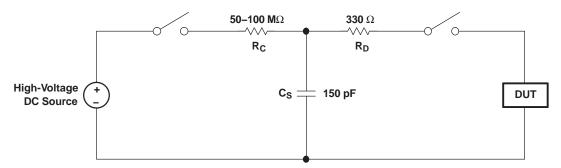


Figure 9. Simplified IEC61000-4-2 ESD Test Circuit



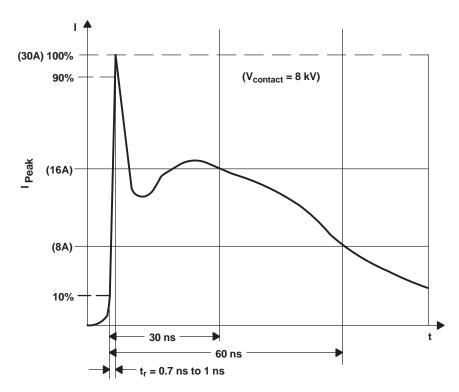


Figure 10. Typical Current Waveform of IEC61000-4-2 ESD Generator

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test is no longer as pertinent to the RS-232 pins.

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REVISION HISTORY

Changes from Revision B (July 2009) to Revision C					
•	Deleted "VALID RIN RS-232 LEVEL" from INPUTS.	3			
•	Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs.	3			
•	Added New Table "ROUT2B and INVALID Outputs" defining truth table for ROUT2B and INVALID outputs	3			

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TRS3243ECDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243ECRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TRS3243ECRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TRS3243EIDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TRS3243EIDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS3243EIRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TRS3243EIRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1
TRS3243ECRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRS3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1
TRS3243EIRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243ECDBR	SSOP	DB	28	2000	346.0	346.0	33.0
TRS3243ECDWR	SOIC	DW	28	1000	346.0	346.0	49.0
TRS3243ECPWR	TSSOP	PW	28	2000	346.0	346.0	33.0
TRS3243ECRHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TRS3243EIDBR	SSOP	DB	28	2000	346.0	346.0	33.0
TRS3243EIDWR	SOIC	DW	28	1000	346.0	346.0	49.0
TRS3243EIPWR	TSSOP	PW	28	2000	346.0	346.0	33.0
TRS3243EIRHBR	QFN	RHB	32	3000	346.0	346.0	29.0

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.



PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.



RHB (S-PVQFN-N32)

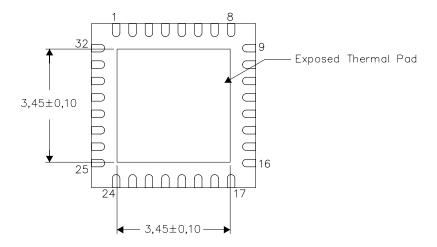
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

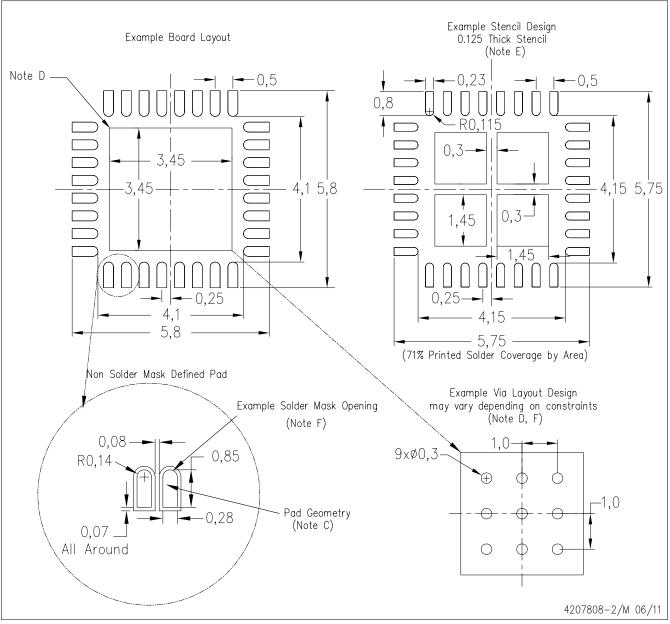
4206356-2/U 06/11

NOTE: A. All linear dimensions are in millimeters



RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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