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- Meets ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Supply Current
- Sleep Mode: 3-State Outputs in High-Impedance State Ultra-Low Supply Current . . . 17 μA Typ
- Improved Functional Replacement for: SN75188, Motorola MC1488, National Semiconductor DS14C88, and DS1488
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/µs
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . . ±4.5 V to ±15 V

description

The SN75C198 is a monolithic low-power BI-MOS device containing four low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI EIA/TIA-232-E. The drivers of the SN75C198 are similar to those of the SN75C188 quadruple driver. The drivers have a controlled-output slew rate that is limited to a maximum of 30 V/ μ s. This feature eliminates the need for external components.

The sleep-mode input, SM, can switch the outputs to high impedance, which avoids the transmission of corrupted data during power-up and allows significant system power savings during data-off periods.

The SN75C198 is characterized for operation from 0°C to 70°C.

I	NPUTS	OUTPUT	
SM	Α	В	Y
Н	Н	Н	L
н	L	Х	Н
Н	Х	L	Н
L	Х	Х	Z
H _ h	iah le		- low level

FUNCTION TABLE

H = high level, L = low level, X = irrelevant, Z = high impedance



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



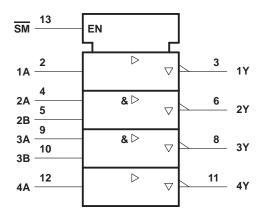
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D OR N PACKAGE (TOP VIEW)										
V _{CC} -	1	υ	14	V _{CC+}						
1A	2		13	SM						
1Y	3		12	4A						
2A	4		11	4Y						
2B	5		10	3B						
2Y	6		9	3A						
GND	7		8	3Y						

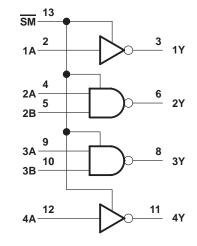
NOT RECOMMENDED FOR NEW DESIGNS

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logic symbol[†]

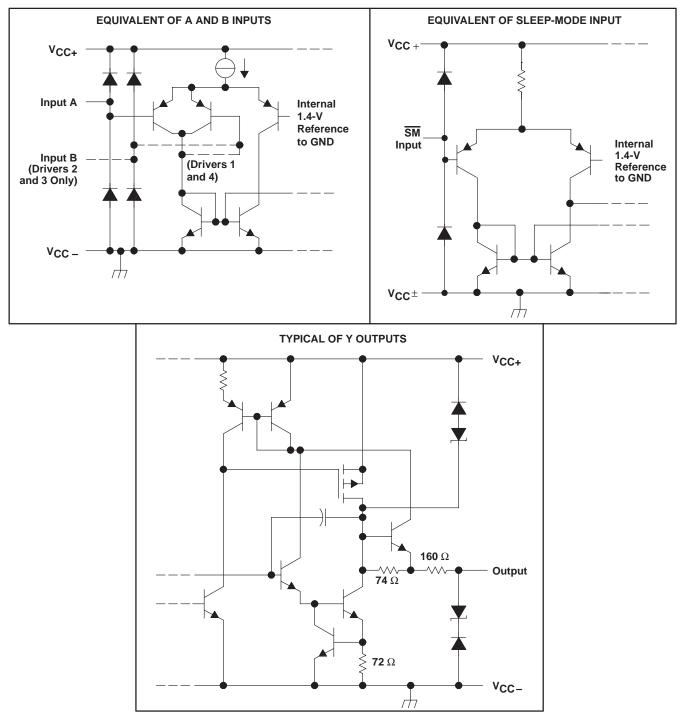


⁺ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. logic diagram (positive logic)





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schematics of inputs and outputs

All resistor values shown are nominal.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC+} (see Note 1)	
Supply voltage, V _{CC} _	
Input voltage range, V _I	
Output voltage range, VO	V_{CC-} –6 V to V _{CC+} + 6 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A : SN75C198	0°C to 70°C
Storage temperature range, T _{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE									
PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING						
D	950 mW	7.6 mW/°C	608 mW						
N	1150 mW	9.2 mW/°C	730 mW						

recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, V _{CC+}		4.5 12				
Supply voltage, V _{CC} _	Supply voltage, V _{CC} 4.5 -					
Input voltage, VI (see Figure 2)	V _{CC} -+	2	V _{CC+}	V		
High-level input voltage, VIH	I-level input voltage, VIH 2					
Low-level input voltage, VIL	A and B inputs			0.8	V	
Low-level input voltage, vIL	SM input			0.6	v	
Operating free-air temperature	0		70	°C		



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	PARAMETER	TEST CONDITI	ONS	MIN	TYP [†]	MAX	UNIT	
Val	High lovel output voltage	$V_{IH} = 0.8 V$, $R_L = 3 k\Omega$	$V_{CC\pm} = \pm 5 V$	4			V	
Vон	High-level output voltage	$V_{IH} = 0.8 \text{ V}, R_L = 3 \text{ k}\Omega$	$V_{CC\pm} = \pm 12 V$	10			v	
V _{OL}	Low-level output voltage (see Note 2)	$V_{IH} = 2 V$, $R_L = 3 k\Omega$	$V_{CC\pm} = \pm 5 V$			-4	V	
VOL	Low-level output voltage (see Note 2)	$V_{\text{H}} = 2 V, N_{\text{L}} = 3 N_{\text{S}2}$	$V_{CC\pm} = \pm 12 V$			-10	v	
IIН	High-level input current	V _I = 5 V				10	μΑ	
Ι _{ΙL}	Low-level input current	V _I = 0 V				-10	μΑ	
IOZ High-impeda	High impodonce state output ourrent		$V_{O} = 12 V,$ $V_{CC\pm} = \pm 12 V$	100				
	High-impedance-state output current	SM at 0.6 V	$V_{O} = -12 V,$ $V_{CC\pm} = \pm 12 V$			-100	μΑ	
IOS(H)	High-level short-circuit output current [‡]	$V_{I} = 0.8 V$, $V_{O} = 0 \text{ or } V_{CC-}$		-4.5	-10	-19.5	mA	
IOS(L)	Low-level short-circuit output current‡	$V_{I} = 2 V$, $V_{O} = 0 \text{ or } V_{CC}$	F	4.5	10	19.5	mA	
r _o	Output resistance	$V_{CC\pm} = 0$, $V_{O} = -2 V \text{ to } 2^{-1}$	V	300			Ω	
		A and B inputs at 0.8 V or 2 V,	$V_{CC\pm} = \pm 5 V$		90	160		
1	Supply surrent from Man	No load	$V_{CC\pm} = \pm 12 V$		95	160	μA	
ICC+	Supply current from V _{CC+}	A and B inputs at 0.8 V or 2 V,	$V_{CC\pm} = \pm 5 V$		40			
		$R_L = 3 k\Omega$, SM at 0.6 V	$V_{CC\pm} = \pm 12 V$		40			
		A and B inputs at 0.8 V or 2 V,	$V_{CC\pm} = \pm 5 V$		-90	-160		
100	Supply current from Voo	No load	$V_{CC\pm} = \pm 12 V$		-95	-160		
ICC-	Supply current from V _{CC} -	A and B inputs at 0.8 V or 2 V,	$V_{CC\pm} = \pm 5 V$		-40		μA	
		$R_L = 3 k\Omega$, SM at 0.6 V	$V_{CC\pm} = \pm 12 V$		-40			

<u>ele</u>ctrical characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12 V$, SM at 2 V (unless otherwise noted)

[†] All typical values are at $T_A = 25^{\circ}C$.

[‡] Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ± 12 V (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	UNIT
^t PLH	Propagation delay time, low- to high-level output \S					3	μs
^t PHL	Propagation delay time, high- to low-level output $\$$	$R_L = 3 k\Omega$ to 7 k Ω ,	C _L = 15 pF,			3.5	μs
^t TLH	Transition time, low- to high-level $\operatorname{output} \P$	See Figure 1		0.53	1	3.2	μs
^t THL	Transition time, high- to low-level $\operatorname{output} \P$			0.53	1	3.2	μs
tTLH	Transition time, low- to high-level output [#]	$R_L = 3 k\Omega$ to 7 k Ω ,	C _L = 2500 pF,		1.5		μs
^t THL	Transition time, high- to low-level output [#]	See Figure 2			1.5		μs
^t PZH	Output enable time to high level	$R_L = 3 k\Omega$ to 7 k Ω ,	CL = 15 pF,			50	μs
^t PHZ	Output disable time from high level	See Figure 3				10	μs
t _{PZL}	Output enable time to low level	$R_L = 3 k\Omega \text{ to } 7 k\Omega$,	C _L = 15 pF,			15	μs
t _{PLZ}	Output disable time from low level	See Figure 4	_			10	μs
SR	Output slew rate [#]	$R_L = 3 k\Omega$ to 7 k Ω ,	C _L = 15 pF	6	15	30	V/µs

[†] All typical values are at $T_A = 25^{\circ}C$.

§ tPHL and tPLH include the additional time due to on-chip slew rate and are measured at the 50% points.

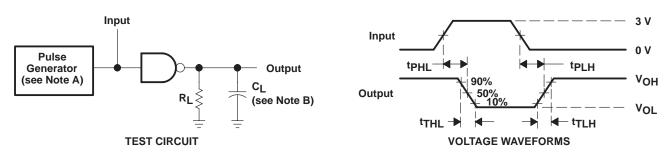
¶ Measured between 10% and 90% points of output waveform

Measured between 3-V and -3-V points of output waveform



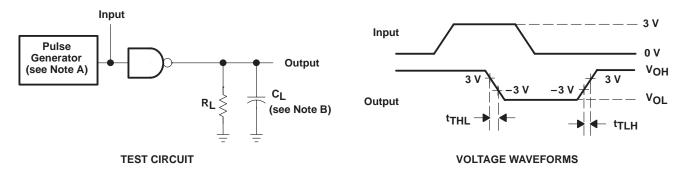
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PARAMETER MEASUREMENT INFORMATION



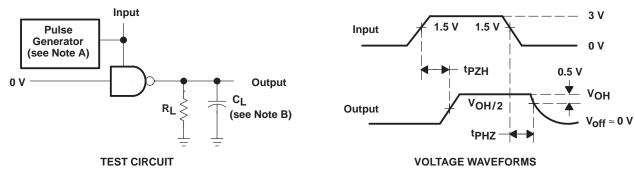
NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \ \mu$ s, PRR = 20 kHz, Z_O = 50 Ω , $t_T = t_f \le 50$ ns. B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \ \mu$ s, PRR = 20 kHz, $Z_O = 50 \ \Omega$, $t_f = t_f \le 50 \ ns$. B. CL includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms, Transition Times

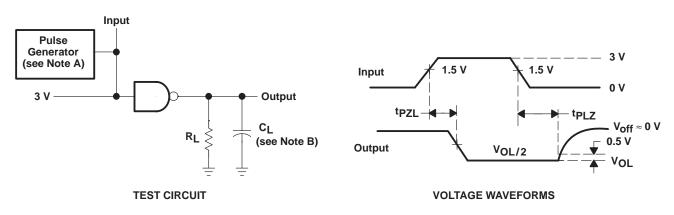


NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \ \mu$ s, PRR = 20 kHz, $Z_O = 50 \ \Omega$, $t_r = t_f \le 50 \ ns$. B. CL includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



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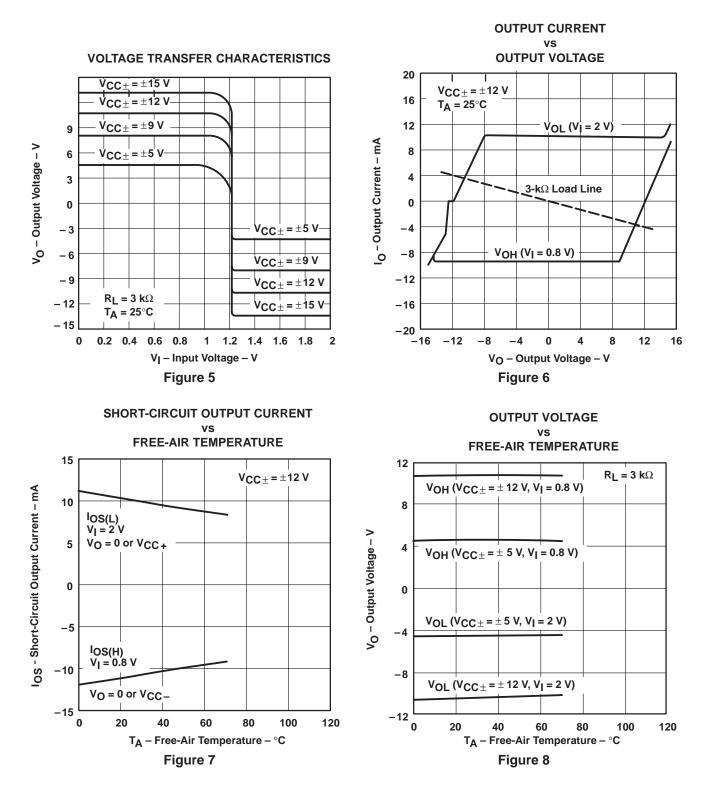
PARAMETER MEASUREMENT INFORMATION

NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \ \mu$ s, PRR = 20 kHz, $Z_O = 50 \ \Omega$, $t_r = t_f \le 50 \ ns$. B. CL includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

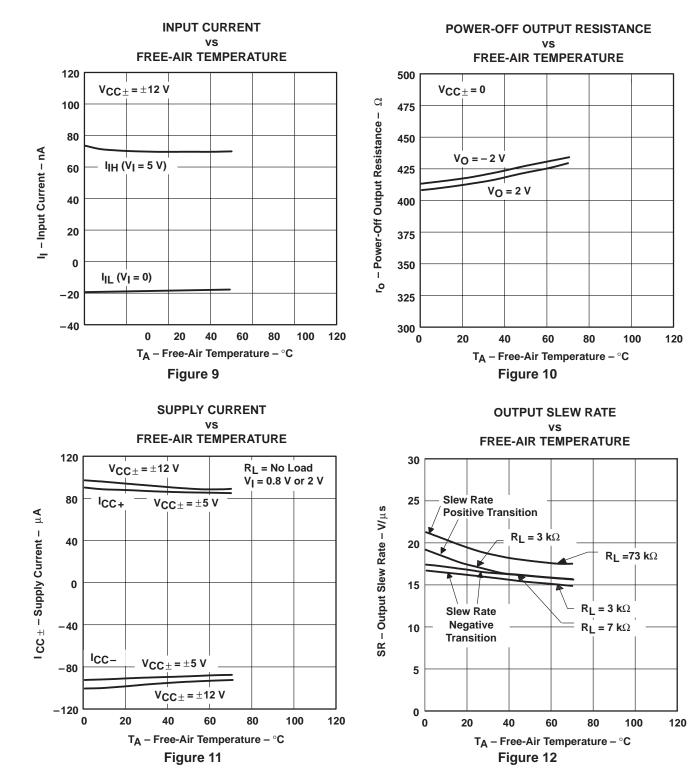


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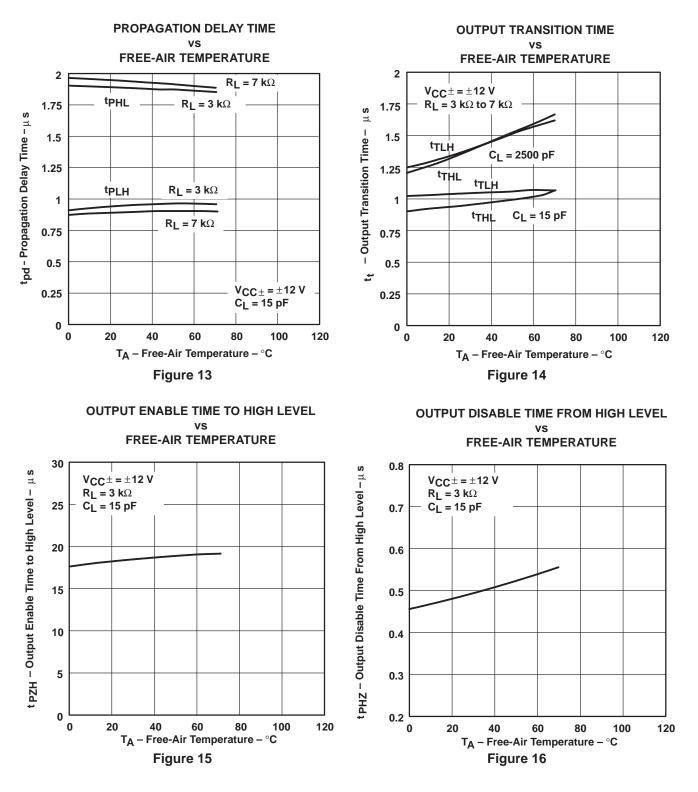


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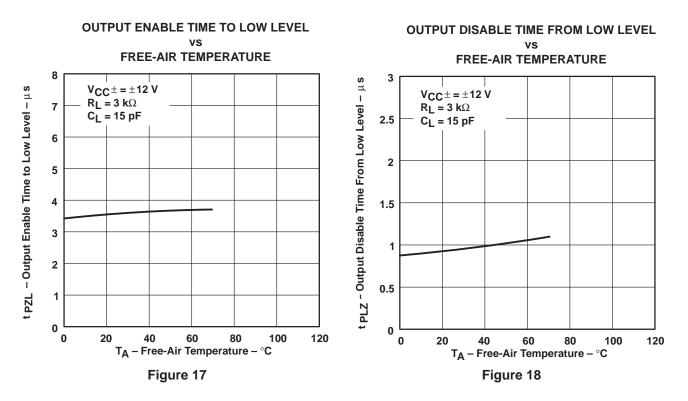


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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75C198D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C198NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

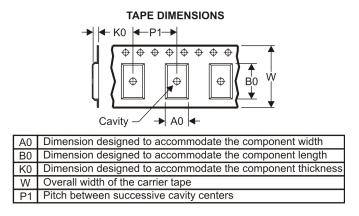
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C198DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C198DR	SOIC	D	14	2500	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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