

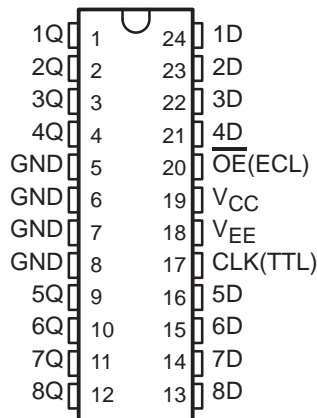
# SN10KHT5578

## OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE

SDZS014A – APRIL 1990 – REVISED JANUARY 1999

- 10KH Compatible
- TTL Clock and ECL Control Inputs
- Noninverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin  $V_{CC}$ ,  $V_{EE}$ , and GND Configurations Minimize High-Speed Switching Noise
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Package Options Include Plastic Small-Outline (DW) Package and Standard Plastic (NT) DIPs

DW OR NT PACKAGE  
(TOP VIEW)



### description

This octal TTL-to-ECL translator is designed to provide efficient translation between a TTL signal environment and a 10KH ECL signal environment. This device is designed specifically to improve the performance and density of TTL-to-ECL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the '5578 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

The output-control input  $\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5578 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

INPUTS			OUTPUT (ECL) Q
$\overline{OE}$	CLK	D	
L	↑	L	L
L	↑	H	H
L	L	X	$Q_0$
H	X	X	L



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

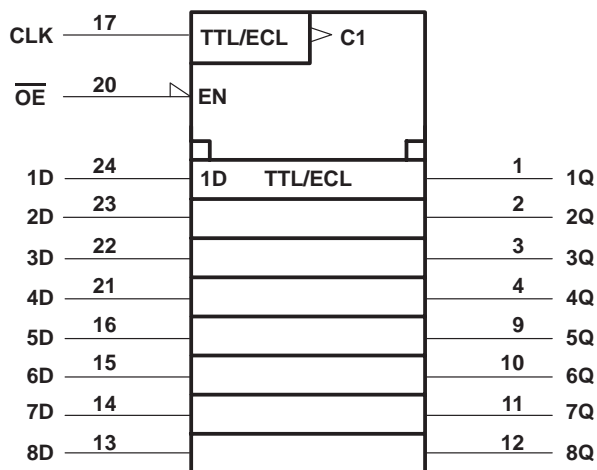
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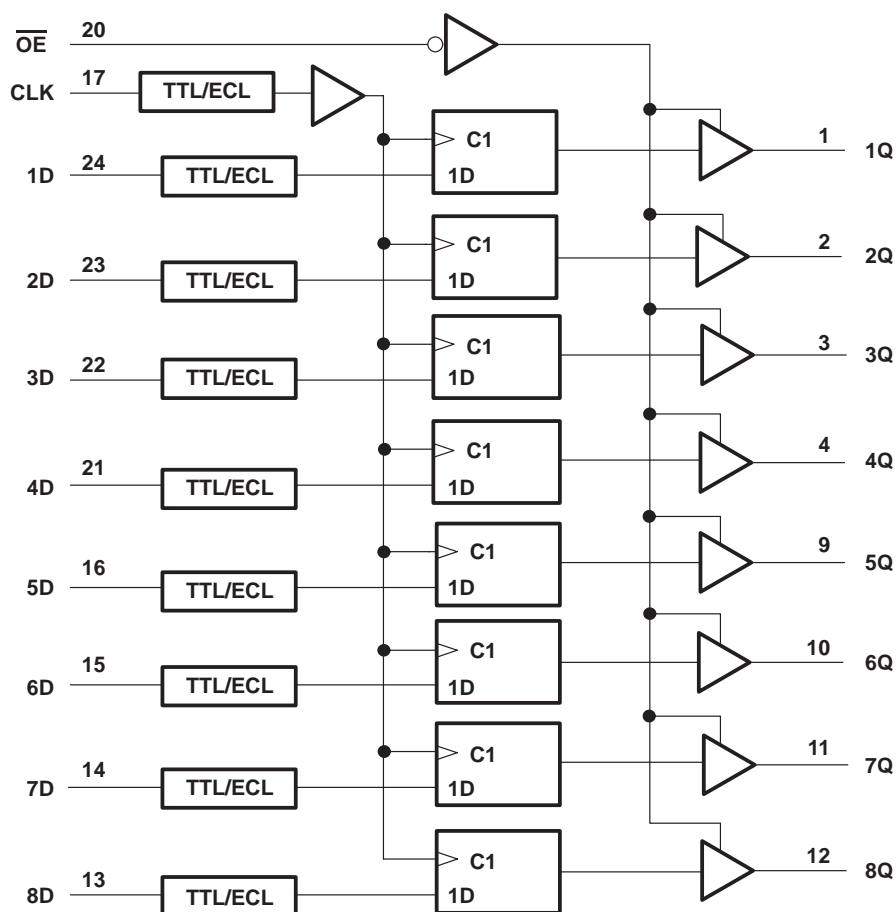
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



**SN10KHT5578**  
**OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE**  
**EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE**

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**absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Supply voltage range, $V_{EE}$ .....	–8 V to 0 V	
Input voltage range (TTL) (see Note 1) .....	–1.2 V to 7 V	
Input voltage range (ECL) .....	$V_{EE}$ to 0 V	
Input current range (TTL) .....	–30 mA to 5 mA	
Current out of any output .....	50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DW package .....	81°C/W
	NT package .....	67°C/W
Storage temperature range .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The TTL input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT	
$V_{CC}$	TTL supply voltage	4.5	5	5.5	V	
$V_{EE}$	ECL supply voltage	–4.94	–5.2	–5.46	V	
$V_{IH}$	TTL high-level input voltage	2			V	
$V_{IH}$	ECL high-level input voltage‡	0°C		–1170	–840	mV
		25°C		–1130	–810	mV
		75°C		–1070	–735	mV
$V_{IL}$	TTL low-level input voltage	0.8			V	
$V_{IL}$	ECL low-level input voltage‡	0°C		–1950	–1480	mV
		25°C		–1950	–1480	mV
		75°C		–1950	–1450	mV
$I_{IK}$	TTL input clamp current	–18			mA	
$T_A$	Operating ambient temperature (see Note 3)	0			75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

NOTE 3: Each 10KH-series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse airflow greater than 500 linear ft/min is maintained.



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**electrical characteristics over recommended operating ambient temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{IK}$	CLK and D inputs	$V_{CC} = 4.5\text{ V}$ ,	$V_{EE} = -4.94\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_I$	CLK and D inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	CLK and D inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
	$\overline{\text{OE}}$ input	$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = -840\text{ mV}$	0°C		350	
		$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = -810\text{ mV}$	25°C		350	
		$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = -735\text{ mV}$	75°C		350	
$I_{IL}$	CLK and D inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.5	mA
	$\overline{\text{OE}}$ input	$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$ ,	$V_I = -1950\text{ mV}$	0°C		0.5	$\mu\text{A}$
					25°C		0.5	
					75°C		0.5	
$V_{OH}^\ddagger$		$V_{CC} = 4.5\text{ V}$ ,	$V_{EE} = -5.2\text{ V} \pm 5\%$ ,	See Note 4	0°C	-1020	-840	mV
					25°C	-980	-810	
					75°C	-920	-735	
$V_{OL}^\ddagger$		$V_{CC} = 4.5\text{ V}$ ,	$V_{EE} = -5.2\text{ V} \pm 5\%$ ,	See Note 4	0°C	-1950	-1630	mV
					25°C	-1950	-1630	
					75°C	-1950	-1600	
$I_{CCH}$		$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$			17.5	25	mA
$I_{CCL}$		$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$			15	22	mA
$I_{EE}$		$V_{CC} = 5.5\text{ V}$ ,	$V_{EE} = -5.46\text{ V}$			-104	-149	mA
$C_i$		$V_{CC} = 5\text{ V}$ ,	$V_{EE} = -5.2\text{ V}$ ,	$f = 10\text{ MHz}$			4	pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $V_{EE} = -5.2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

NOTE 4: Outputs are terminated through a 50-Ω resistor to -2 V.

**timing requirements over recommended operating conditions**

		MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency		180	MHz
$t_w$	Pulse duration, CLK	High	4	ns
		Low	4	
$t_{su}$	Setup time, data before CLK↑	High	1.5	ns
		Low	2.5	
$t_h$	Hold time, data after CLK↑	High	1	ns
		Low	1	

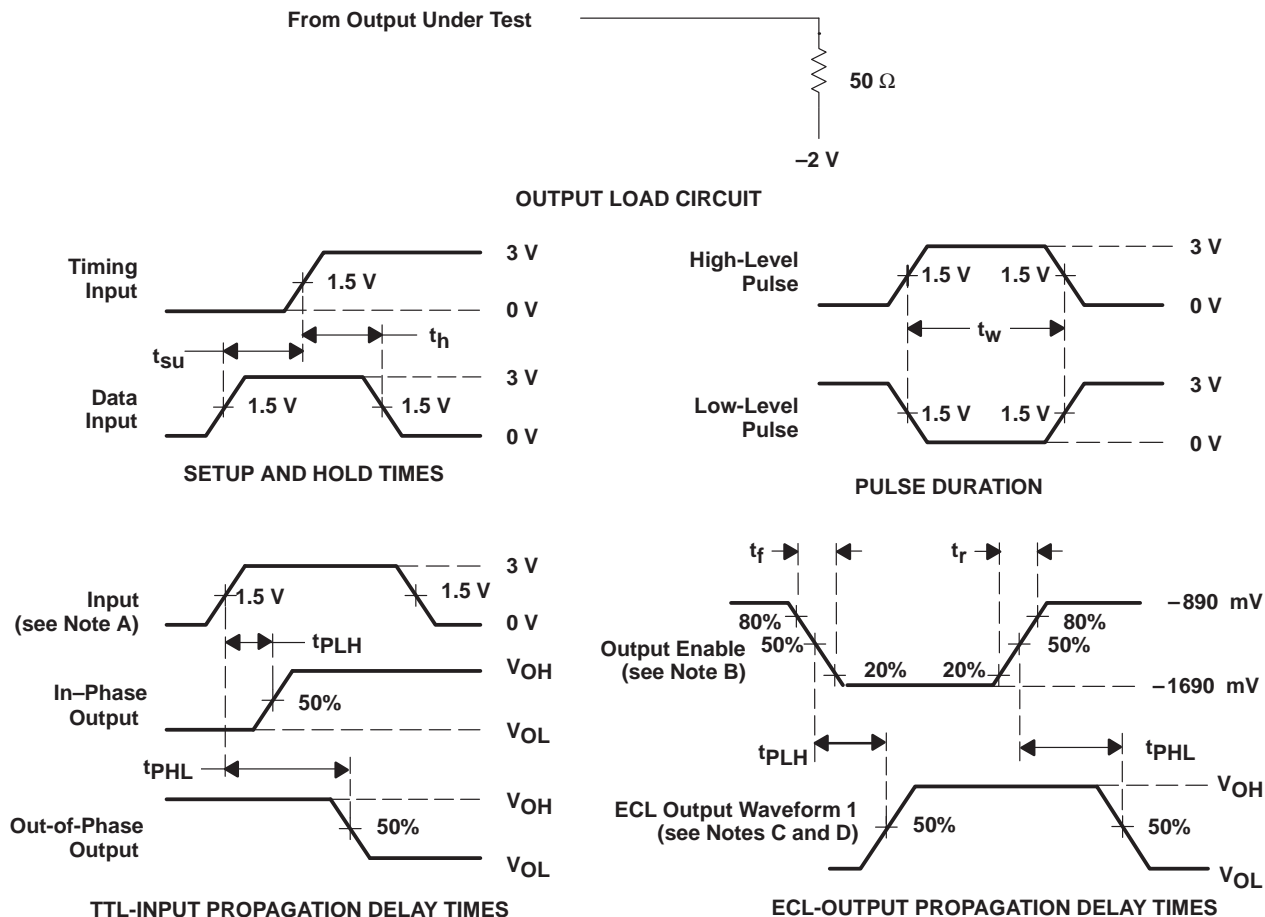
**switching characteristics over recommended ranges of supply voltage and operating ambient temperature (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$f_{\text{max}}$			180			MHz
$t_{PLH}$	CLK	Q	0.8	2.2	4	ns
$t_{PHL}$			0.8	2.1	3.8	
$t_{PLH}$	OE	Q	0.5	1.4	3.2	ns
$t_{PHL}$			0.5	1.7	3.3	
$t_r$		Y		1.5		ns
$t_f$		Y		1.5		ns

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $V_{EE} = -5.2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 2.5 \text{ ns}$ ,  $t_f = 2.5 \text{ ns}$ .  
 B. For ECL inputs, input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 1.5 \text{ ns}$ ,  $t_f = 1.5 \text{ ns}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by  $\overline{OE}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN10KHT5578DW	NRND	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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