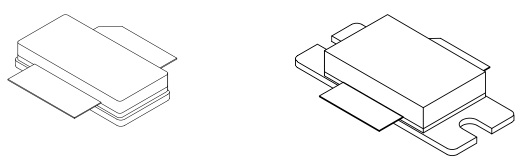
agere systems

Preliminary Data Sheet
April 2004

AGR09130E
130 W, 921 MHz—960 MHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR09130E is a high-voltage, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for cellular band, code division multiple access (CDMA), global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and time division multiple access (TDMA) single and multicarrier class AB wireless base station amplifier applications. This device is manufactured on an advanced LDMOS technology offering state-of-the-art performance, and reliability. Packaged in an industry-standard package incorporating internal matching and capable of delivering a minimum output power of 130 W, it is ideally suited for today's RF power amplifier applications.



AGR09130EU (unflanged) **AGR09130EF (flanged)**

Figure 1. Available Packages

Features

- Typical performance ratings are for the EDGE format: 3GPP GSM 05.05:
  - — Output power (P_{OUT}): 50 W.
  - — Power gain: 17.8 dB.
  - — Modulation spectrum:
    @ ±400 kHz = –60 dBc.
    @ ±600 kHz = –72 dBc.
  - — Error vector magnitude (EVM) = 1.8%.
  - — Return loss: –10 dB.
- High-reliability, gold-metalization process.
- Internally matched.
- High gain, efficiency, and linearity.
- Integrated ESD protection.
- Si LDMOS.
- Industry-standard packages.
- P1dB of 130 W minimum output power.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case: AGR09130EU	$R_{\theta JC}$	0.5	°C/W
AGR09130EF		0.5	

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Drain Current—Continuous	I_D	15	Adc
Total Dissipation at T_C = 25 °C: AGR09130EU	P_D	350	W
AGR09130EF		350	
Derate Above 25 °C: AGR09130EU		2.0	W/°C
AGR09130EF		2.0	
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR09130E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

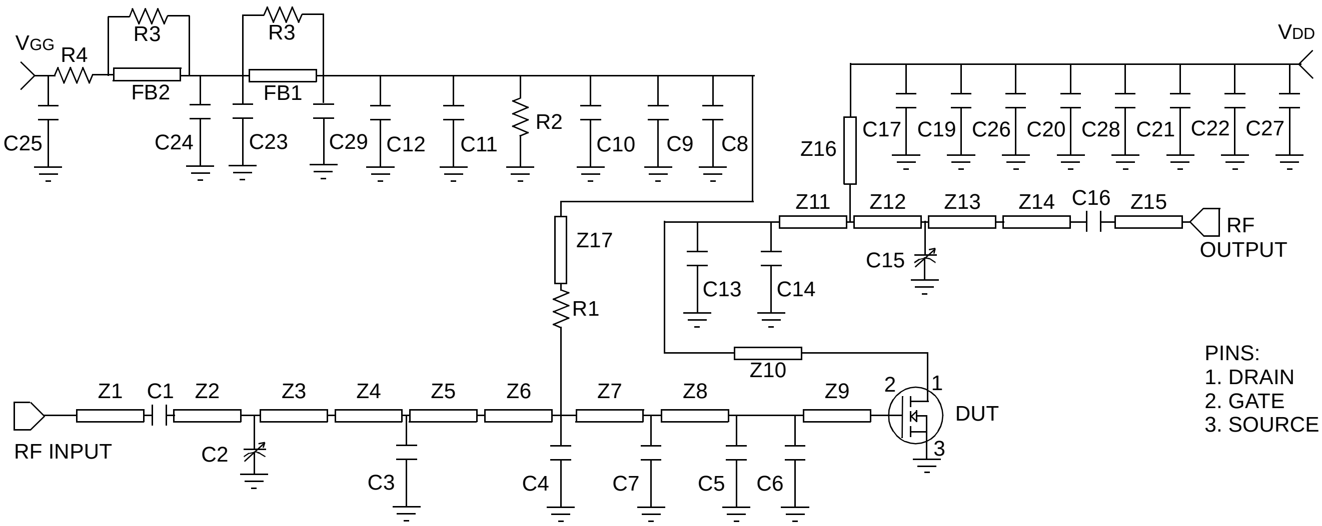
Table 4. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 200 µA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	4	µAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	12	µAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	9	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 400 µA)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 26 V, I_{DQ} = 1000 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

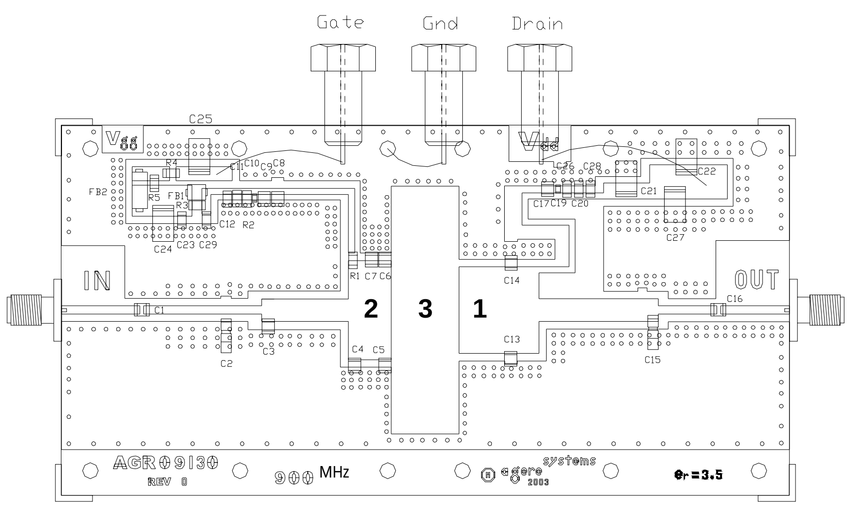
Table 5. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Output Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{OSS}	—	72	—	pF
Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{RSS}	—	3.0	—	pF
Functional Tests (in Agere Systems Supplied Test Fixture) (Test frequencies (f) = 920 MHz, 940 MHz, 960 MHz)					
Linear Power Gain (V_{DS} = 26 V, P_{OUT} = 50 W, I_{DQ} = 1000 mA)	G_L	16	18	—	dB
Output Power (V_{DS} = 26 V, 1 dB compression, I_{DQ} = 1000 mA)	P1dB	130	150	—	W
Drain Efficiency (V_{DS} = 26 V, P_{OUT} = P1dB, I_{DQ} = 1000 mA)	η	—	55	—	%
Third-order Intermodulation Distortion (100 kHz spacing, V_{DS} = 26 V, P_{OUT} = 120 WPEP, I_{DQ} = 1000 mA)	IM3	—	30	—	dBc
Input VSWR	$VSWR_I$	—	2:1	—	—
Ruggedness (V_{DS} = 26 V, P_{OUT} = 130 W, I_{DQ} = 1000 mA, f = 940 MHz, VSWR = 5:1, all angles)	—	No degradation in output power.			

Test Circuit Illustrations for AGR09130E



A. Schematic



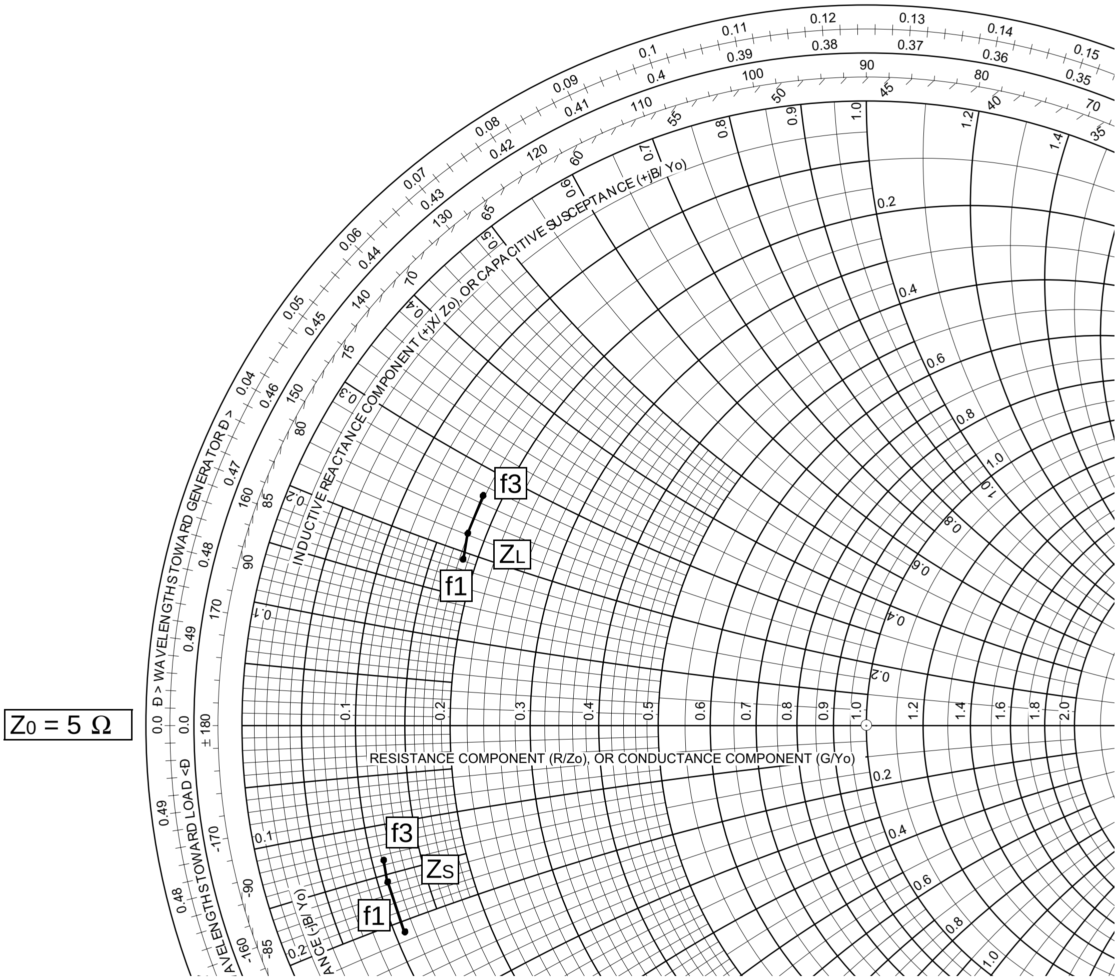
Parts List:

- Microstrip line:
  Z1 0.834 in. x 0.066 in.; Z2 0.066 in. x 0.066 in.; Z3 0.290 in. x 0.066 in.; Z4 0.050 in. x 0.180 in.; Z5 0.650 in. x 0.180 in.; Z6 0.050 in. x 0.800 in.; Z7 0.132 in. x 0.800 in.; Z8 0.105 in. x 0.800 in.; Z9 0.050 in. x 0.800 in.; Z10 0.423 in. x 0.700 in.; Z11 0.227 in. x 0.700 in.; Z12 0.920 in. x 0.180 in.; Z13 0.040 in. x 0.180 in.; Z14 0.470 in. x 0.066 in.; Z15 0.495 in. x 0.066 in.; Z16 1.340 in. x 0.050 in.: Z17 1.100 in. x 0.050 in.
- *ATC*® chip capacitor:
  C1, C8, C16, C17: 47 pF 100B470JW; C3 1.5 pF 100B1R5BW; C4: 6.8 pF 100B6R8BW; C13, C14: 12 pF 100B120JW; C5, C6, 10 pF 100B100JW; C7 5.6 pF 100B5R6BW; C9: 100 pF 100B101JW.
- 0603 chip capacitor: C10, C19: 220 pF.
- *Kemet*®: chip capacitor, C11, C26: 0.01 µF C1206C103KRAC7800; C12, C20, C23, C28, C29: 0.1 µF C1206C104KRAC7800.
- *Johanson Giga-Trim*® variable capacitor, 27291SL: C2, C15: 0.8 pF to 8 pF.
- *Sprague*® tantalum chip capacitor (35 V): C21, C24, C25, C27 10 µF; C22 22 µF.
- 1206 size fixed film chip resistor (0.25 W): R1: 51 Ω RM73B2B510J; R2 56 kΩ RM73B2B563J; R3 12 Ω RM73B2B120J; R4 1.2 kΩ RM73B2B122J; R5 RM73B2B4R3J 4.3 Ω.
- *Kreger*® ferrite bead: FB1 2743019447; FB2 2743021447.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, ε_r = 3.5.

B. Component Layout

Figure 2. AGR09130E Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
920 (f1)	0.55 – j1.06	0.9 + j0.96
940	0.55 – j0.77	0.89 + j1.09
960 (f3)	0.58 – j0.66	0.84 + j1.35

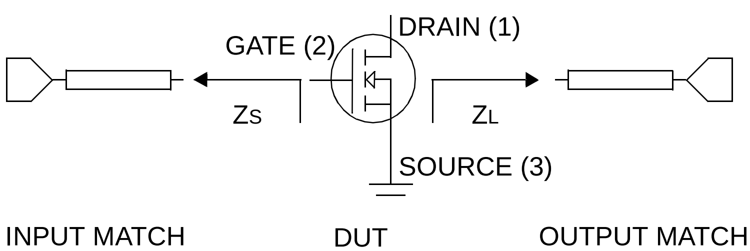
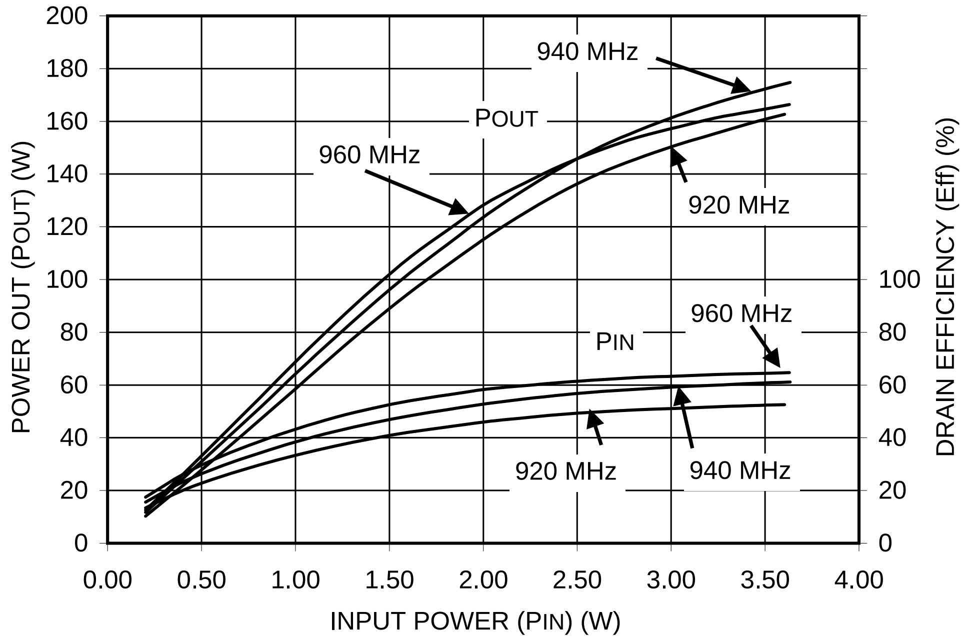


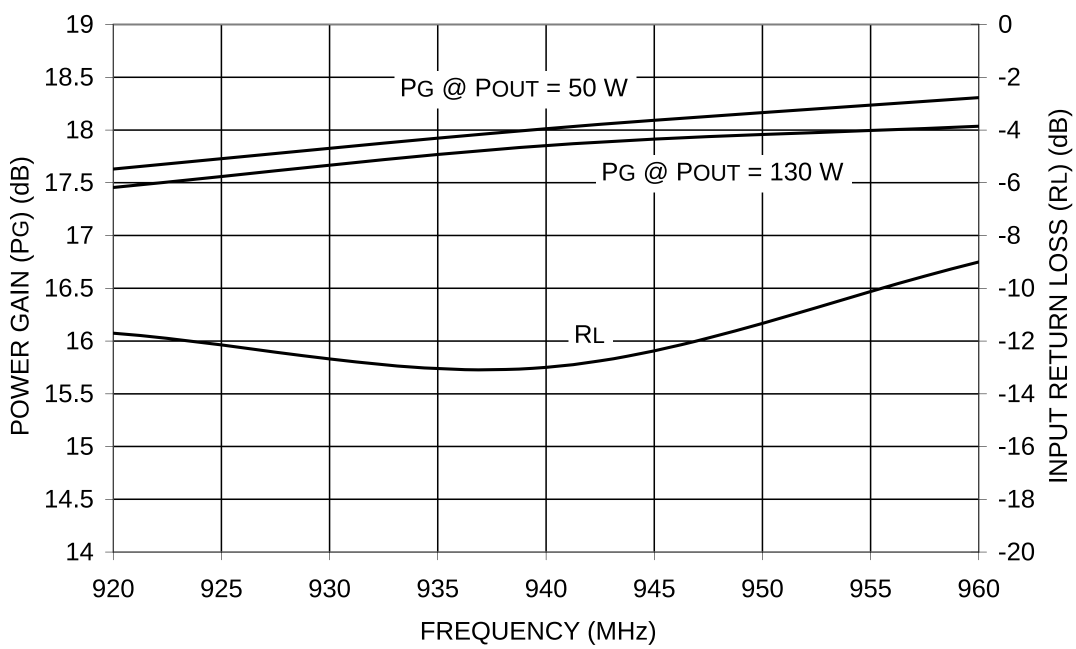
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, T_F = 30 °C, FORMAT = CW.

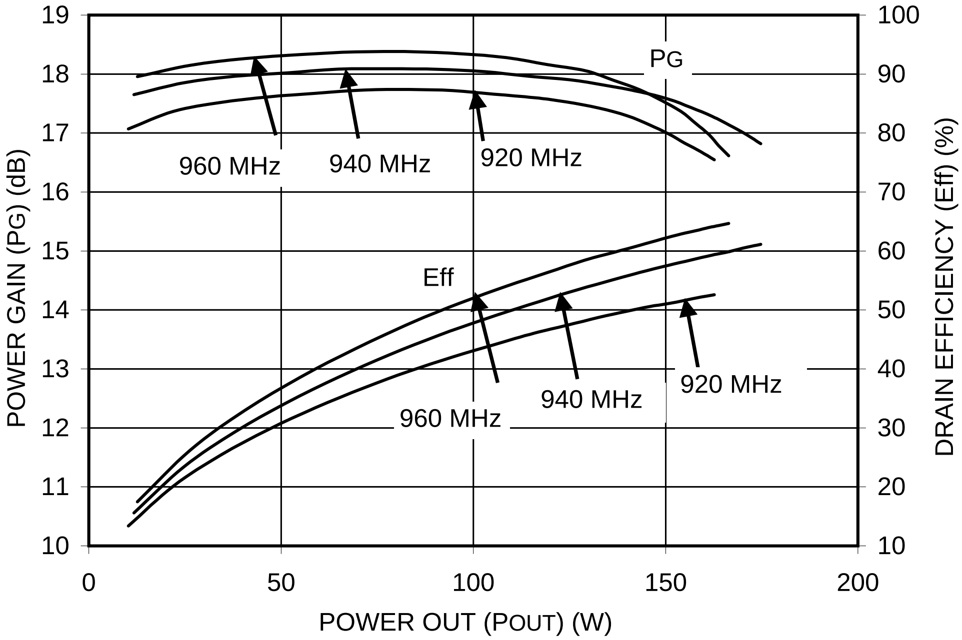
Figure 4. POUT and Drain Efficiency vs. PIN



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, T_F = 30 °C.

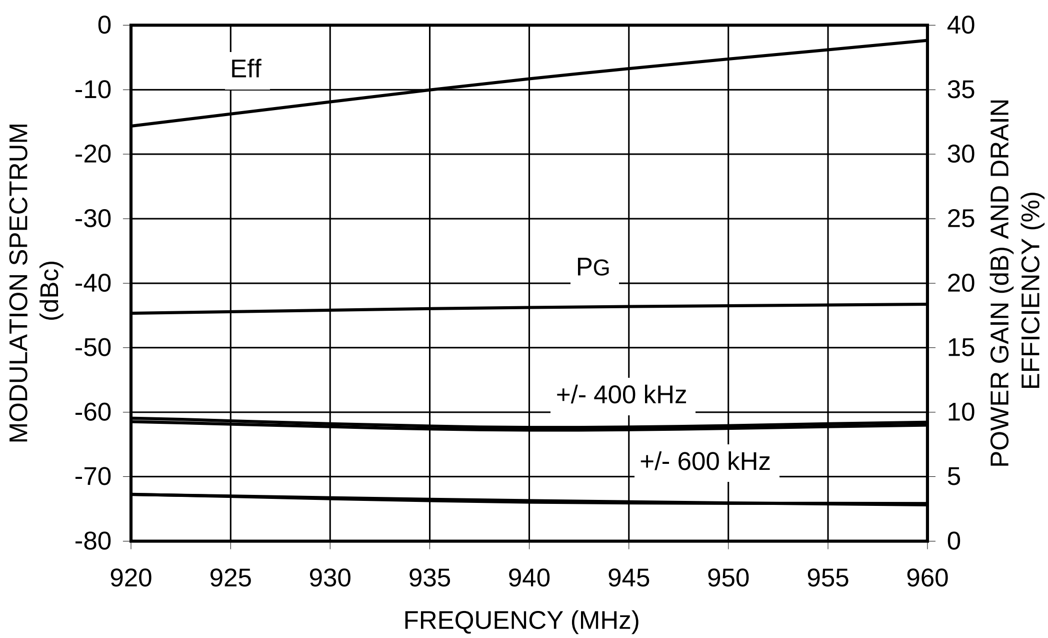
Figure 5. Power Gain and Return Loss vs. Frequency

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, T_F = 30 °C, FORMAT = CW.

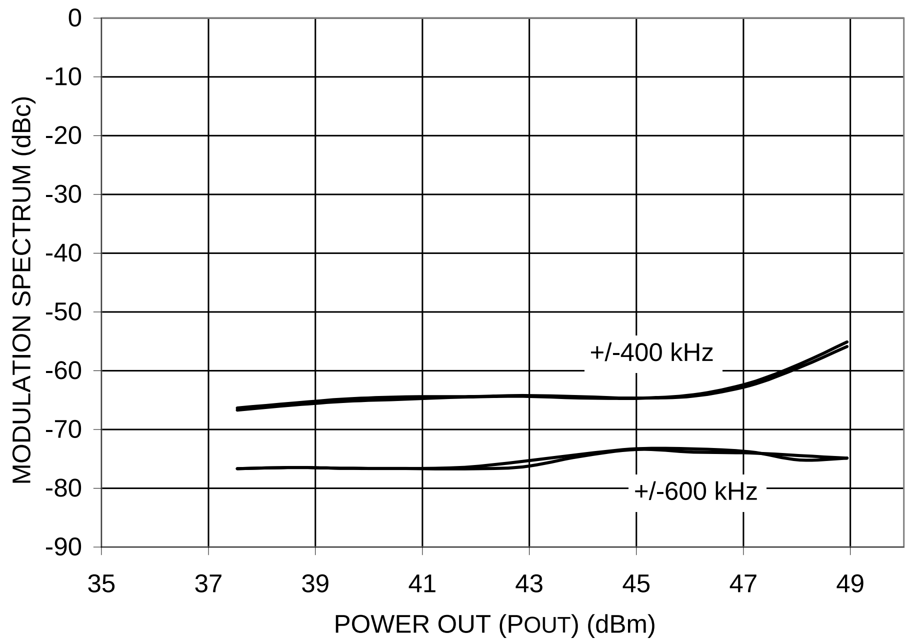
Figure 6. Power Gain and Drain Efficiency vs. Power Out



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, P_O = 50 W, T_F = 30 °C, EDGE FORMAT = 3GPP GSM 05.05.

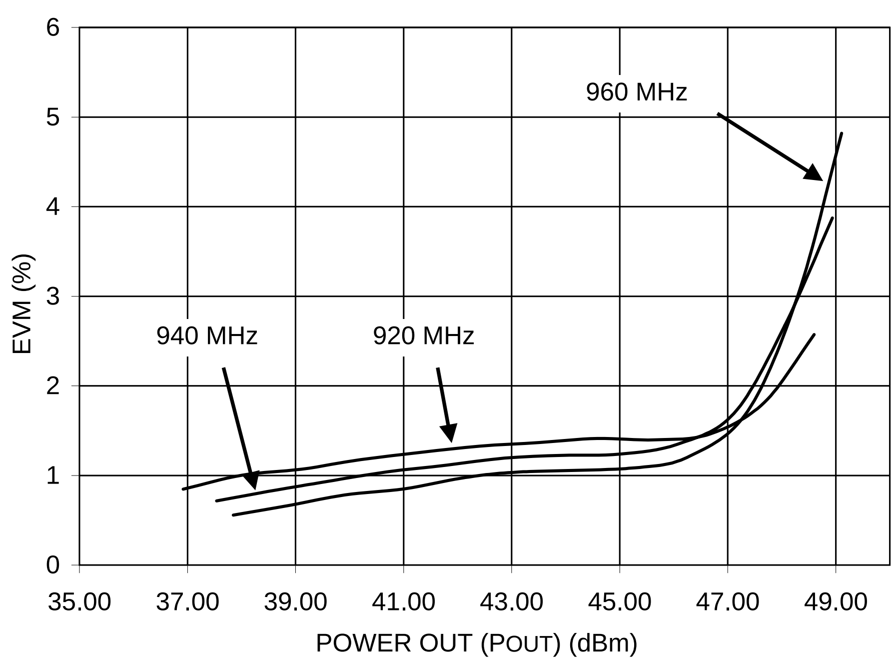
Figure 7. ACP, Power Gain, and Efficiency vs. Frequency

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, T_F = 30 °C, FREQUENCY = 940 MHz, EDGE FORMAT = 3GPP GSM 05.05.

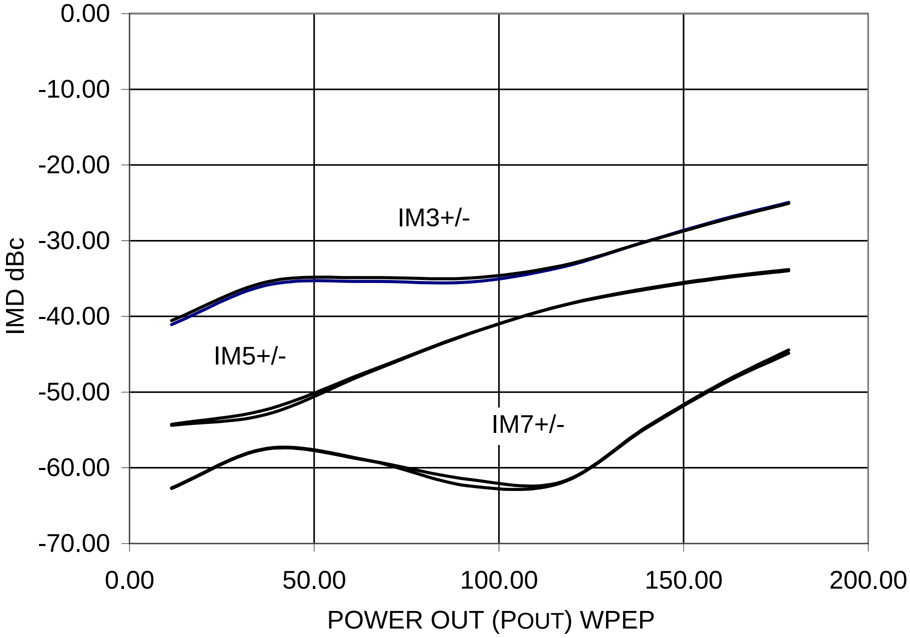
Figure 8. EDGE Modulation Spectrum vs. Power Out



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, T_F = 30 °C, EDGE FORMAT = 3GPP GSM 05.05.

Figure 9. EVM vs. Power Out

Typical Performance Characteristics (continued)



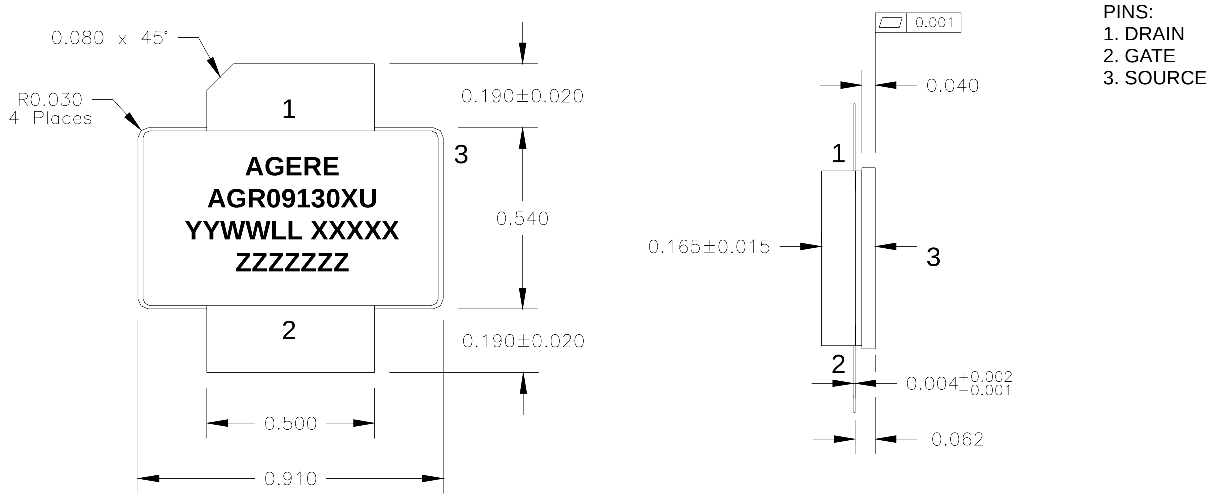
TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 1.0 A, T_F = 30 °C, F1 = 940.0 MHz, F2 = 940.1 MHz.

Figure 10. 2-Tone IMD vs. Po

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR09130EU



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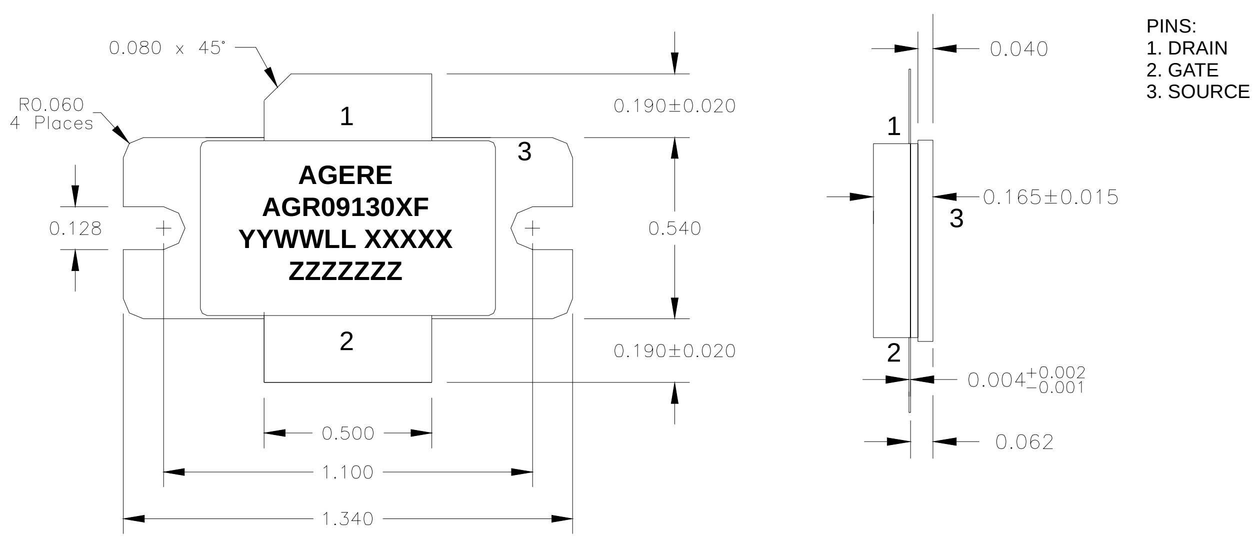

Label Notes:
- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.

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