SLOS241B - AUGUST 1999 - REVISED MARCH 2000

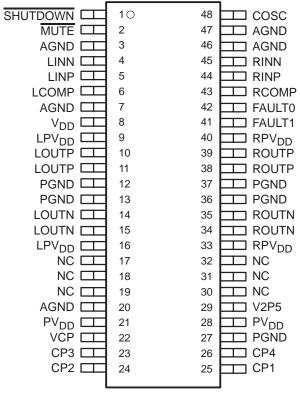
NOT RECOMMENDED FOR NEW DESIGNS

- Choose TPA2000D2 For Upgrade
- **Extremely Efficient Class-D Stereo** Operation
- **Drives L and R Channels**
- 2-W BTL Output Into 4 Ω
- 5-W Peak Music Power
- **Fully Specified for 5-V Operation**
- **Low Quiescent Current**
- Shutdown Control . . . 0.2 µA
- Thermally-Enhanced PowerPAD™ Surface-**Mount Packaging**
- Thermal, Over-Current, and Under-Voltage **Protection**

description

The TPA005D12 is a monolithic power IC stereo audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA005D12 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 2 W of continuous average power into a 4- Ω load at 0.5% THD+N from a 5-V power supply in the high-fidelity audio

DCA PACKAGE (TOP VIEW)



NC - No internal connection

frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control is provided to limit total quiescent current to 0.2 μA, making the device ideal for battery-powered applications.

A full range of protection circuitry is included to increase device reliability: thermal, over-current, and under-voltage shutdown, with two status feedback terminals for use when any error condition is encountered.

The high switching frequency of the TPA005D12 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA005D12 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

AVAILABLE OPTIONS

	PACKAGED DEVICES
TA	TSSOP† (DCA)
1000 / 10500	` '
−40°C to 125°C	TPA005D12DCA

 $[\]dagger$ The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA005D12DCAR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

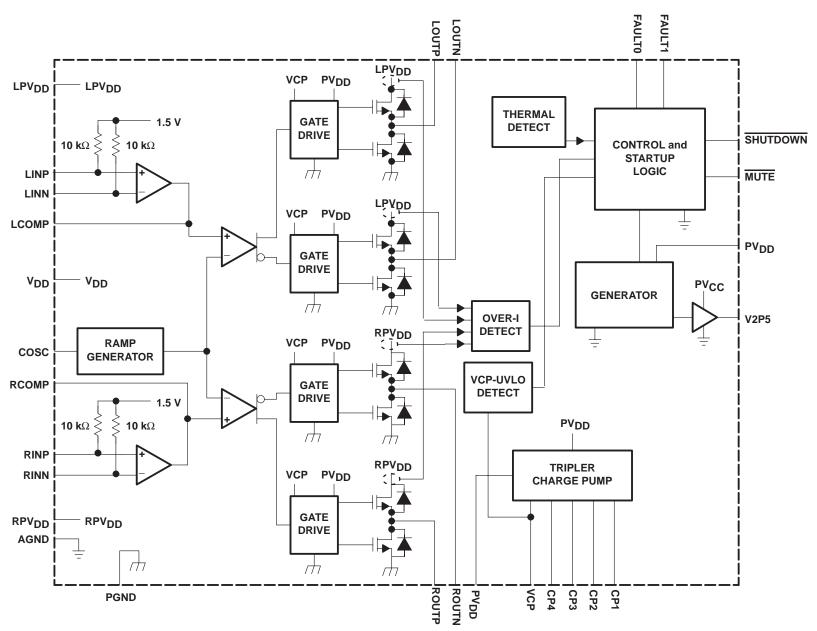
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STRUMENTS

lemplate

Release Date: 7-11-94





NOTE A: LPVDD, RPVDD, VDD, and PVDD are externally connected. AGND and PGND are externally connected.

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Terminal Functions

TERMINAL								
NAME NO.		DESCRIPTION						
AGND	3, 7, 20, 46, 47	Analog ground for headphone and Class-D analog sections						
cosc	48	Capacitor I/O for ramp generator. Adjust the capacitor size to change the switching frequency.						
CP1	25	First diode node for charge pump						
CP2	24	First inverter switching node for charge pump						
CP3	23	Second diode node for charge pump						
CP4	26	Second inverter switching node for charge pump						
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.						
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.						
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier						
LINN	4	Class-D left-channel negative input						
LINP	5	Class-D left-channel positive input						
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge						
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge						
LPV _{DD}	9, 16	Class-D amplifier left-channel power supply						
MUTE	2	Active-low logic-level mute input signal. When MUTE is held low, the selected amplifier is muted. When MUTE is held high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.						
NC	17, 18, 19, 30, 31, 32	No connection						
PGND	12, 13	Power ground for left-channel H-bridge only						
PGND	27	Power ground for charge pump only						
PGND	36, 37	Power ground for right-channel H-bridge only						
PV_{DD}	21, 28	V _{DD} supply for charge-pump and gate-drive circuitry						
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier						
RINN	45	Class-D right-channel negative input						
RINP	44	Class-D right-channel positive input						
RPV _{DD}	33, 40	Class-D amplifier right-channel power supply						
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge						
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge						
SHUTDOWN	1	Active-low logic-level shutdown input signal. When SHUTDOWN is held low, the device goes into shutdown mode. When SHUTDOWN is held at logic high, the device operates normally.						
V2P5	29	2.5-V internal reference bypass						
VCP	22	Storage capacitor terminal for charge pump						
V _{DD}	8	V _{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.						



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Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0 [†]	FAULT 1 [†]	DESCRIPTION
1	1	No fault. — The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. — All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. FAULT1 is cleared by cycling MUTE, SHUTDOWN, or the power supply.
1	0	Over-current fault. — The output transistors are all switched off. This causes the load to be in a high-impedance state. This is a latched fault and is cleared by cycling MUTE, SHUTDOWN, or the power supply.
0	0	Thermal fault. — All the low-side transistors are turned on, shorting the load to ground. This is latched fault and is cleared by cycling MUTE, SHUTDOWN, or the power supply.

 $[\]ensuremath{^{\dagger}}$ These logic levels assume a pullup to PVDD from the open-drain outputs.

absolute maximum ratings over operating free-air temperature range, $T_C = 25^{\circ}C$ (unless otherwise noted)[‡]

Supply voltage, V _{DD} (PV _{DD} , LPV _{DD} , RPV _{DD} , V _{DD})	5.5 V
Input voltage, V _I (SHUTDOWN, MUTE)	
Output current, IO (FAULT0, FAULT1), open drain terminated	1 mA
Charge pump voltage, V _{CP}	PV _{DD} + 15 V
Continuous H-bridge output current	2 A
Pulsed H-Bridge output current, each output, I _{max} (see Note 1)	5 A
Continuous total power dissipation	See Dissipation Ratings Table
Operating virtual junction temperature range, T _J	–40°C to 150°C
Operating case temperature range, T _C	–40°C to 125°C
Storage temperature range, T _{stg}	–40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle \leq 2%

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C†	DERATING FACTOR	T _A = 70°C	T _A = 85°C	T _A = 125°C
	POWER RATING	ABOVE T _A = 25°C	POWER RATING	POWER RATING	POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W	1.1 mW

[†] Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, PV _{DD} , LPV _{DD} , RPV _{DD} , V _{DD}	4.5		5.5	V
High-level input voltage, VIH	4.25			V
Low-level input voltage, V _{IL}			0.75	V
Audio inputs, LINN, LINP, RINN, RINP, differential input voltage			1	VRMS
PWM frequency	150		450	kHZ



electrical characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = SV_{DD} = SV_{D

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 4.5 \text{ V}$ to 5.5 V		40		dB
I _{DD}	Supply current	No load, No filter		25	35	mA
I _{DD} (MUTE)	Supply current, mute mode	MUTE = 0 V		3.9	10	mA
I _{DD} (SD)	Supply current, shutdown mode	SHUTDOWN = 0 V		0.2	10	μΑ
lн	High-level input current	V _{IH} = 5.3 V			1	μΑ
I _{IL}	Low-level input current	V _{IL} = -0.3 V			-1	μΑ
r _{DS(on)}	Total static drain-to-source on-state resistance (low-side plus high-side FETs)	I _D = 2 A		700	900	mΩ
r _{DS(on)}	Matching, high-side to high-side, low-side to low-side, same channel	I _D = 0.5 A	95%	99%	·	

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = SV_{DD} = SV_{DD

	PARAMETER	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
PO	RMS output power, THD = 0.5%, per channel				2		W
THD+N	Total harmonic distortion plus noise	P _O = 1 W,	f = 1 kHz		0.2%		
	Efficiency	P _O = 1 W,	$R_L = 8 \Omega$		80%		
Ay	Gain				25		dB
	Left/right channel gain matching			95%	99%		
	Noise floor				-55		dBV
	Dynamic range				70		dB
	Crosstalk	f = 1 kHz			-55		dB
	Frequency response bandwidth, post output filter, -3 dB		·	20		20 000	Hz
ВОМ	Maximum output power bandwidth		·			20	kHz

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JP}$	Thermal resistance, junction-to-pad				10	°C/W
	Thermal shutdown temperature			165		°C

PARAMETER MEASUREMENT INFORMATION

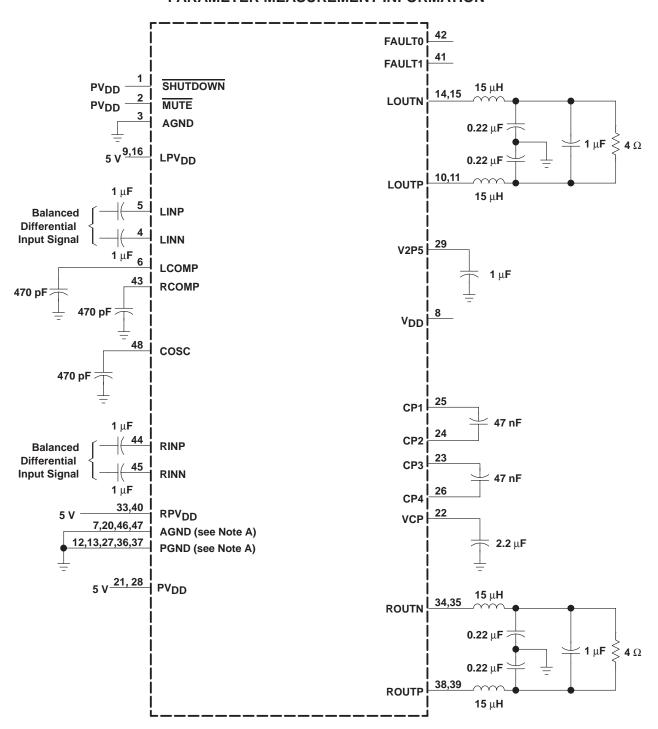


Figure 1. 5-V, 4- Ω Test Circuit, Class-D Amplifier





PACKAGE OPTION ADDENDUM

31-Mar-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPA005D12DCA	NRND	HTSSOP	DCA	48	40	TBD	CU NIPDAU	Level-3-220C-168 HR	
TPA005D12DCARG4	ACTIVE	HTSSOP	DCA	48		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCA (R-PDSO-G48)

PowerPAD ™ PLASTIC SMALL-OUTLINE



NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com.

 E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-153

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DCA (R-PDSO-G48)

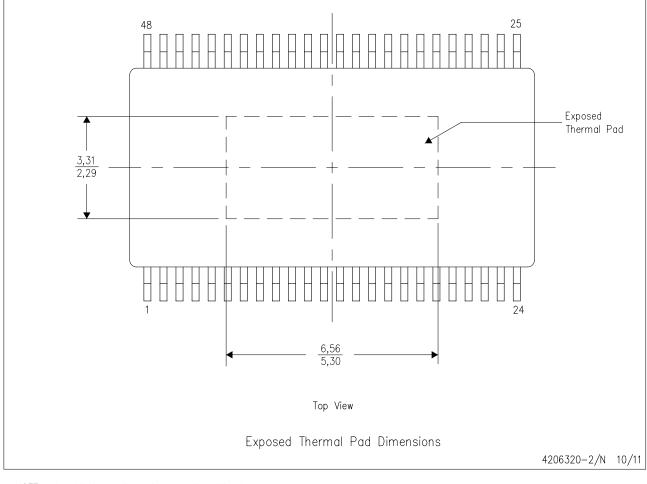
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD $^{\text{M}}$ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters

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