



## TS4984FC

### 1.2W Stereo Audio Power Amplifier with Active Low Standby Mode

- Operating from  $V_{CC} = 2.2V$  to  $5.5V$
- 1.2W output power per channel @  $V_{CC} = 5V$ , THD+N = 1%,  $R_L = 8\Omega$
- 10nA standby current
- 62dB PSRR @ 217Hz with grounded inputs
- High SNR: 106dB(A) typ.
- Near-zero pop & click
- Available in a 15-bump flip-chip (lead-free)

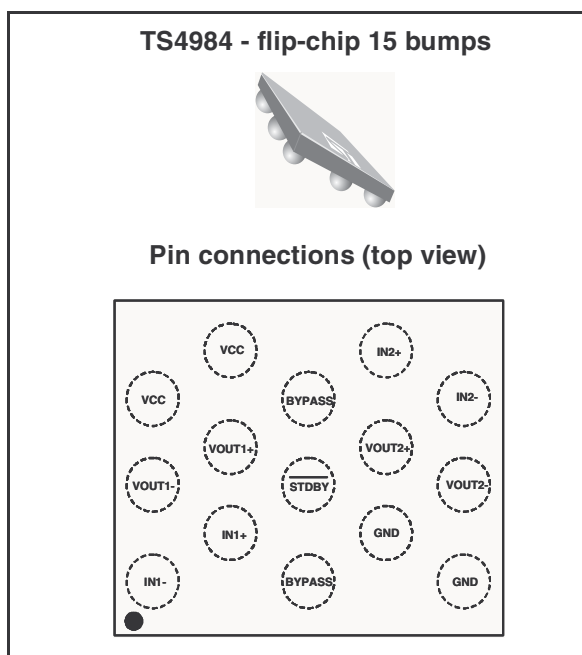
### Description

The TS4984 has been designed for top-class stereo audio applications. Thanks to its compact and power dissipation efficient flip-chip package, it suits various applications.

With a output BTL configuration, this audio power amplifier is capable of delivering 1.2W per channel of continuous RMS output power into an  $8\Omega$  load @ 5V.

An externally-controlled standby mode reduces the supply current to less than 10nA per channel. The device also features an internal thermal shutdown protection.

The gain of each channel can be configured by external gain setting resistors.



### Applications

- Cellular mobile phones
- Notebook & PDA computers
- LCD monitors & TVs
- Portable audio devices

### Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TS4984EIJT	-40, +85°C	Lead free flip-chip	Tape & Reel	A84
TS4984EIKJT		Lead free flip-chip + back coating		

# 1 Typical Application Schematic

Figure 1 show a typical application schematic for the TS4984FC.

Figure 1. Application information

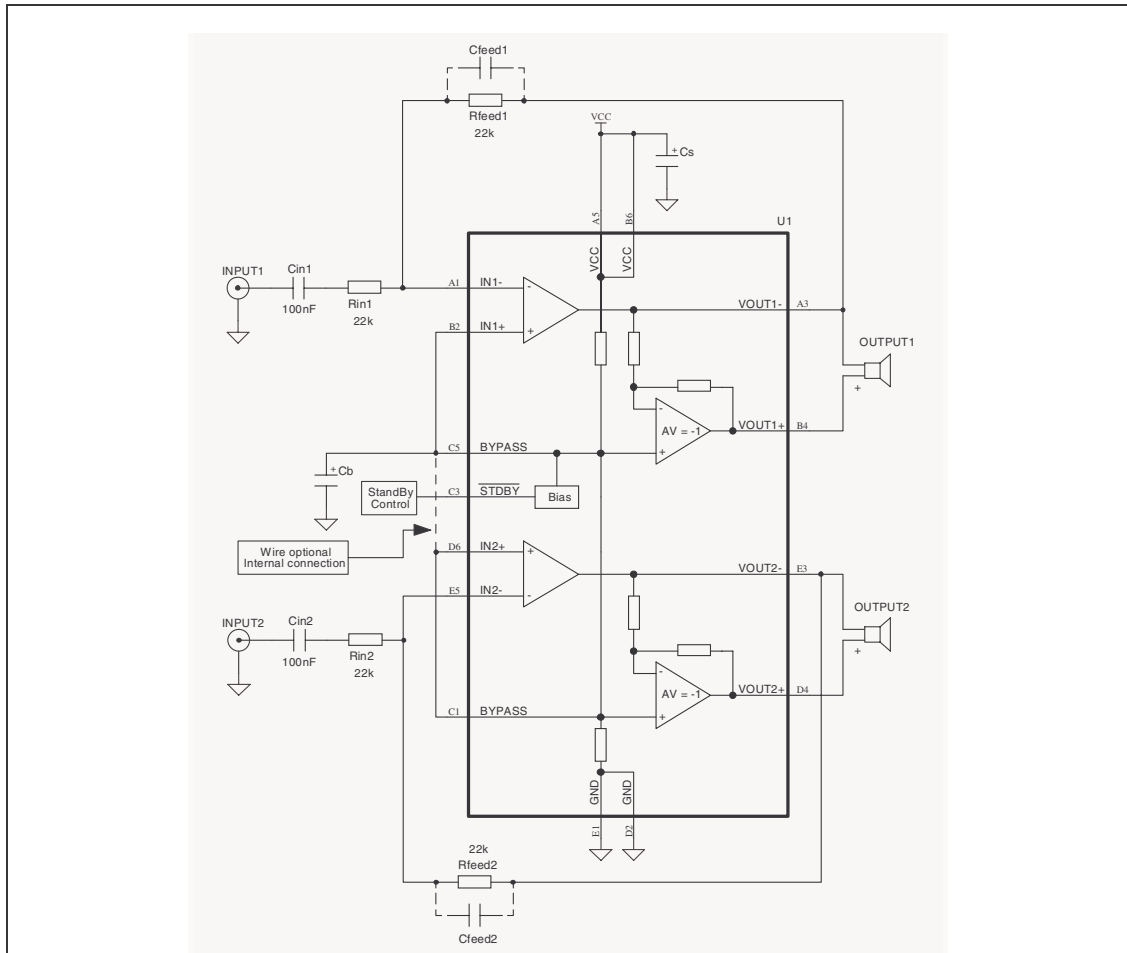


Table 1. External component descriptions

Components	Functional Description
$R_{in\ L,R}$	Inverting input resistors which sets the closed loop gain in conjunction with $R_{feed}$ . These resistors also form a high pass filter with $C_{in} = 1/2 \times \pi \times R_{in} \times C_{in}$
$C_{in\ L,R}$	Input coupling capacitors which blocks the DC voltage at the amplifier input terminal
$R_{feed\ L,R}$	Feedback resistors which sets the closed loop gain in conjunction with $R_{in}$
$C_s$	Supply Bypass capacitor which provides power supply filtering
$C_b$	Bypass pin capacitor which provides half supply filtering
$A_{V\ L,R}$	Closed loop gain in BTL configuration = $2 \times (R_{feed} / R_{in})$ on each channel

## 2 Absolute Maximum Ratings

**Table 2. Key parameters and their absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_i$	Input Voltage <sup>(2)</sup>	GND to $V_{CC}$	V
$T_{oper}$	Operating Free Air Temperature Range	-40 to + 85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_j$	Maximum Junction Temperature	150	°C
$R_{thja}$	Thermal Resistance Junction to Ambient for Flip-chip15	180	°C/W
$P_{diss}$	Power Dissipation	Internally Limited	
ESD	Human Body Model <sup>(3)</sup>	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	200mA	

1. All voltages values are measured with respect to the ground pin
2. The magnitude of input signal must never exceed  $V_{CC} + 0.3V / G_{ND} - 0.3V$
3. All voltage values are measured from each pin with respect to supplies

**Table 3. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2.2 to 5.5	V
$V_{ICM}$	Common Mode Input Voltage Range	1.2V to $V_{CC}$	V
$V_{STBY}$	Standby Voltage Input: Device ON Device OFF	$1.35 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
$R_L$	Load Resistor	$\geq 4$	$\Omega$
$R_{OUTGND}$	Resistor Output to GND ( $V_{STBY} = GND$ )	$\geq 1$	M $\Omega$
$T_{SD}$	Thermal Shutdown Temperature	150	°C
$R_{thja}$	Thermal Resistance Junction to Ambient Flip-chip15 <sup>(1)</sup>	110	°C/W

1. When mounted on a 4-layer PCB

### 3 Electrical Characteristics

**Table 4.**  $V_{CC} = +5V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current	No input signal, no load		7.4	12	mA
$I_{STBY}$	Standby Current <sup>(1)</sup>	No input signal, $V_{STBY} = GND$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage	No input signal, $R_L = 8\Omega$		1	10	mV
$P_{out}$	Output Power	THD = 1% Max, $F = 1kHz$ , $R_L = 8\Omega$	0.9	1.2		W
THD + N	Total Harmonic Distortion + Noise	$P_{out} = 1Wrms$ , $A_V = 2$ $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$		0.2		%
PSRR	Power Supply Rejection Ratio <sup>(2)</sup>	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 217Hz$	55	62		dB
		$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 1kHz$	55	64		
Crosstalk	Channel Separation,	$R_L = 8\Omega$ , $F = 1kHz$		107		dB
		$R_L = 8\Omega$ , $F = 20Hz$ to $20kHz$		82		
$t_{wu}$	Wake-Up Time	$C_b = 1\mu F$		90	130	ms
$t_{stby}$	Standby Time	$C_b = 1\mu F$		10		$\mu s$
$V_{STBYH}$	Standby Voltage Level High				1.3	V
$V_{STBYL}$	Standby Voltage Level Low				0.4	V
$\Phi_M$	Phase Margin at Unity Gain	$R_L = 8\Omega$ , $C_L = 500pF$		65		Degrees
GM	Gain Margin	$R_L = 8\Omega$ , $C_L = 500pF$		15		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		1.5		MHz

1. Standby mode is activated when  $V_{STBY}$  is tied to Gnd.

2. All PSRR data limits are guaranteed by production sampling tests.

Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is the sinusoidal signal superimposed upon  $V_{CC}$ .

Table 5.  $V_{CC} = +3.3V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current	No input signal, no load		6.6	12	mA
$I_{STBY}$	Standby Current <sup>(1)</sup>	No input signal, $V_{STBY} = GND$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage	No input signal, $R_L = 8\Omega$		1	10	mV
$P_{out}$	Output Power	THD = 1% Max, $F = 1kHz$ , $R_L = 8\Omega$	375	500		mW
THD + N	Total Harmonic Distortion + Noise	$P_{out} = 400mWrms$ , $A_V = 2$ $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection Ratio <sup>(2)</sup>	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 217Hz$	55	61		dB
		$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 1kHz$	55	63		
Crosstalk	Channel Separation,	$R_L = 8\Omega$ , $F = 1kHz$		107		dB
		$R_L = 8\Omega$ , $F = 20Hz$ to $20kHz$		82		
$t_{wu}$	Wake-Up Time	$C_b = 1\mu F$		110	140	ms
$t_{stby}$	Standby Time	$C_b = 1\mu F$		10		$\mu s$
$V_{STBYH}$	Standby Voltage Level High				1.2	V
$V_{STBYL}$	Standby Voltage Level Low				0.4	V
$\Phi_M$	Phase Margin at Unity Gain	$R_L = 8\Omega$ , $C_L = 500pF$		65		Degrees
GM	Gain Margin	$R_L = 8\Omega$ , $C_L = 500pF$		15		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		1.5		MHz

- Standby mode is activated when  $V_{STBY}$  is tied to Gnd.
- All PSRR data limits are guaranteed by production sampling tests.  
Dynamic measurements -  $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$ .  $V_{ripple}$  is the sinusoidal signal superimposed upon  $V_{CC}$ .

Table 6.  $V_{CC} = +2.6V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current	No input signal, no load		6.2	12	mA
$I_{STBY}$	Standby Current <sup>(1)</sup>	No input signal, $V_{STBY} = GND$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage	No input signal, $R_L = 8\Omega$		1	10	mV
$P_{out}$	Output Power	THD = 1% Max, $F = 1kHz$ , $R_L = 8\Omega$	220	300		mW
THD + N	Total Harmonic Distortion + Noise	$P_{out} = 200mWrms$ , $A_V = 2$ $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection Ratio <sup>(2)</sup>	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 217Hz$	55	60		dB
		$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 1kHz$	55	62		
Crosstalk	Channel Separation,	$R_L = 8\Omega$ , $F = 1kHz$		107		dB
		$R_L = 8\Omega$ , $F = 20Hz$ to $20kHz$		82		
$t_{wu}$	Wake-Up Time	$C_b = 1\mu F$		125	150	ms
$t_{stby}$	Standby Time	$C_b = 1\mu F$		10		$\mu s$
$V_{STBYH}$	Standby Voltage Level High				1.2	V
$V_{STBYL}$	Standby Voltage Level Low				0.4	V
$\Phi_M$	Phase Margin at Unity Gain	$R_L = 8\Omega$ , $C_L = 500pF$		65		Degrees
GM	Gain Margin	$R_L = 8\Omega$ , $C_L = 500pF$		15		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		1.5		MHz

- Standby mode is activated when  $V_{STBY}$  is tied to Gnd.
- All PSRR data limits are guaranteed by production sampling tests.  
Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is the sinusoidal signal superimposed upon  $V_{CC}$ .

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Figure 2. Open loop frequency response

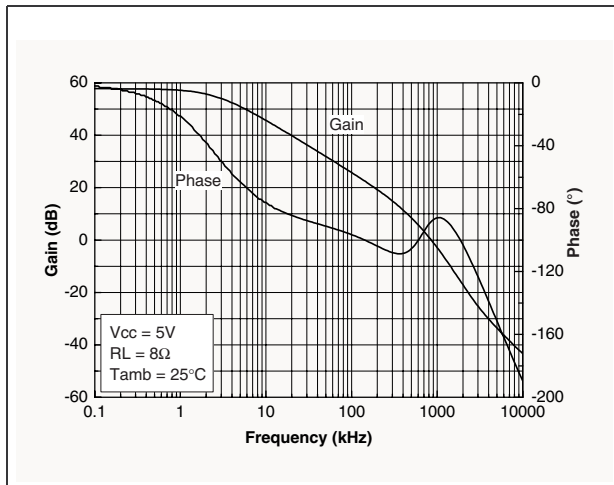


Figure 3. Open loop frequency response

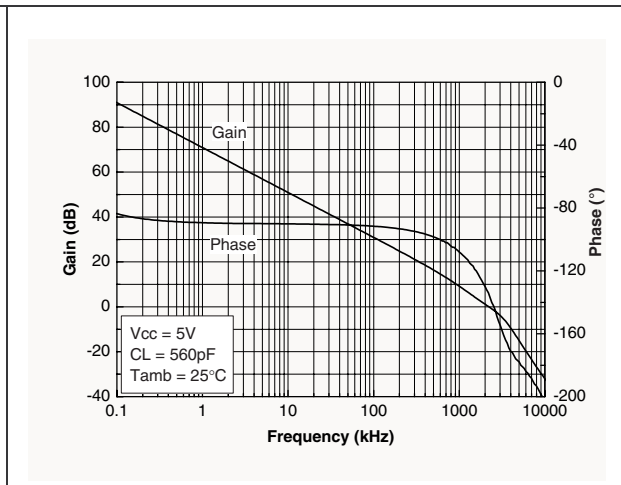


Figure 4. Open loop frequency response

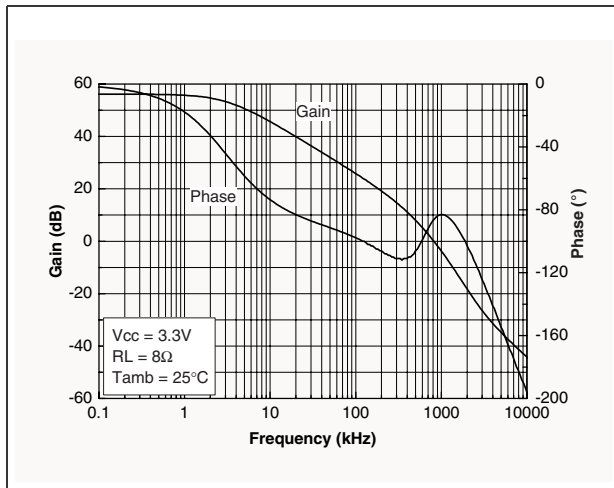


Figure 5. Open loop frequency response

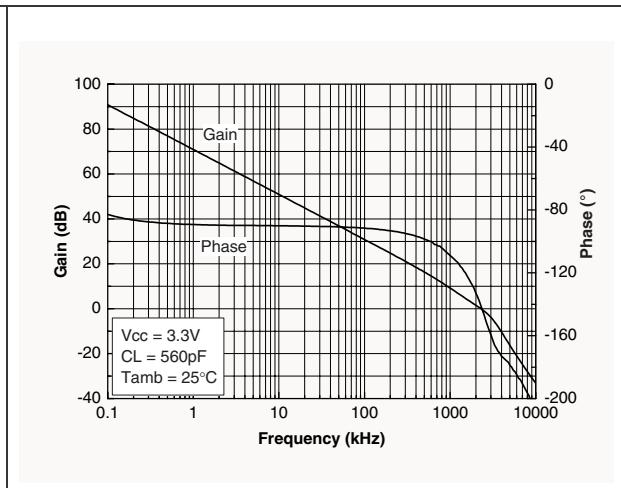


Figure 6. Open loop frequency response

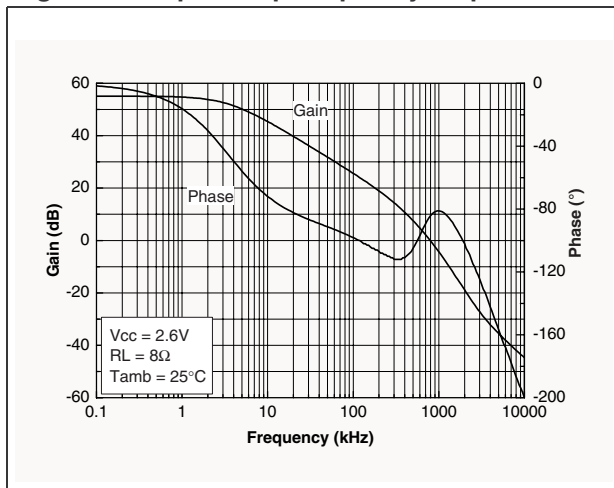


Figure 7. Open loop frequency response

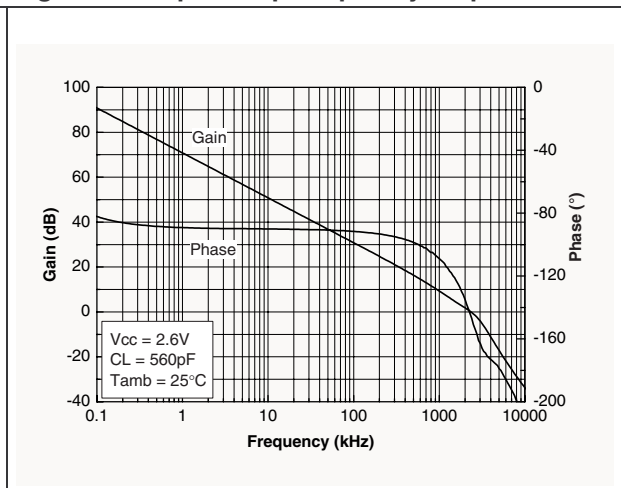




Figure 8. Power supply rejection ratio (PSRR) vs. frequency Figure 9. Power supply rejection ratio (PSRR) vs. frequency

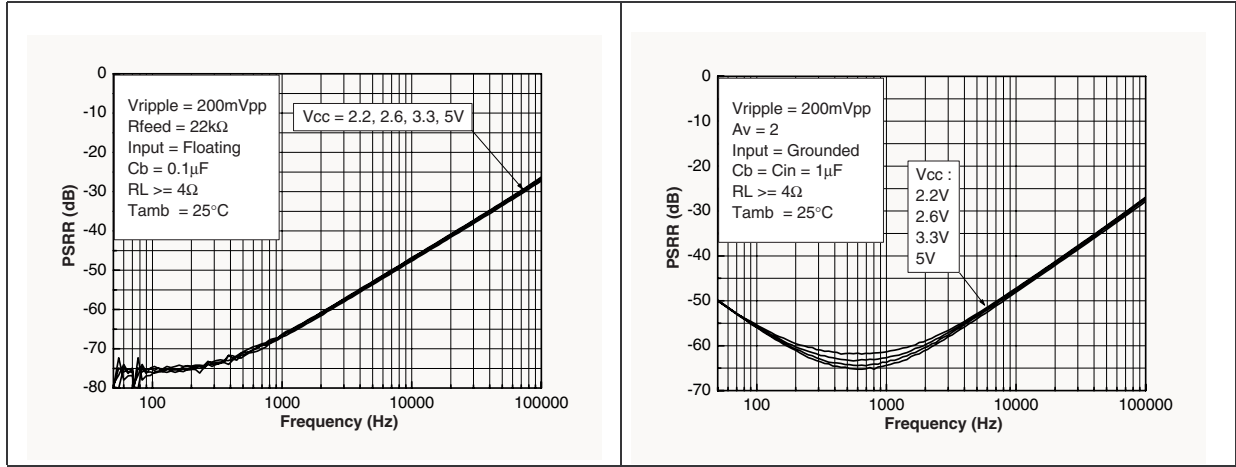


Figure 10. Power supply rejection ratio (PSRR) vs. frequency Figure 11. Power supply rejection ratio (PSRR) vs. frequency

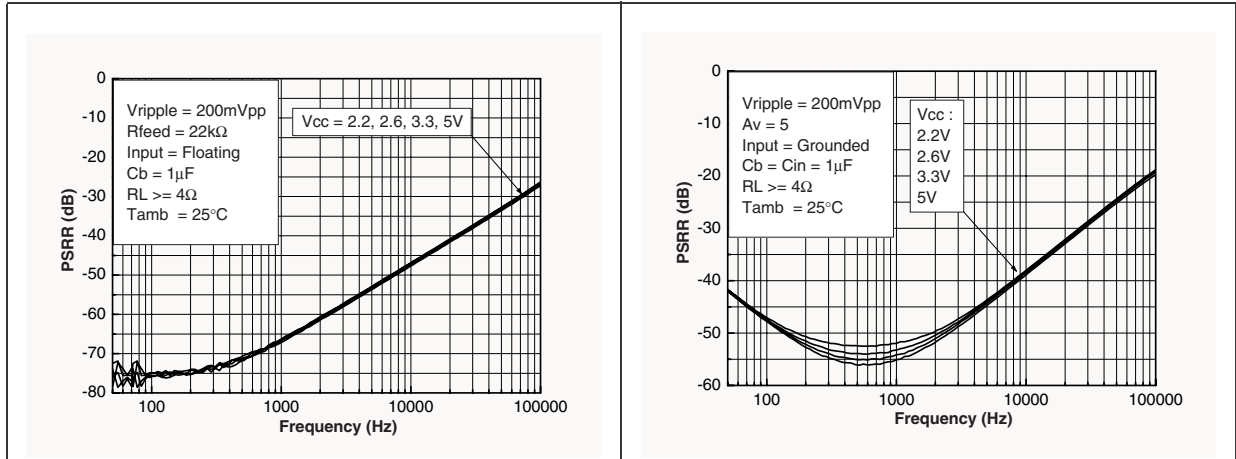


Figure 12. Power supply rejection ratio (PSRR) vs. frequency Figure 13. Power supply rejection ratio (PSRR) vs. frequency

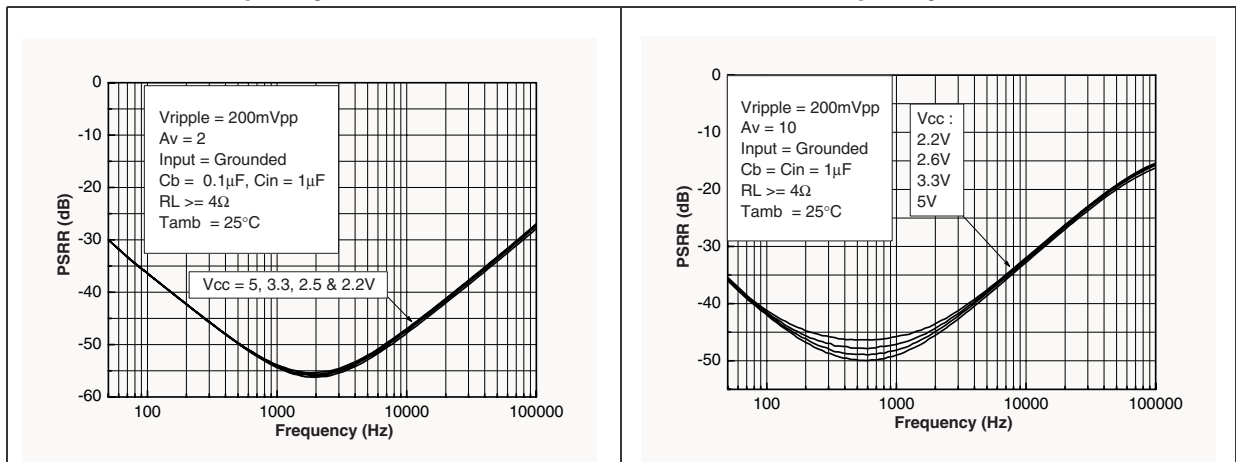


Figure 14. Power supply rejection ratio (PSRR) vs. DC output voltage Figure 15. Power supply rejection ratio (PSRR) vs. DC output voltage

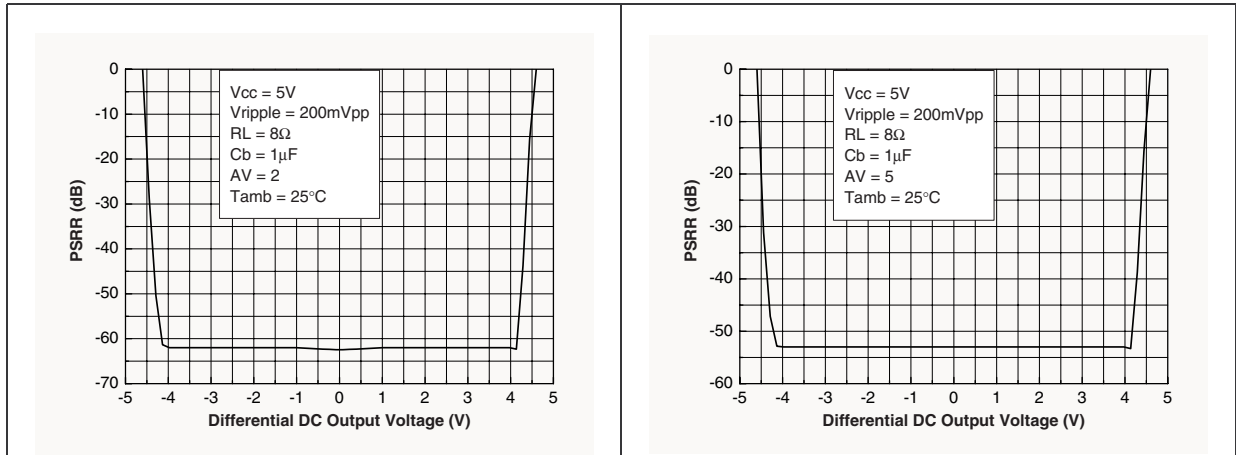


Figure 16. Power supply rejection ratio (PSRR) vs. DC output voltage Figure 17. Power supply rejection ratio (PSRR) vs. DC output voltage

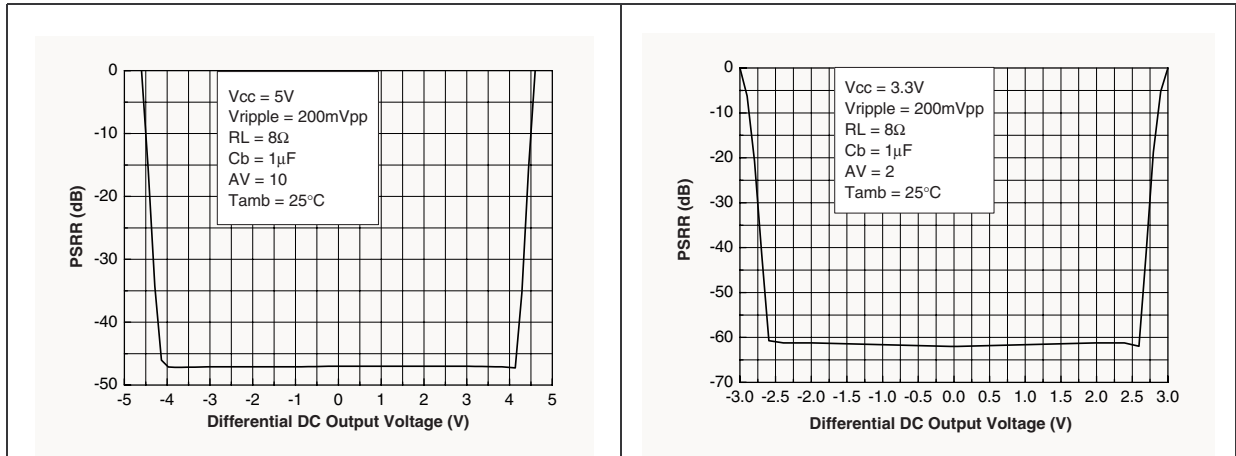


Figure 18. Power supply rejection ratio (PSRR) vs. DC output voltage Figure 19. Power supply rejection ratio (PSRR) vs. DC output voltage

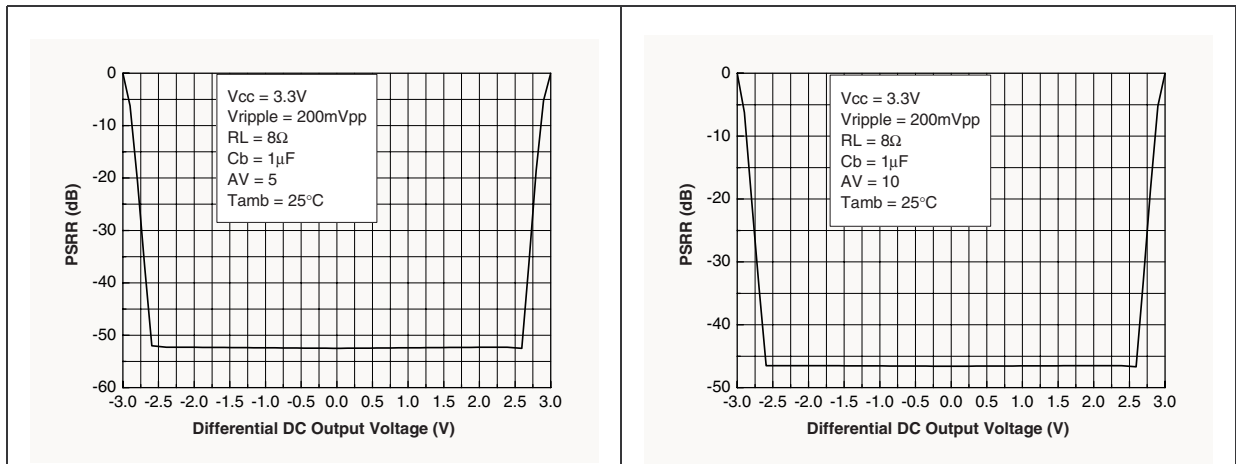


Figure 20. Power supply rejection ratio (PSRR) vs. DC output voltage

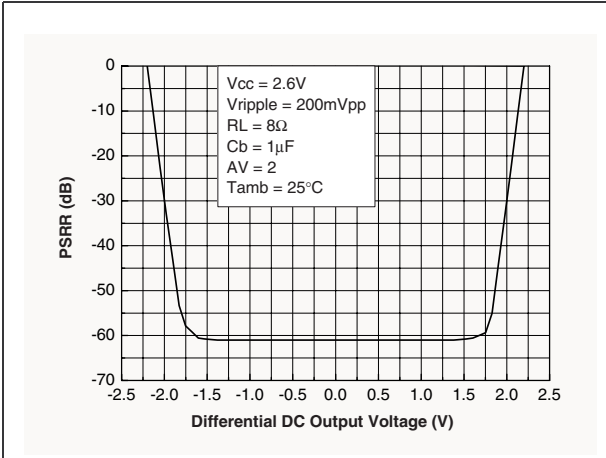


Figure 21. Power supply rejection ratio (PSRR) vs. DC output voltage

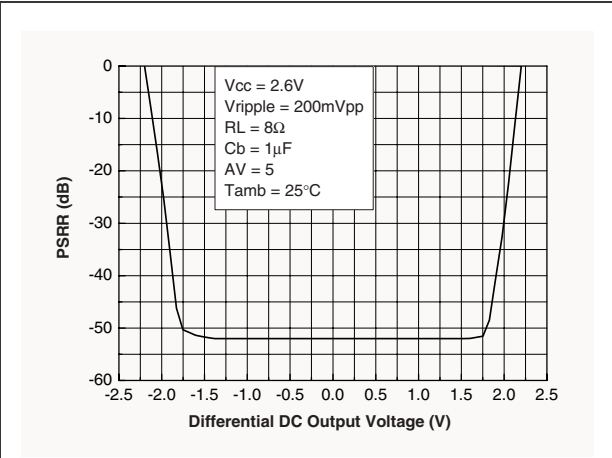


Figure 22. Power supply rejection ratio (PSRR) vs. DC output voltage

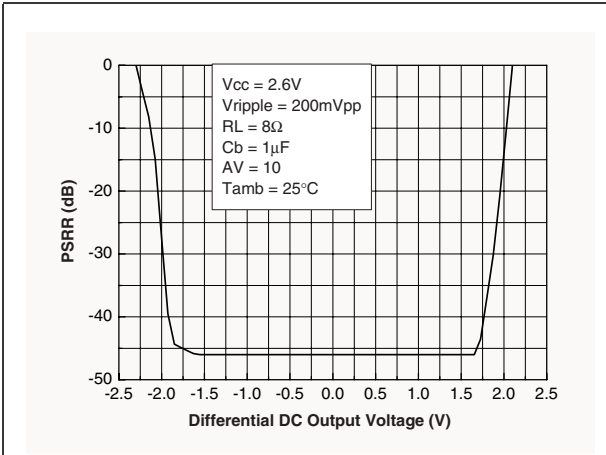


Figure 23. Power supply rejection ratio (PSRR) at F = 217Hz vs. bypass capacitor

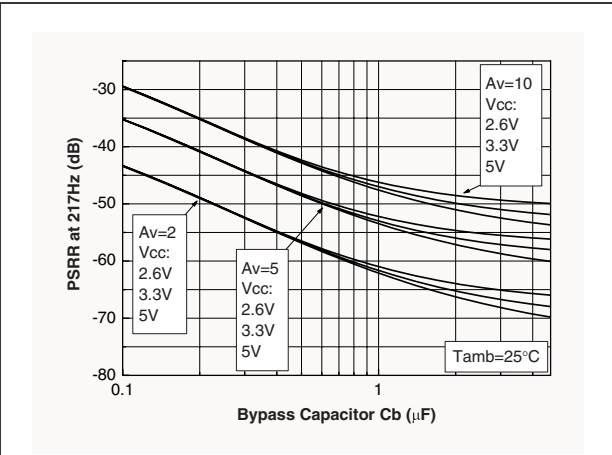


Figure 24. Output power vs. power supply voltage

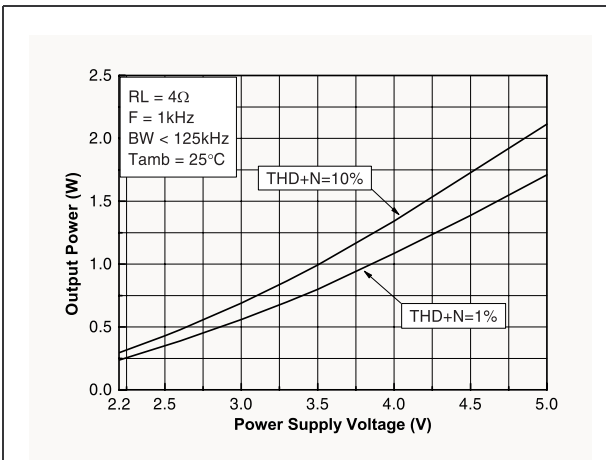


Figure 25. Output power vs. power supply voltage

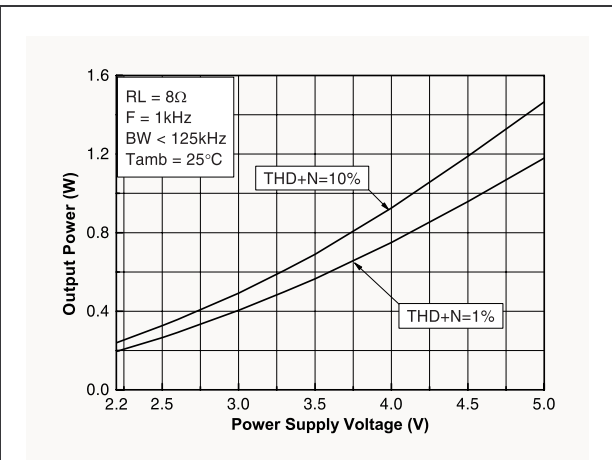


Figure 26. Output power vs. power supply voltage

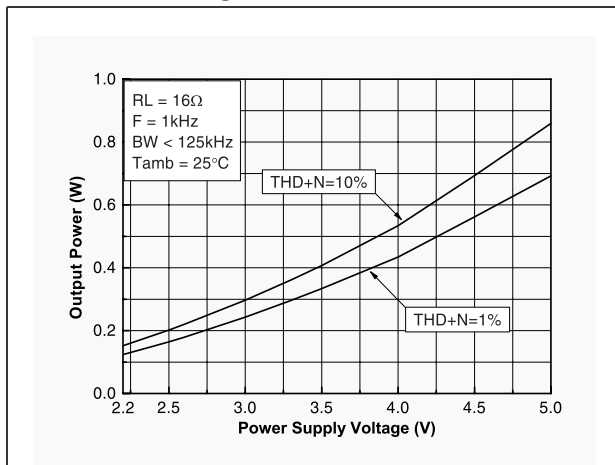


Figure 27. Output power vs. power supply voltage

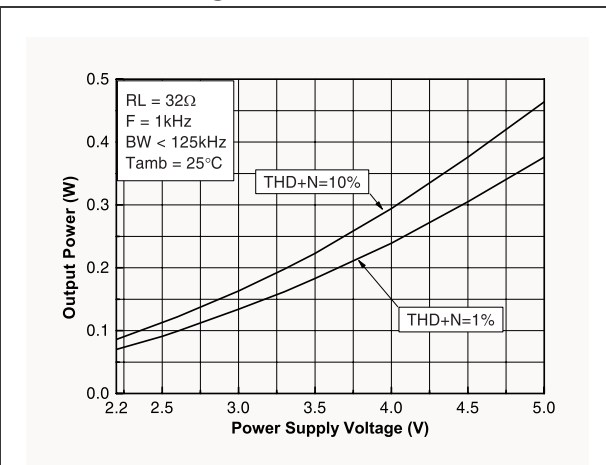


Figure 28. Output power vs. load resistor

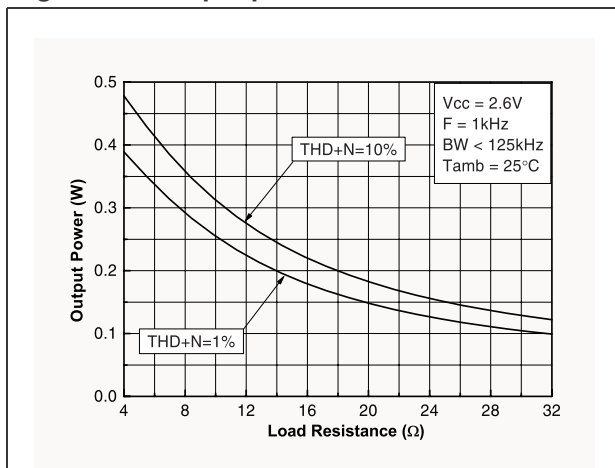


Figure 29. Output power vs. load resistor

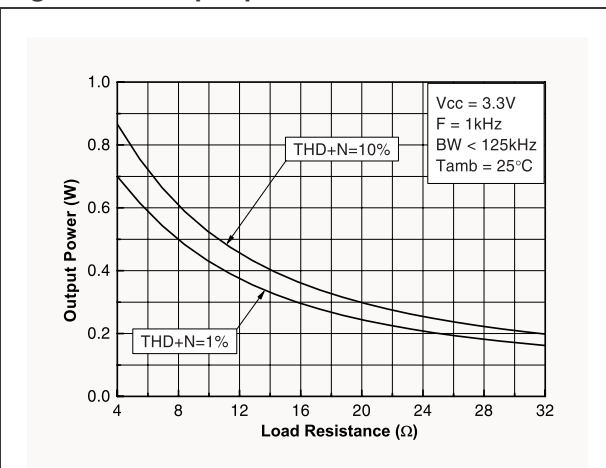


Figure 30. Output power vs. load resistor

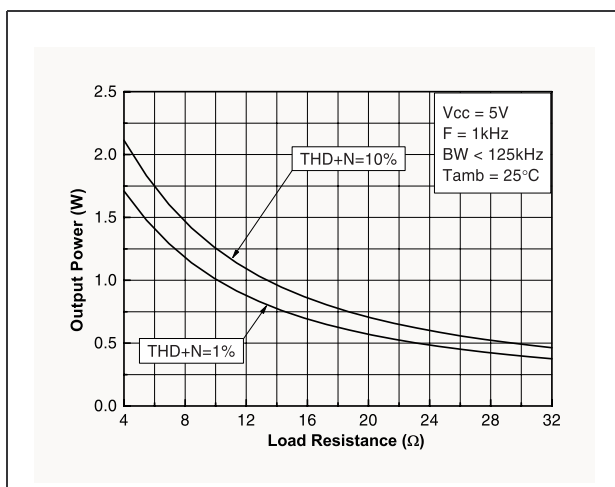


Figure 31. Power dissipation vs. output power per channel

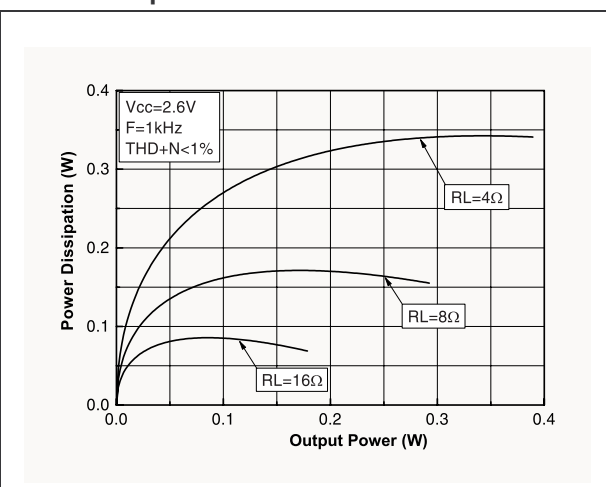


Figure 32. Power dissipation vs. output power per channel

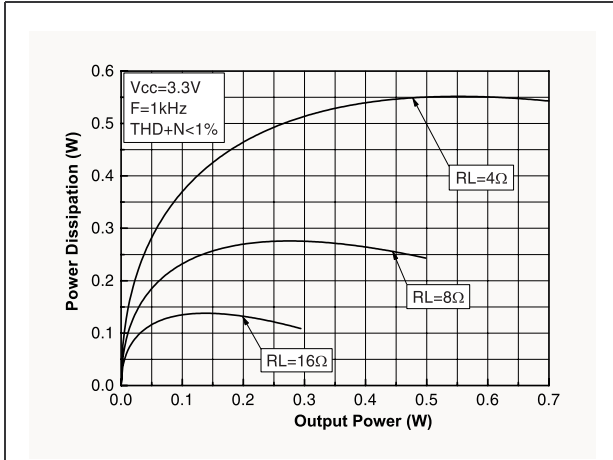


Figure 33. Power dissipation vs. output power per channel

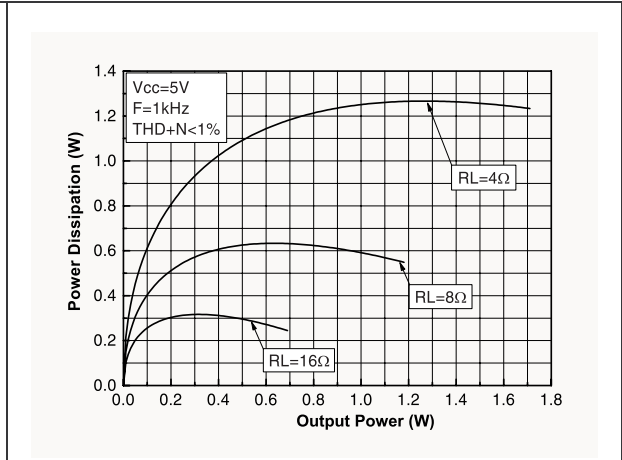


Figure 34. Clipping voltage vs. power supply voltage and load resistor

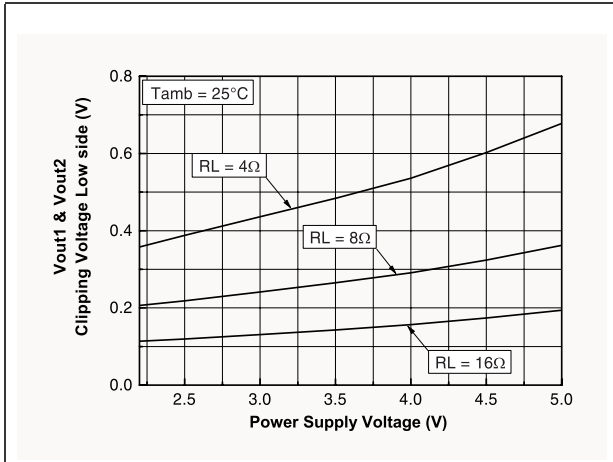


Figure 35. Clipping voltage vs. power supply voltage and load resistor

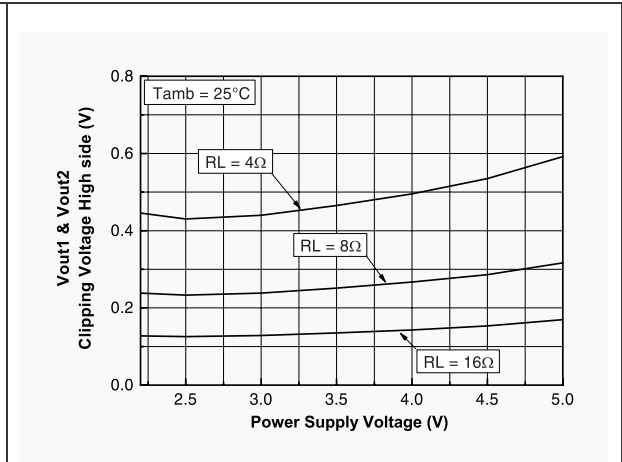


Figure 36. Current consumption vs. power supply voltage

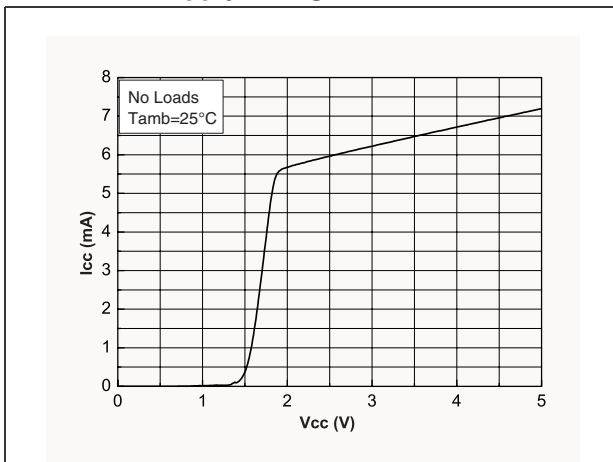


Figure 37. Current consumption vs. standby voltage at  $V_{CC} = 5V$

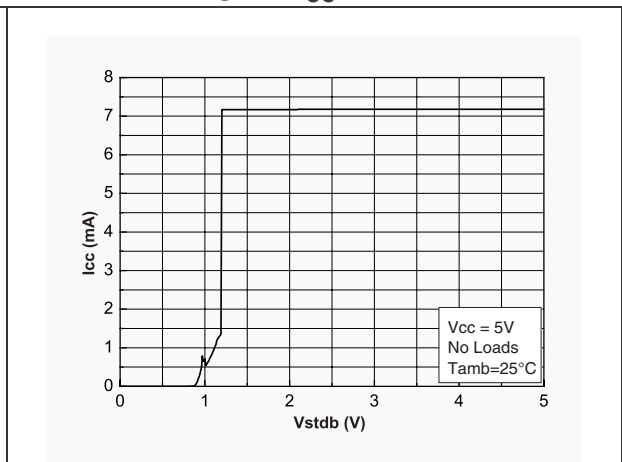


Figure 38. Current consumption vs. standby voltage at  $V_{CC} = 3.3V$

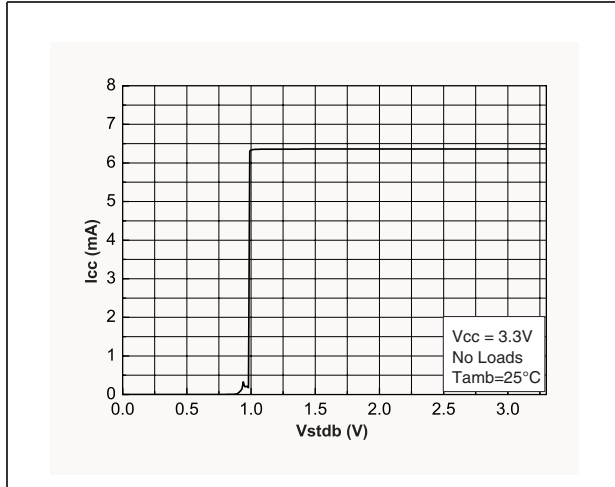


Figure 39. Current consumption vs. standby voltage at  $V_{CC} = 2.6V$

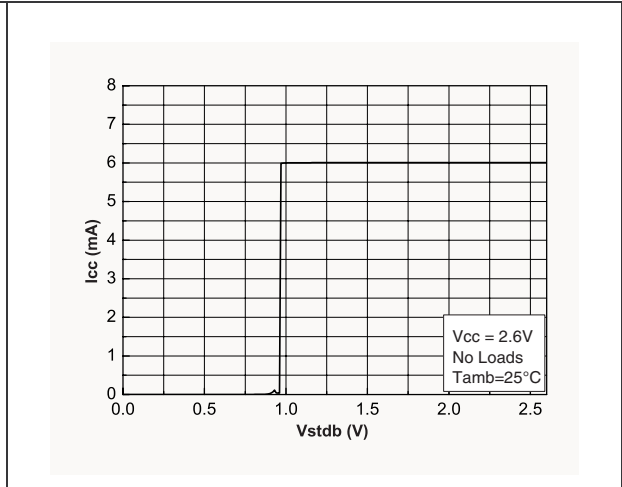


Figure 40. Power derating curves

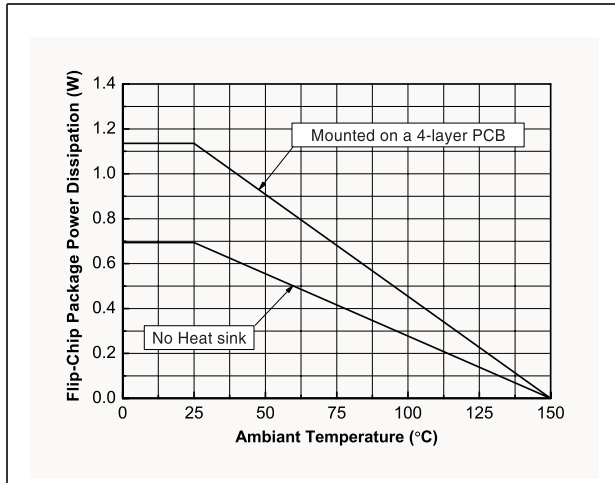


Figure 41. THD + N vs. output power

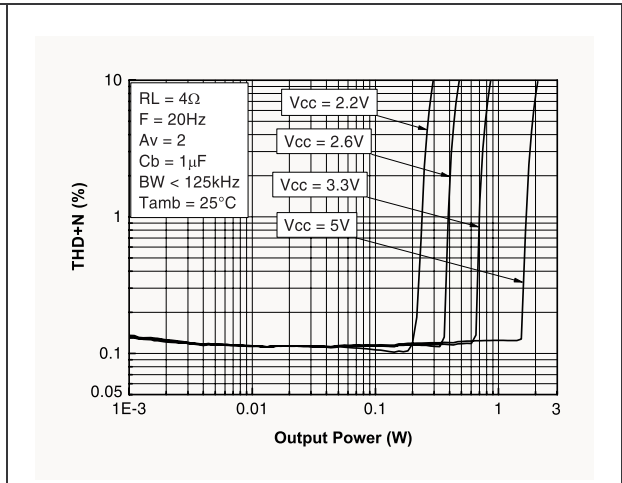


Figure 42. THD + N vs. output power

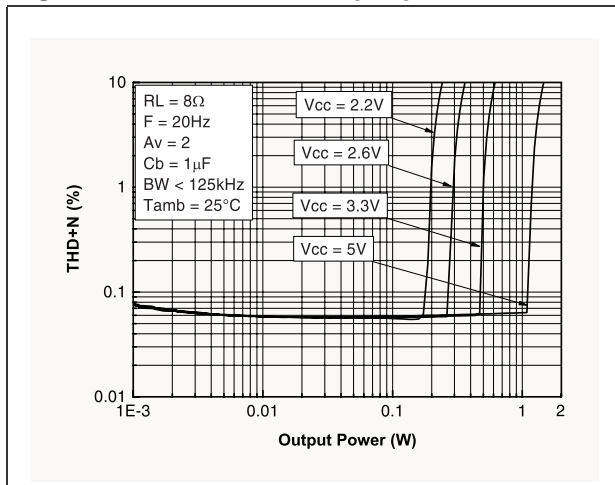


Figure 43. THD + N vs. output power

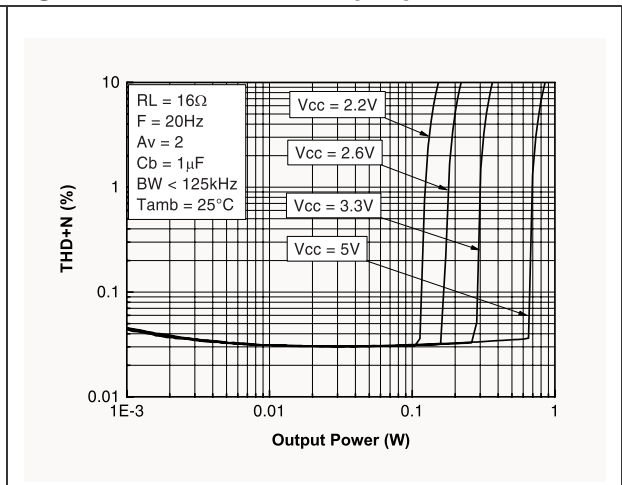


Figure 44. THD + N vs. output power

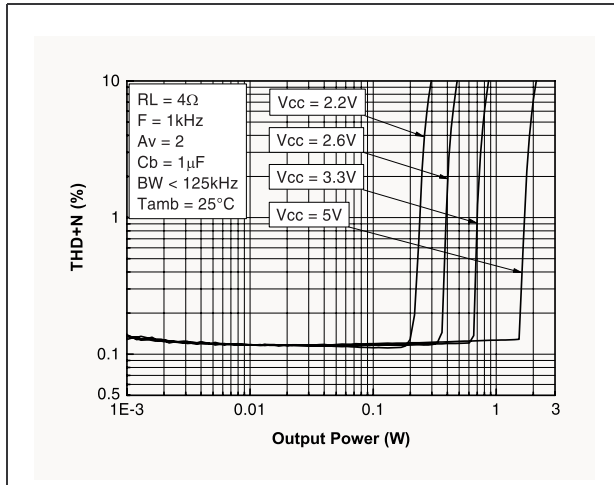


Figure 45. THD + N vs. output power

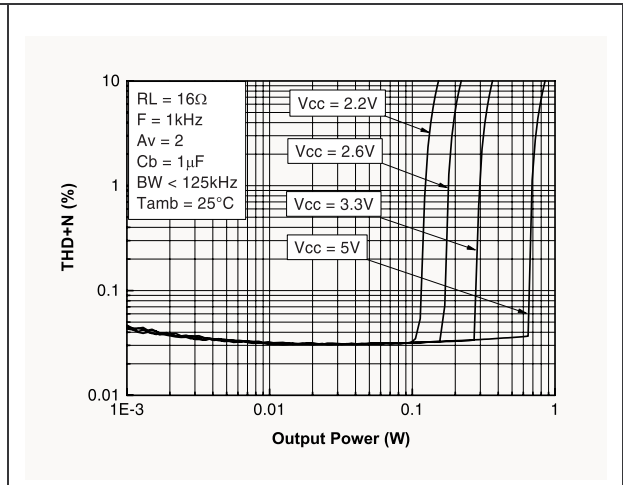


Figure 46. THD + N vs. output power

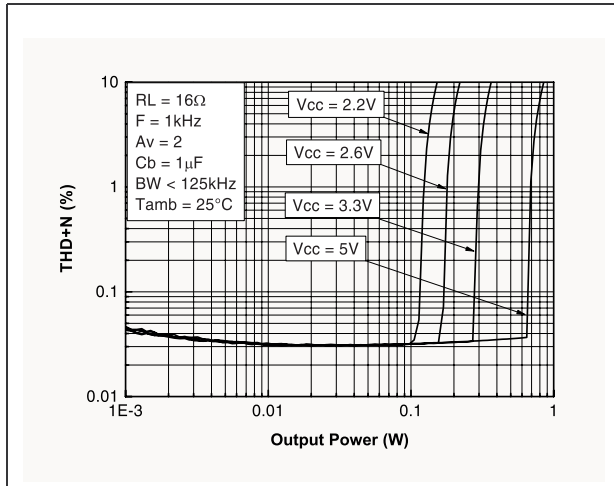


Figure 47. THD + N vs. output power

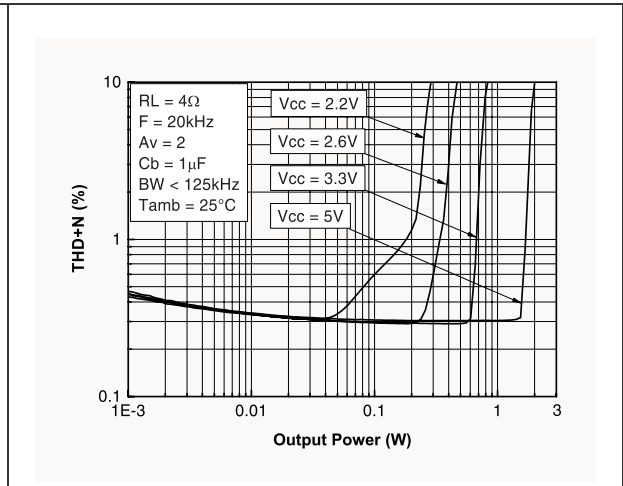


Figure 48. THD + N vs. output power

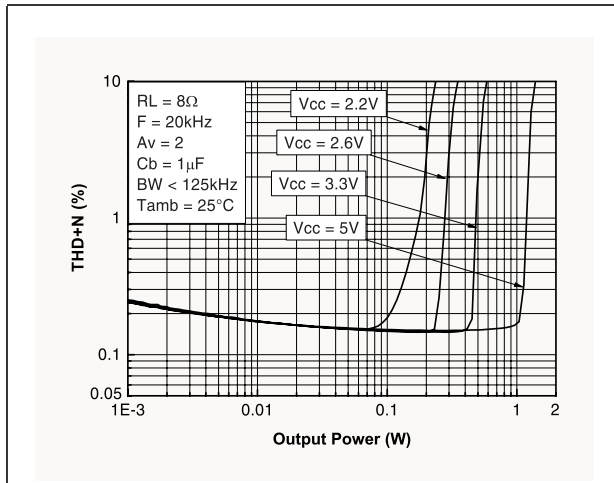


Figure 49. THD + N vs. output power

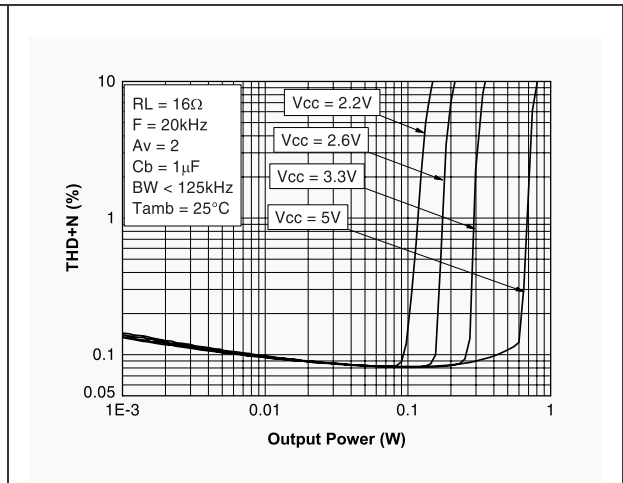


Figure 50. THD + N vs. frequency

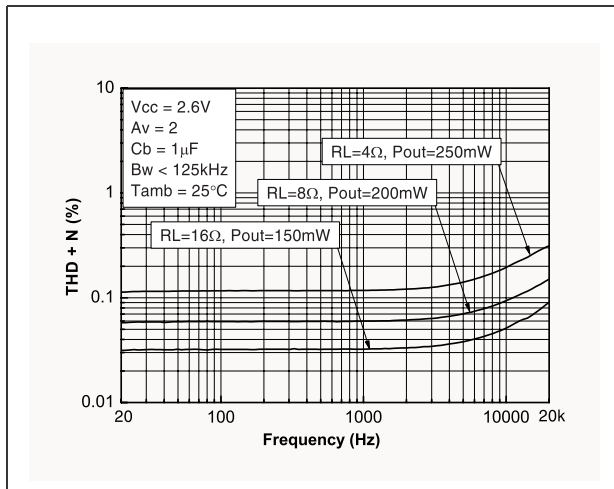


Figure 51. THD + N vs. frequency

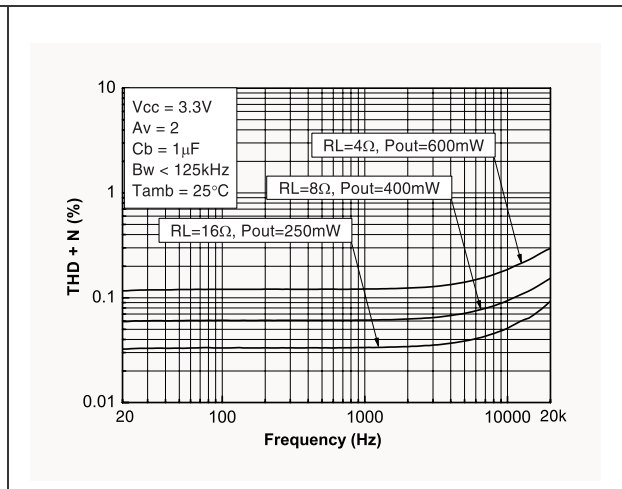


Figure 52. THD + N vs. frequency

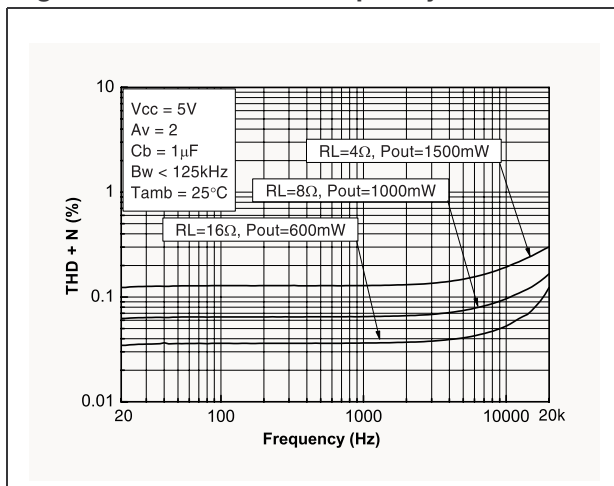


Figure 53. Crosstalk vs. frequency

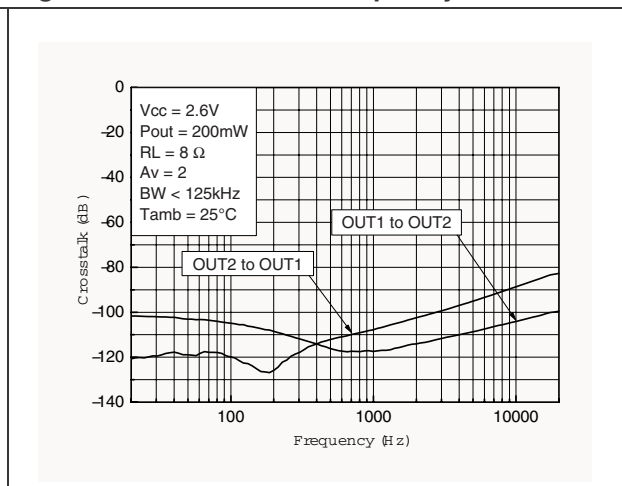


Figure 54. Crosstalk vs. frequency

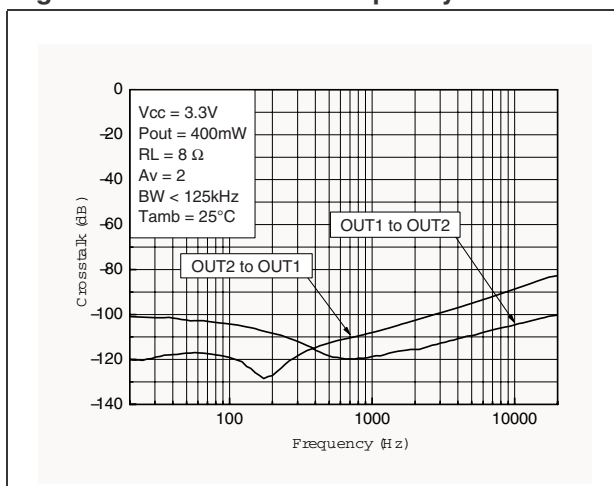


Figure 55. Crosstalk vs. frequency

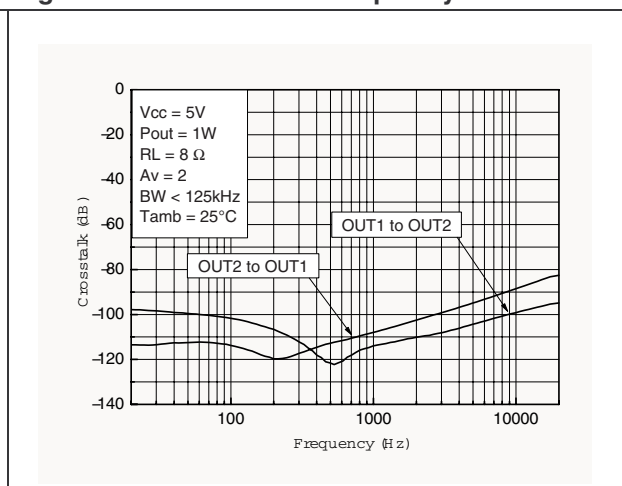




Figure 56. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

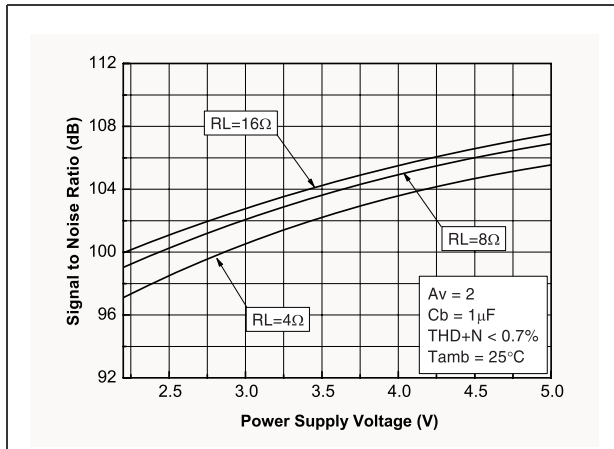


Figure 57. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

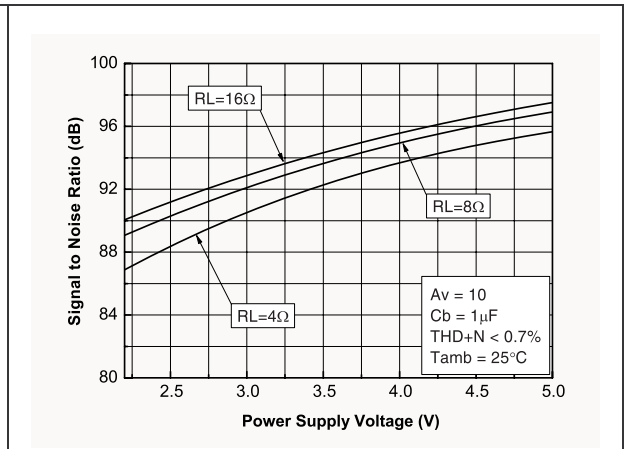


Figure 58. Signal to noise ratio vs. power supply with A weighted filter

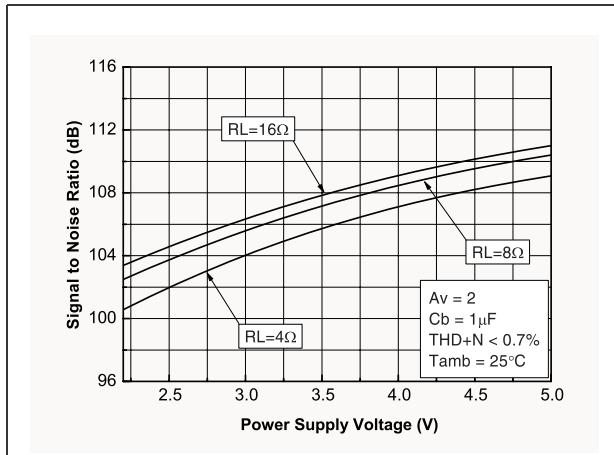


Figure 59. Signal to noise ratio vs. power supply with A weighted filter

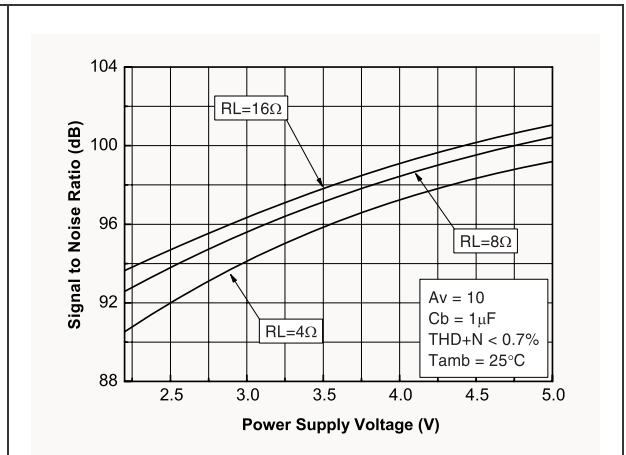


Figure 60. Output noise voltage, device ON

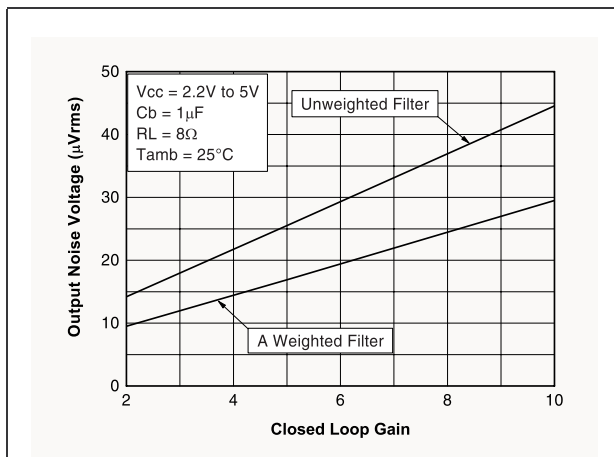
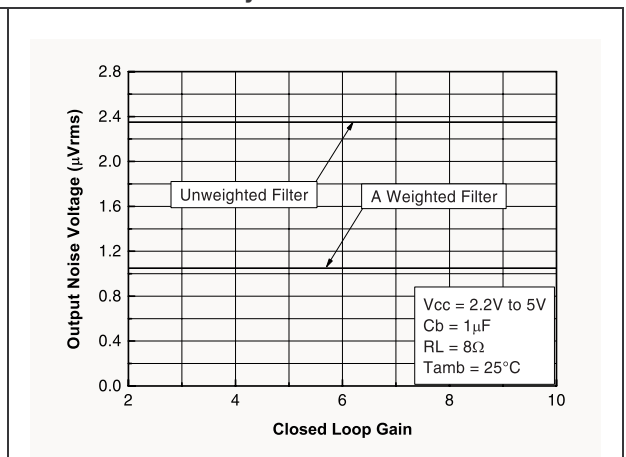


Figure 61. Output noise voltage, device in standby



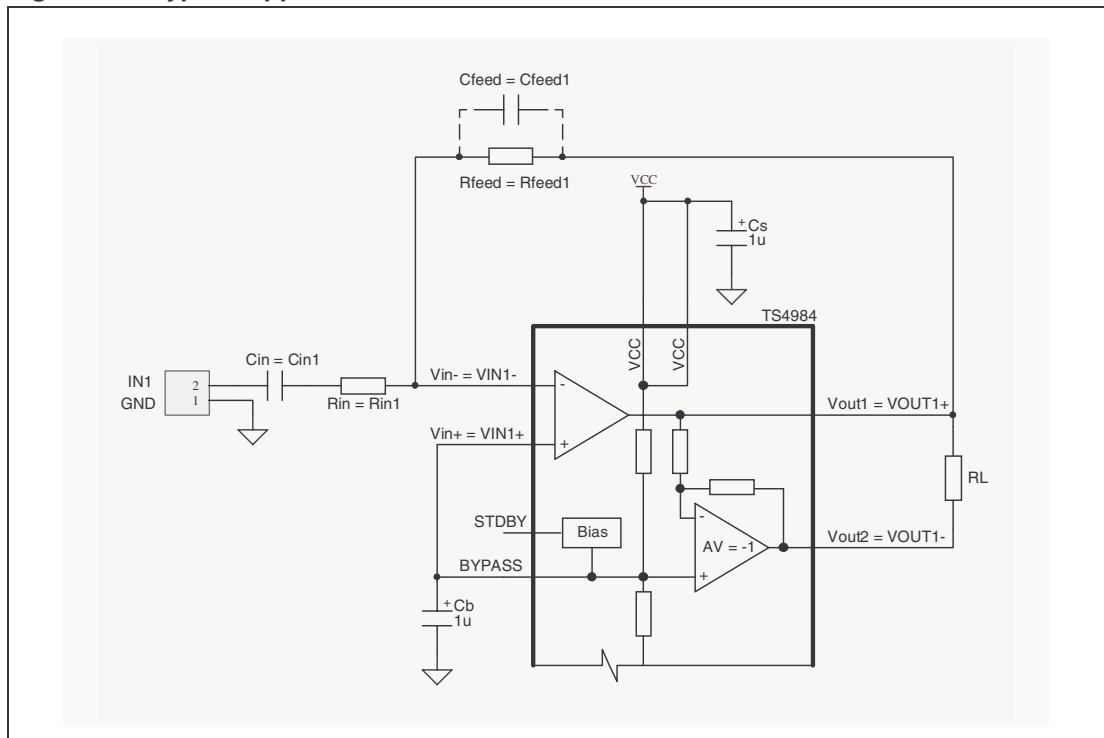
## 4 Application Information

The TS4984 integrates two monolithic power amplifiers with a BTL (Bridge Tied Load) output type (explained in more detail in *Section 4.1*). For this discussion, only the left-channel amplifier will be referred to.

Referring to the schematic in *Figure 62*, we assign the following variables and values:

- $V_{in} = Vin1-$
- $V_{out1} = VOUT1+$
- $V_{out2} = VOUT1-$
- $R_{in} = Rin1$
- $R_{feed} = Rfeed1$
- $C_{feed} = Cfeed1$

**Figure 62. Typical application schematic - left channel**



### 4.1 BTL configuration principle

BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

$$\text{Single-ended output 1} = V_{out1} = V_{out} \text{ (V),}$$

$$\text{Single-ended output 2} = V_{out2} = -V_{out} \text{ (V), } V_{out1} - V_{out2} = 2V_{out} \text{ (V)}$$

The output power is:

$$P_{\text{out}} = \frac{(2V_{\text{outRMS}})^2}{R_L}$$

For the same power supply voltage, the output power in a BTL configuration is four times higher than the output power in a single-ended configuration.

## 4.2 Gain in typical application schematic

The typical application schematic (*Figure 62*) is shown on *page 18*.

In the flat region (no  $C_{\text{in}}$  effect), the output voltage of the first stage is:

$$V_{\text{out1}} = (-V_{\text{in}}) \frac{R_{\text{feed}}}{R_{\text{in}}} \quad (\text{V})$$

For the second stage:

$$V_{\text{out2}} = -V_{\text{out1}} \quad (\text{V})$$

The differential output voltage is:

$$V_{\text{out2}} - V_{\text{out1}} = 2V_{\text{in}} \frac{R_{\text{feed}}}{R_{\text{in}}} \quad (\text{V})$$

The differential gain, referred to as  $G_v$  for greater convenience, is:

$$G_v = \frac{V_{\text{out2}} - V_{\text{out1}}}{V_{\text{in}}} = 2 \frac{R_{\text{feed}}}{R_{\text{in}}}$$

$V_{\text{out2}}$  is in phase with  $V_{\text{in}}$  and  $V_{\text{out1}}$  is phased  $180^\circ$  with  $V_{\text{in}}$ . This means that the positive terminal of the loudspeaker should be connected to  $V_{\text{out2}}$  and the negative to  $V_{\text{out1}}$ .

## 4.3 Low and high frequency response

In the low frequency region,  $C_{\text{in}}$  starts to have an effect.  $C_{\text{in}}$  forms with  $R_{\text{in}}$  a high-pass filter with a -3dB cut-off frequency:

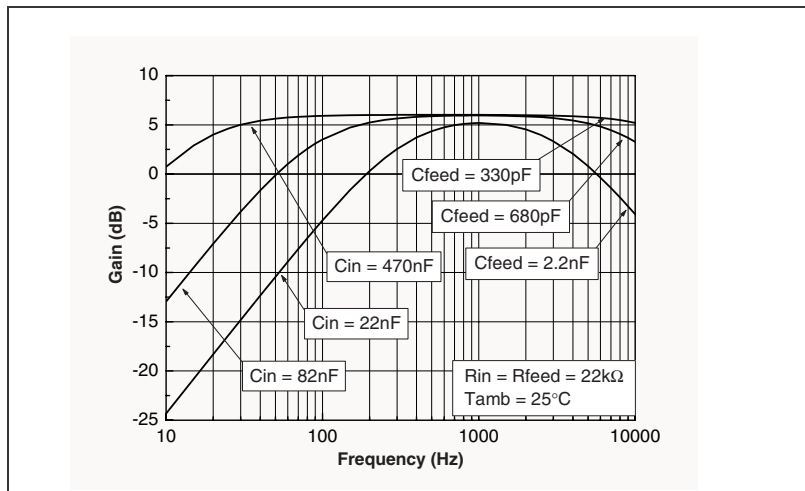
$$F_{\text{CL}} = \frac{1}{2\pi R_{\text{in}} C_{\text{in}}} \quad (\text{Hz})$$

In the high frequency region, you can limit the bandwidth by adding a capacitor ( $C_{\text{feed}}$ ) in parallel with  $R_{\text{feed}}$ . It forms a low-pass filter with a -3dB cut-off frequency.  $F_{\text{CH}}$  is in Hz.

$$F_{\text{CH}} = \frac{1}{2\pi R_{\text{feed}} C_{\text{feed}}} \quad (\text{Hz})$$

The following graph (*Figure 63*) shows an example of  $C_{in}$  and  $C_{feed}$  influence.

**Figure 63. Frequency response gain versus  $C_{in}$  &  $C_{feed}$**



### 4.4 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal ( $V_{out}$  and  $I_{out}$ ).
- Supply voltage is a pure DC source ( $V_{CC}$ ).

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin \omega t \quad (V)$$

and

$$I_{out} = \frac{V_{out}}{R_L} \quad (A)$$

and

$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \quad (W)$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2 \frac{V_{PEAK}}{\pi R_L} \quad (A)$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} \cdot I_{CC_{AVG}} \quad (W)$$

Then, the **power dissipated by each amplifier** is:

$$P_{diss} = P_{supply} - P_{out} \quad (W)$$

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \cdot \sqrt{P_{out}} - P_{out} \quad (W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{\text{diss}}}{\partial P_{\text{out}}} = 0$$

and its value is:

$$P_{\text{dissmax}} = \frac{2V_{\text{CC}}^2}{\pi^2 R_{\text{L}}} \quad (\text{W})$$

*Note:* This maximum value is only depending on power supply voltage and load values.

The **efficiency**,  $\eta$ , is the ratio between the output power and the power supply:

$$\eta = \frac{P_{\text{out}}}{P_{\text{supply}}} = \frac{\pi V_{\text{PEAK}}}{4V_{\text{CC}}}$$

The maximum theoretical value is reached when  $V_{\text{PEAK}} = V_{\text{CC}}$ , so that:

$$\frac{\pi}{4} = 78.5\%$$

The TS4984 has two independent power amplifiers, and each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of the each amplifier's maximum power dissipation. It is calculated as follows:

$P_{\text{diss1}}$  = Power dissipation due to the 1st channel power amplifier.

$P_{\text{diss2}}$  = Power dissipation due to the 2nd channel power amplifier.

Total  $P_{\text{diss}} = P_{\text{diss1}} + P_{\text{diss2}}$  (W)

In most cases,  $P_{\text{diss1}} = P_{\text{diss2}}$ , giving:

$$\text{Total } P_{\text{diss}} = P_{\text{diss1}} = P_{\text{diss2}} \quad (\text{W})$$

or, stated differently:

$$\text{Total } P_{\text{diss}} = \frac{4\sqrt{2}V_{\text{CC}}}{\pi\sqrt{R_{\text{L}}}} \sqrt{P_{\text{out}}} - 2P_{\text{out}} \quad (\text{W})$$

## 4.5 Decoupling the circuit

Two capacitors are needed to correctly bypass the TS4984. A power supply bypass capacitor  $C_{\text{S}}$  and a bias voltage bypass capacitor  $C_{\text{b}}$ .

$C_{\text{S}}$  has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for  $C_{\text{S}}$  of 1 $\mu\text{F}$ , you can expect similar THD+N performances to those shown in the datasheet. For example:

- In the high frequency region, if  $C_{\text{S}}$  is lower than 1 $\mu\text{F}$ , it increases THD+N and disturbances on the power supply rail are less filtered.
- On the other hand, if  $C_{\text{S}}$  is higher than 1 $\mu\text{F}$ , those disturbances on the power supply rail are more filtered.

$C_{\text{b}}$  has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region), in the following manner:

- If  $C_{\text{b}}$  is lower than 1 $\mu\text{F}$ , THD+N increases at lower frequencies and PSRR worsens.

- If  $C_b$  is higher than  $1\mu\text{F}$ , the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

*Note:* The TS4984FC has two BYPASS pins.  $C_b$  can be connected equally to pin C5 or to pin C1. These pins are internally connected. Connecting pin C5 and pin C1 together by an external wire is optional.

$C_{in}$  has a non-negligible effect on PSRR at lower frequencies. The lower the value of  $C_{in}$ , the higher the PSRR.

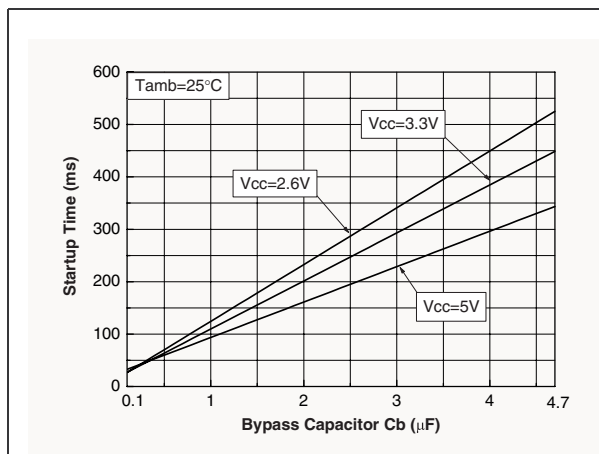
### 4.6 Wake-up time, $t_{wu}$

When the standby is released to put the device ON, the bypass capacitor  $C_b$  will not be charged immediately. As  $C_b$  is directly linked to the bias of the amplifier, the bias will not work properly until the  $C_b$  voltage is correct. The time required to reach this voltage is called the wake-up time or  $t_{wu}$  and specified in the tables in *Chapter 3: Electrical Characteristics* with  $C_b = 1\mu\text{F}$ .

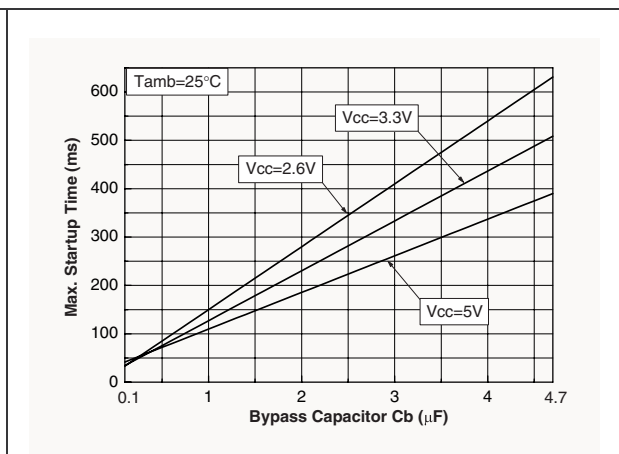
If  $C_b$  has a value other than  $1\mu\text{F}$ , please refer to the graph in *Figure 64* to establish the wake-up time value.

Due to process tolerances, the maximum value of wake-up time could be established by the graph in *Figure 65*.

**Figure 64. Typical wake-up time vs.  $C_b$**



**Figure 65. Maximum wake-up time vs.  $C_b$**



*Note:* Bypass capacitor  $C_b$  as also a tolerance of typically  $\pm 20\%$ . To calculate the wake-up time with this tolerance, refer to the previous graph (considering for example for  $C_b = 1\mu\text{F}$  in the range of  $0.8\mu\text{F} \leq 1\mu\text{F} \leq 1.2\mu\text{F}$ ).

### 4.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

*Note:* In shutdown mode, Bypass pin and  $V_{in-}$  pin are short-circuited to ground by internal switches. This allows for the quick discharge of the  $C_b$  and  $C_{in}$  capacitors.

### 4.8 Pop performance

Pop performance is intimately linked with the size of the input capacitor  $C_{in}$  and the bias voltage bypass capacitor  $C_b$ .

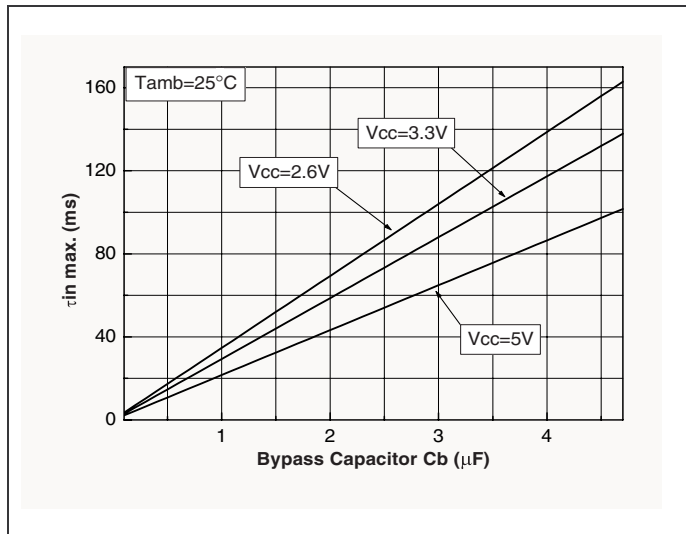
The size of  $C_{in}$  is dependent on the lower cut-off frequency and PSRR values requested. The size of  $C_b$  is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover,  $C_b$  determines the speed with which the amplifier turns ON. In order to reach near zero pop and click, the equivalent input constant time,

$$\tau_{in} = (R_{in} + 2k\Omega) \times C_{in} \text{ (s) with } R_{in} \geq 5k\Omega$$

must not reach the  $\tau_{in}$  maximum value as indicated in the graph below in *Figure 66*.

**Figure 66.  $\tau_{in}$  max. versus bypass capacitor**



By following the previous rules, the TS4984 can reach near zero pop and click even with high gains such as 20dB.

**Example calculation:**

With  $R_{in} = 22k\Omega$  and a 20Hz, -3dB lower cut-off frequency,  $C_{in} = 361nF$ .

So,  $C_{in} = 390nF$  with standard value which gives a lower cut-off frequency equal to 18.5Hz.

In this case,  $(R_{in} + 2k\Omega) \times C_{in} = 9.36ms$ .

When referring to the previous graph, if  $C_b = 1\mu F$  and  $V_{CC} = 5V$ , we read 20 ms max.

This value is twice as high as our current value, thus we can state that pop and click will be reduced to its lowest value. Minimizing both  $C_{in}$  and the gain benefits both the pop phenomena, and the cost and size of the application.

### 4.9 Application example: differential-input BTL power stereo amplifier

The schematic in *Figure 67* shows how to design the TS4984 to work in differential-input mode. For this discussion, only the left-channel amplifier will be referred to.

Let:

$$R_{1R} = R_{2L} = R_1, R_{2R} = R_{2L} = R_2$$

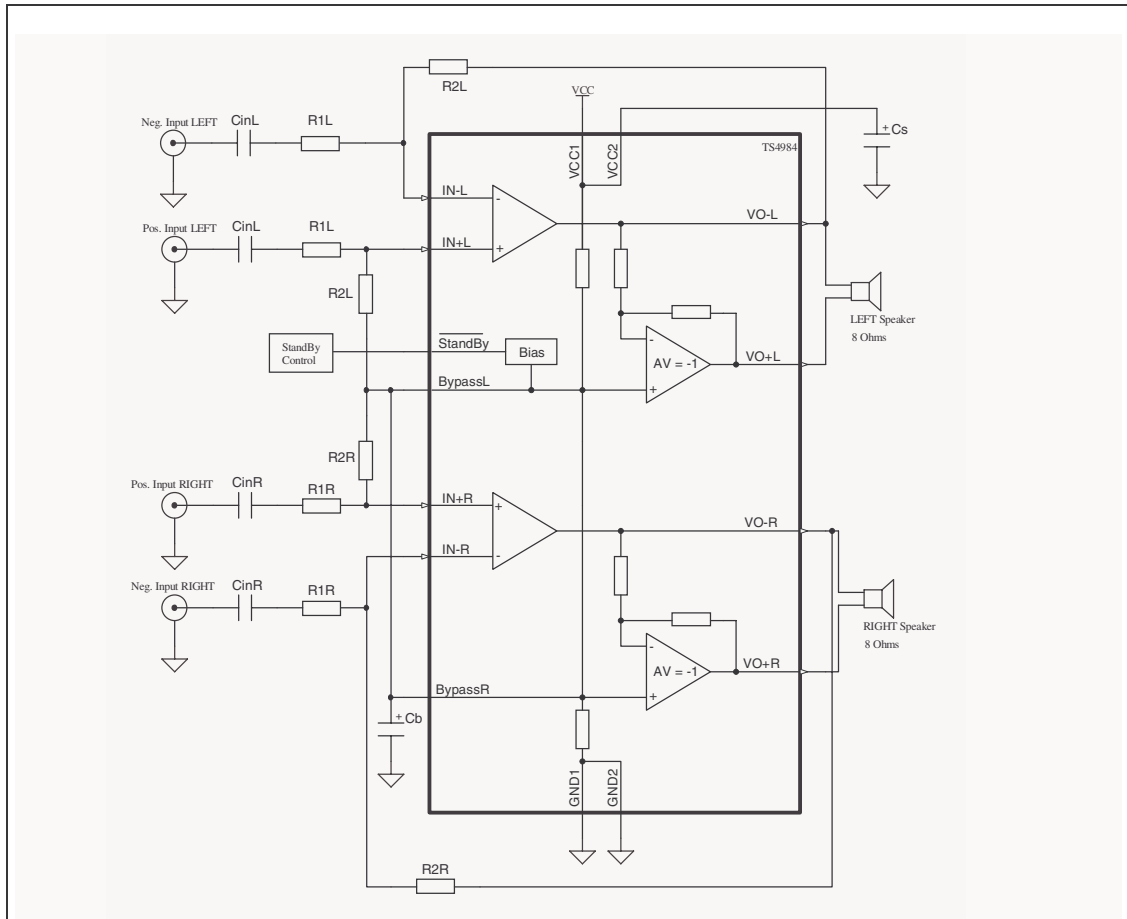
$$C_{inR} = C_{inL} = C_{in}$$

The gain of the amplifier is:

$$G_{Vdif} = 2 \frac{R_2}{R_1}$$

In order to reach the optimal performance of the differential function,  $R_1$  and  $R_2$  should be matched at 1% maximum.

**Figure 67. Differential input amplifier configuration**



The value of the input capacitor  $C_{in}$  can be calculated with the following formula, using the -3dB lower frequency required (where  $F_L$  is the lower frequency required):

$$C_{in} \approx \frac{1}{2\pi R_1 F_L} \quad (F)$$



Note: This formula is true only if:

$$F_{CB} = \frac{1}{2\pi(R_1 + R_2)C_b} \quad (\text{Hz})$$

is 5 times lower than  $F_L$ .

The following bill of materials is provided as an example of a differential amplifier with a gain of 2 and a -3dB lower cut-off frequency of about 80Hz.

**Table 8. Example of a bill of materials**

Designator	Part Type
$R_{1L} = R_{1R}$	20kΩ / 1%
$R_{2L} = R_{2R}$	20kΩ / 1%
$C_{inR} = C_{inL}$	100nF
$C_b = C_s$	1μF
U1	TS4984

### 4.10 Demoboard

A demoboard for the TS4984 in flip-chip package is available.

For more information about this demoboard, please refer to **Application Note AN2153**, which can be found on [www.st.com](http://www.st.com).

*Figure 68* shows the component locations, and *Figure 69* and *Figure 70* show top layer and bottom layers of the demoboard, respectively. *Figure 71* shows a schematic of the demoboard

**Figure 68. Component locations**

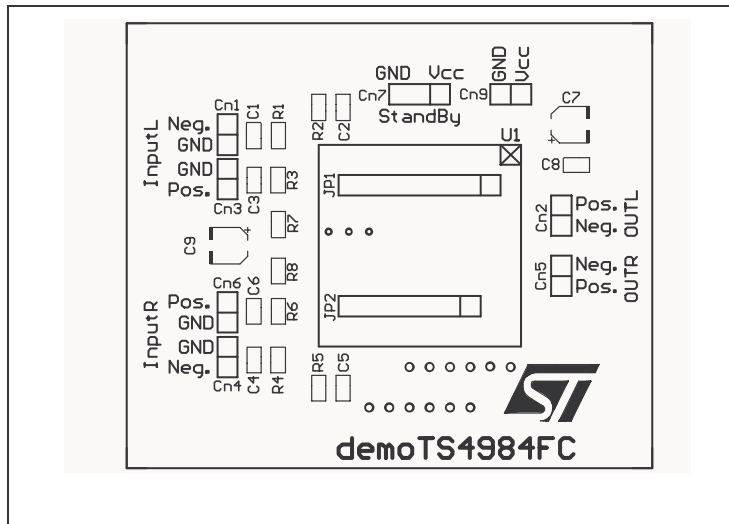


Figure 69. Top layer

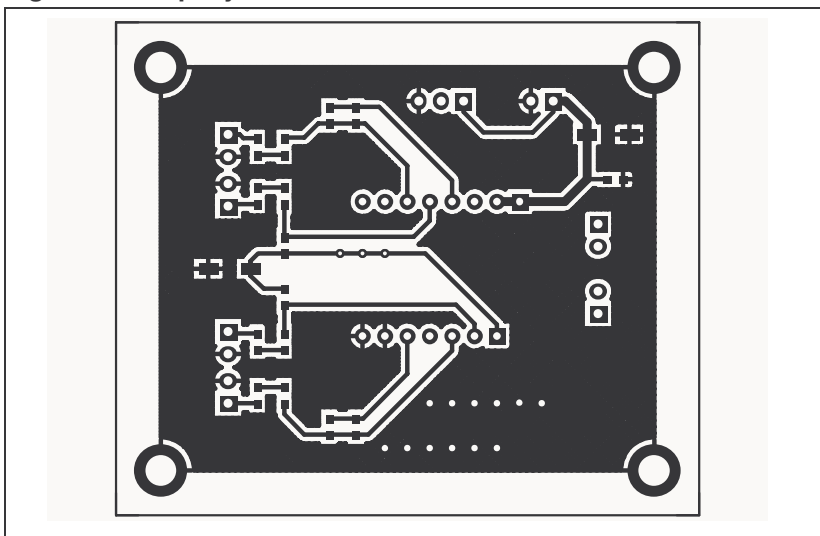


Figure 70. Bottom layer

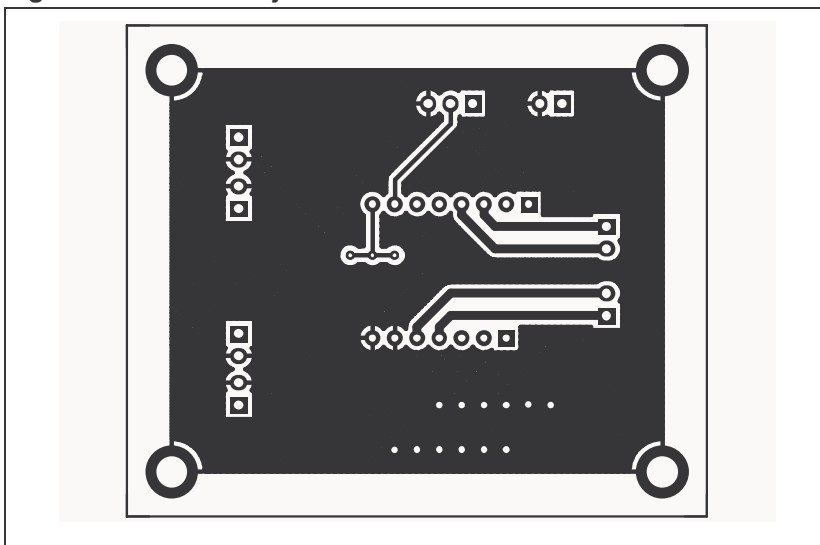
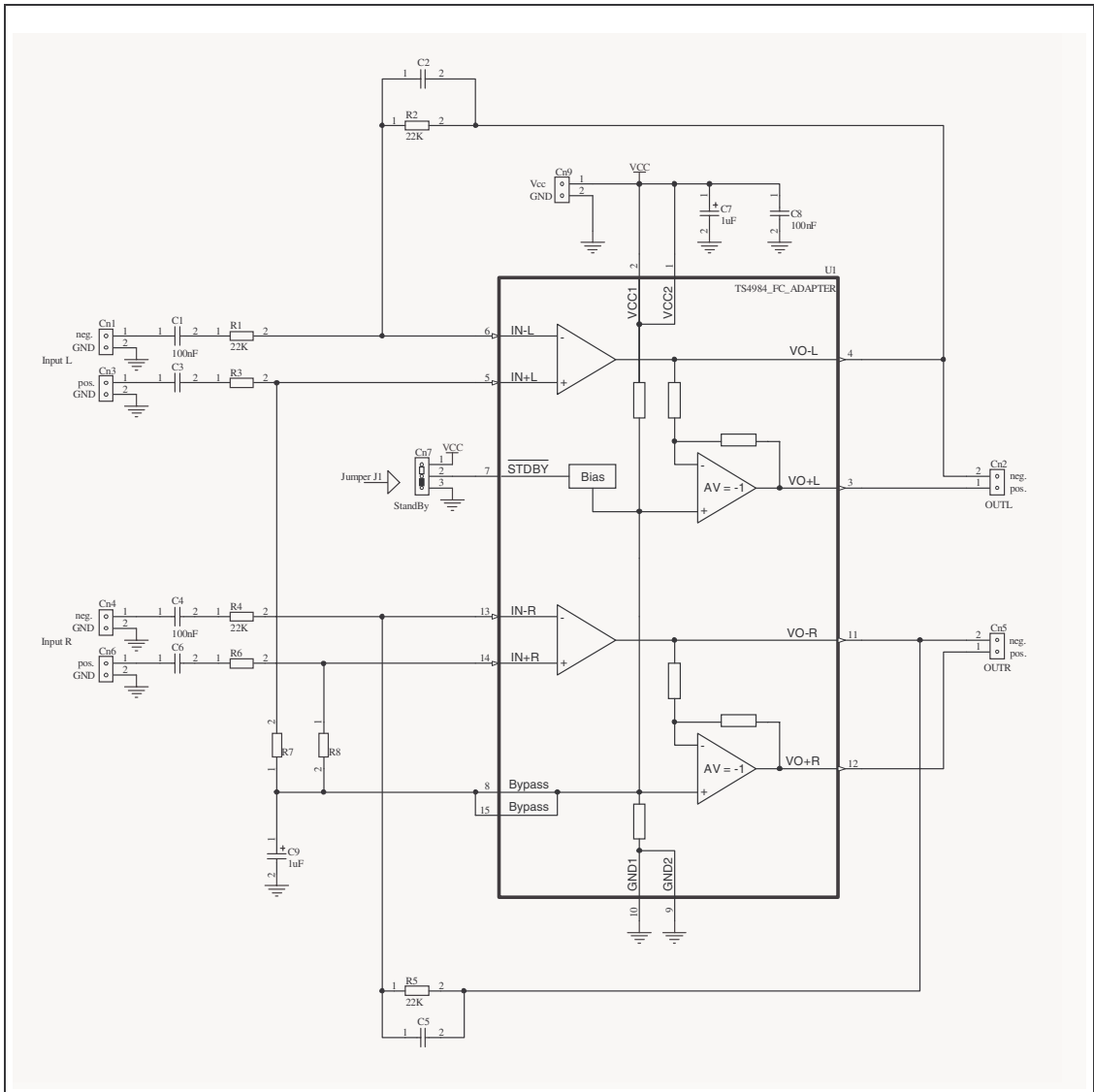


Figure 71. Demoboard schematic



## 5 Package Mechanical Data

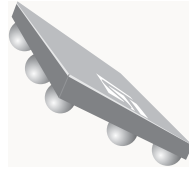


Figure 72. Pinout (top view)

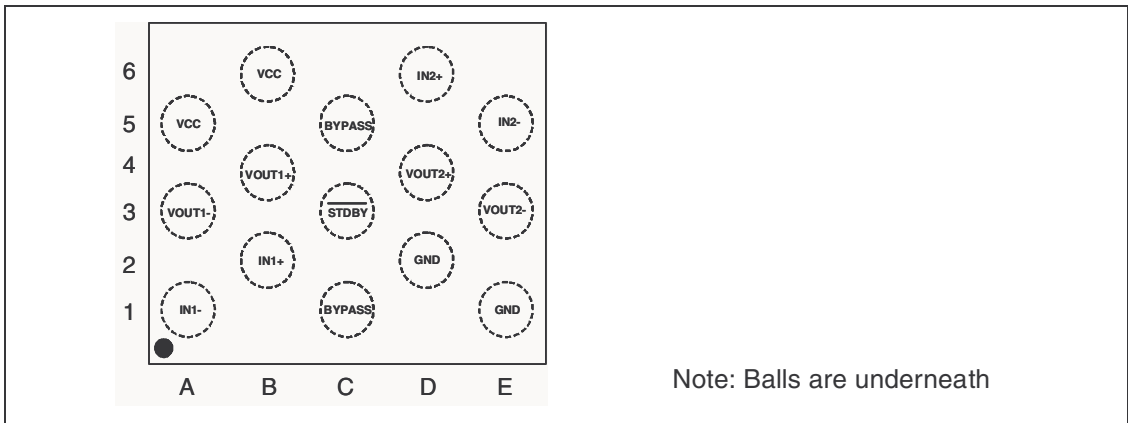


Figure 73. Marking (top view)

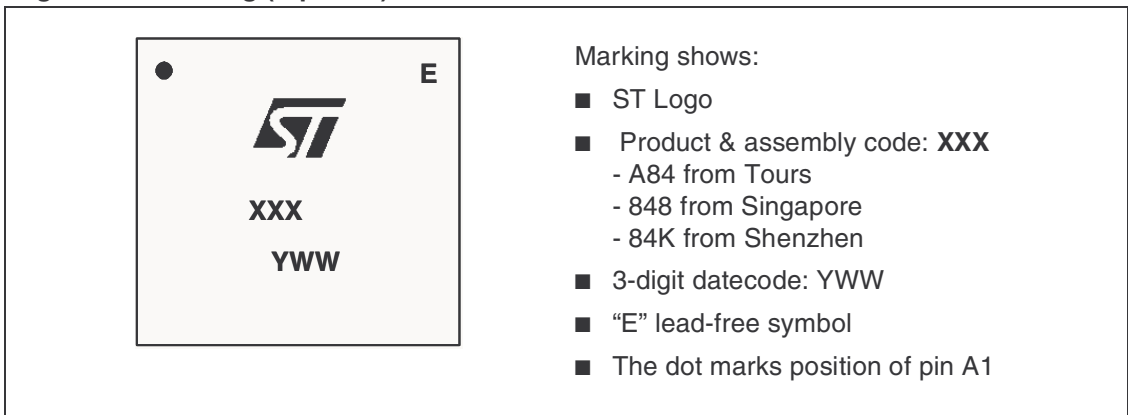


Figure 74. Package mechanical data for 15-bump flip-chip

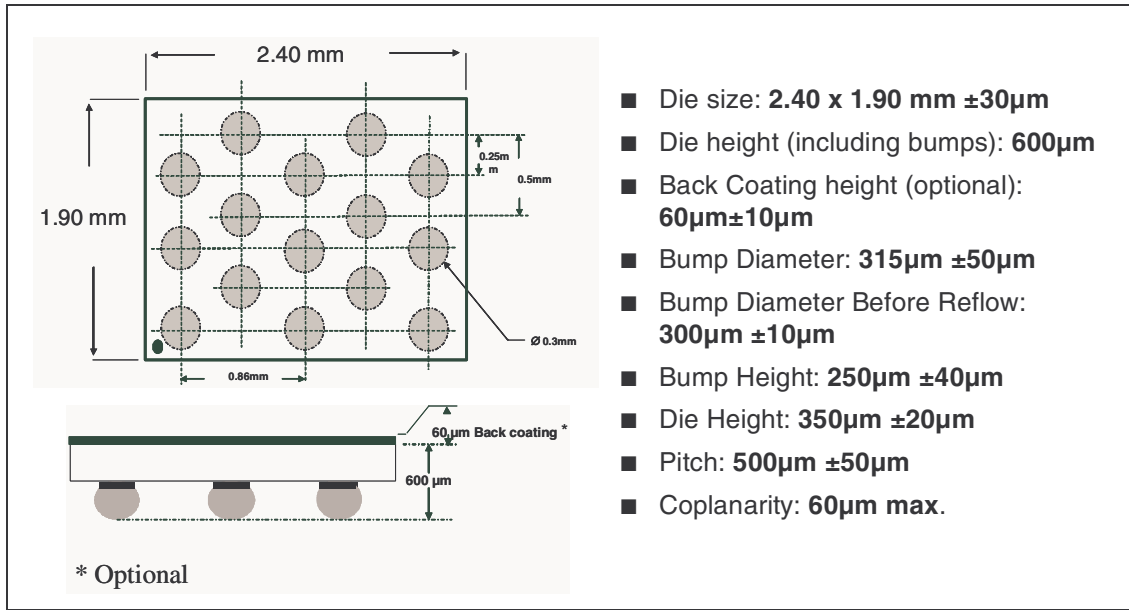
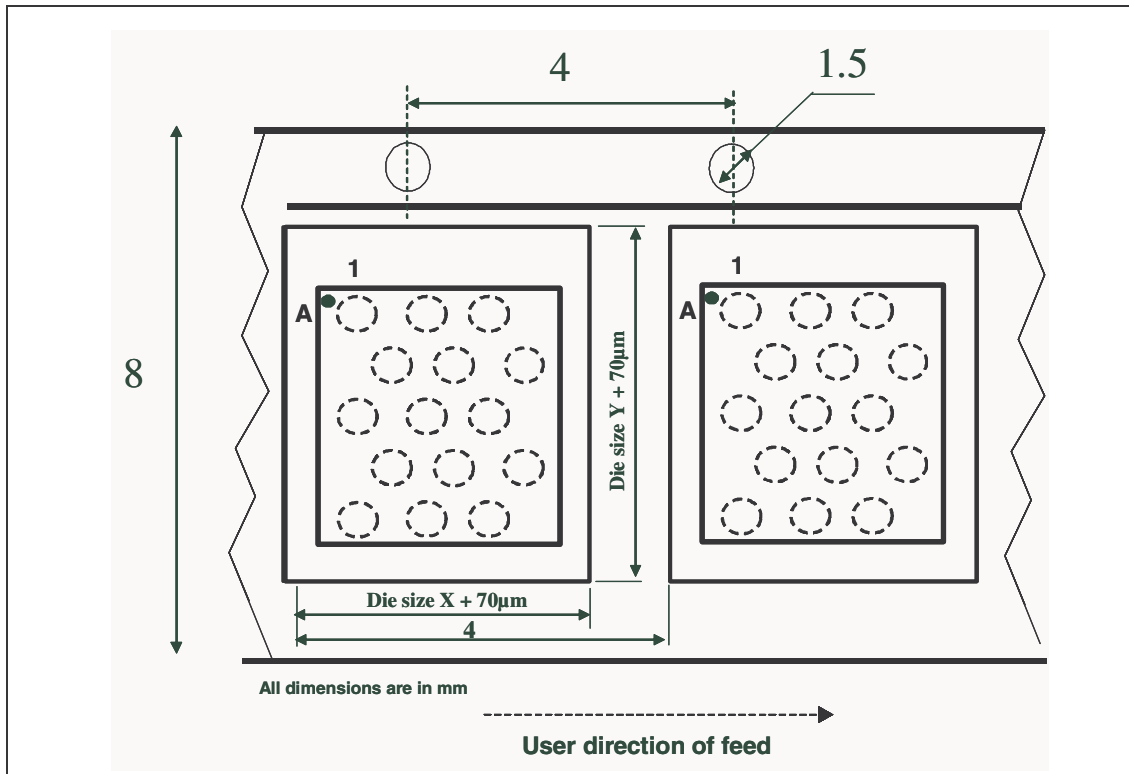


Figure 75. Tape & Reel specification (top view)



## 6 Revision History

Date	Revision	Changes
20 May 2005	1	Initial release.
Nov. 2005	2	Typical application schematic corrected see <i>Figure 1: Application information on page 2</i> . Change to layout of tables in <i>Chapter 3: Electrical Characteristics on page 4</i> . Minor grammatical and formatting changes throughout.

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