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SCES346C-JANUARY 2001-REVISED DECEMBER 2005

FEATURES

- Member of the Texas Instruments Widebus™ Family
- UBT[™] Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes
- TI-OPC[™] Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC[™] Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels
- GTLP Buffered CLKAB Signal (CLKOUT)
- LVTTL Interfaces Are 5-V Tolerant
- High-Drive GTLP Outputs (100 mA)
- LVTTL Outputs (-24 mA/24 mA)
- Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG PACKAGE (TOP VIEW)

1		_	
OEAB[₁ O	64	CEAB
LEAB[2	63	CLKAB
A1[3	62] B1
A2[4	61	B2
GND[5	60] GND
A3[6	59] B3
v _{cc} [7	58	BIAS V _{CC}
A4[8	57] B4
A5[9	56] B5
GND	10	55] GND
A6[11	54] B6
A7[12	53] B7
A8[13	52] B8
GND	14	51] GND
A9[15	50] B9
Vcc	16	49] v _{cc}
A10[17	48] B10
GND	18] GND
A11	19	r] B11
A12[20		B12
GND	21] GND
A13	22	43	B13
A14	23	t	B14
GND[24	41	GND
A15	25	- 1	B15
V _{CC} [26	39	V_{REF}
A16	27] B16
ERC[28	· •	GND
A17	29	36	B17
CLKIN	30	35	CLKOUT
OEBA	31	34	CLKBA
LEBA	32	33	CEBA

DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH1616 is a high-drive, 17-bit UBTTM transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent, latched, clocked, or clock-enabled modes of data transfer. Additionally, it provides for a copy of CLKAB at GTLP signal levels (CLKOUT) and conversion of a GTLP clock to LVTTL logic levels (CLKIN). The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OECTM circuitry, and TI-OPCTM circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes, with equivalent load impedance down to 11 Ω.



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17-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1616 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2 \text{ V}$ and $V_{REF} = 0.8 \text{ V}$) or GTLP ($V_{TT} = 1.5 \text{ V}$ and $V_{REF} = 1 \text{ V}$) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port reference input voltage.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (\overline{ERC}). Changing the \overline{ERC} input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP - DGG	Tape and reel	SN74GTLPH1616DGGR	GTLPH1616

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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FUNCTIONAL DESCRIPTION

The SN74GTLPH1616 is a high-drive (100 mA), 17-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes, and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1616 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
Registered transceiver	'646, '652			'16646, '16652	'16474
Flip-flop	'374, '574		'821	'16374	
Standard UBT					'16500, '16501
Universal bus driver					'16835
Registered transceiver with clock enable	'2952			'16470, '16952	
Flip-flop with clock enable	'377	'823			'16823
Standard UBT with clock enable					'16600, '16601
SN74GTL	PH1616 UBT transce	iver replace	s all above	functions	

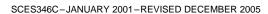
Additionally, the device allows for transparent conversion of CLKAB-to-GTLP signal levels (CLKOUT) and CLKOUT-to-LVTTL logic levels (CLKIN).

Data flow in each direction is controlled by clock enables (\overline{CEAB} and \overline{CEBA}), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables (\overline{OEAB} and \overline{OEBA}). \overline{CEAB} and \overline{CEBA} enable all 17 bits, and \overline{OEBA} and \overline{OEBA} control the 17 bits of data and the CLKOUT/CLKIN buffered clock path for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{\text{CEAB}}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{\text{CEAB}}$ and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{\text{OEAB}}$ is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except CEBA, OEBA, LEBA, and CLKBA are used.

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FUNCTION TABLES

OUTPUT ENABLE⁽¹⁾

INPUTS					OUTPUT	MODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
X	Н	Χ	Χ	X	Z	Isolation
L	L	L	Н	X	B ₀ ⁽²⁾	Latebad starage of A data
L	L	L	L	X	B ₀ ⁽³⁾	Latched storage of A data
Х	L	Н	Х	L	L	Two transparent
X	L	Н	X	Н	Н	True transparent
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	\uparrow	Н	Н	Clocked storage of A data
Н	L	L	Х	Х	B ₀ ⁽³⁾	Clock inhibit

- (1) A-to-B data flow is shown; B-to-A data flow is similar, but uses $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, LEBA, and CLKBA. The condition when $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ are both low at the same time is not recommended.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
- (3) Output level before the indicated steady-state input conditions were established

BUFFERED CLOCK

	INPUTS			OPERATION OR	MODE
CE	LE	OEAB	OEBA	FUNCTION	MODE
Х	Х	Н	Н	Z	Isolation
Х	Χ	L	Н	CLKAB to CLKOUT	True delayed clock signal
Х	Χ	Н	L	CLKOUT to CLKIN	True delayed clock signal
Х	X	L	L	CLKAB to CLKOUT, CLKOUT to CLKIN	True delayed clock signal with feedback path (1)

(1) This condition is not recommended.

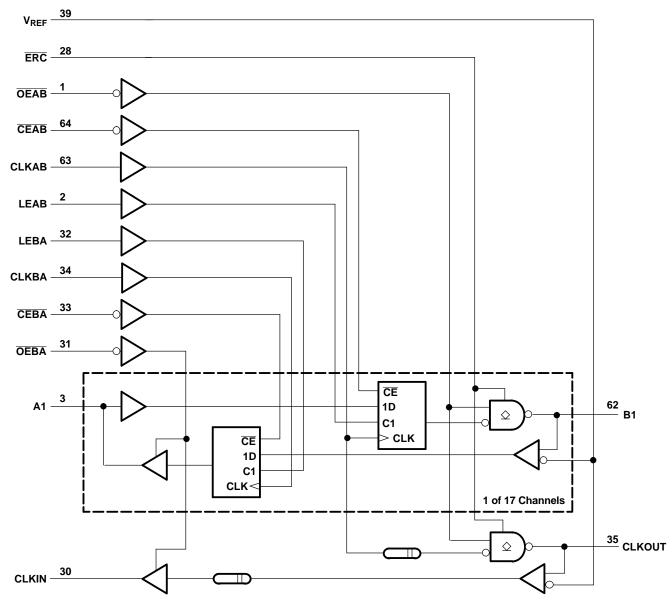
B-PORT EDGE-RATE CONTROL (ERC)

IN	IPUT ERC	OUTPUT
LOGIC LEVEL	NOMINAL VOLTAGE	B-PORT EDGE RATE
L	GND	Slow
Н	V _{CC}	Fast



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LOGIC DIAGRAM (POSITIVE LOGIC)



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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range				V
V	Input voltage range (2)	A-port, ERC, and control inputs	-0.5	7	V
VI	input voitage range · ·	B port and V _{REF}	-0.5	4.6	V
V	Voltage range applied to any output	A port	-0.5	7	V
Vo	in the high-impedance or power-off state (2)	B port	-0.5	4.6	V
	Command into any systematic the law state	A port		48	A
Io	Current into any output in the low state	B port		200	mA
Io	Current into any A-port output in the high state (3)			48	mA
	Continuous current through each V _{CC} or GND			±100	mA
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
θ_{JA}	Package thermal impedance (4)			55	°C/W
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and V_O > V_{CC}.
 (4) The package thermal impedance is calculated in accordance with JESD 51-7.



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Recommended Operating Conditions (1)(2)(3)(4)

			MIN	NOM	MAX	UNIT	
$V_{\rm CC}$ BIAS $V_{\rm CC}$	Supply voltage		3.15	3.3	3.45	٧	
V	Tormination voltage	GTL	1.14	1.2	1.26	V	
VTT	Termination voltage	GTLP	1.35	1.5	1.65	V	
M	Deference voltage	GTL	0.74	0.8	0.87	٧	
VREF	Reference voltage	GTLP	0.87	1	1.1	V	
M	lanut valtaga	B port			V_{TT}	V	
V _I	Input voltage	Except B port		V _{CC}	5.5	V	
V _{IH}	High-level input voltage	B port	V _{REF} + 0.05				
		ERC	V _{CC} - 0.6	V _{CC}	5.5	V	
		Except B port and ERC	2				
		B port			V _{REF} - 0.05		
V _{IL}	Low-level input voltage	ERC		GND	0.6	V	
V_{REF} Refe V_{I} Input V_{IH} High- V_{IL} Low- I_{IK} Input I_{OH} High- I_{OL} Low- $\Delta t/\Delta V$ Input $\Delta t/\Delta V_{CC}$ Power		Except B port and ERC			0.8		
I _{IK}	Input clamp current				-18	mA	
I _{OH}	High-level output current	A port			-24	mA	
	Low lovel output ourrent	A port			24	A	
I _{OL}	Low-level output current	B port			100	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10	ns/V	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			μs/V	
T _A	Operating free-air temperature		-40		85	°C	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
- Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3 \text{ V}$ first, I/O second, and $V_{CC} = 3.3 \text{ V}$ last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.
- V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc-recommended I_{OL} ratings are not exceeded. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} . TI-OPC circuitry is enabled in the A-to-B direction and is activated when $V_{TT} > 0.7$ V above V_{REF} . If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current

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Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

F	PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}		V _{CC} = 3.15 V,	I _I = -18 mA			-1.2	V
		V _{CC} = 3.15 V to 3.45 V,	$I_{OH} = -100 \mu A$	V _{CC} - 0.2			
V_{OH}	A port	V 245 V	I _{OH} = -12 mA	2.4			V
		V _{CC} = 3.15 V	$I_{OH} = -24 \text{ mA}$	75 -75 -75 -700 -500 -6.5 -9.5 -11			
		V _{CC} = 3.15 V to 3.45 V,	I _{OL} = 100 μA			0.2	
	A port	V 245 V	I _{OL} = 12 mA			0.4	
\ /		V _{CC} = 3.15 V	I _{OL} = 24 mA			0.5	V
V_{OL}			I _{OL} = 10 mA	-1.2 V _{CC} - 0.2 2.4 2 0.2 0.4 0.5 0.5 0.2 0.4 0.55 ±10 10 10 75 -75 500 -500 45 45 45 1.5 4 5.5 6.5 8	V		
	B port	V _{CC} = 3.15 V	$I_{OL} = 64 \text{ mA}$			0.4	
			I _{OL} = 100 mA		-1.2 0.2 0.4 0.5 0.2 0.4 0.55 ±10 10 -10 -10 45 45 45 45 45 1.5 4 5.5 6.5 8 9.5 11.5		
I _I	Control inputs	V _{CC} = 3.45 V,	V _I = 0 or 5.5 V			±10	μΑ
1 (2)	A port	V _{CC} = 3.45 V	$V_O = V_{CC}$			10	^
I _{OZH} ⁽²⁾	B port		V _O = 1.5 V			10	μΑ
I _{OZL} ⁽²⁾	A and B ports	V _{CC} = 3.45 V,	V _O = GND			-10	μΑ
I _{BHL} (3)	A port	V _{CC} = 3.15 V,	V _I = 0.8 V	75			μΑ
I _{BHH} ⁽⁴⁾	A port	V _{CC} = 3.15 V,	V _I = 2 V	-75			μΑ
I _{BHLO} ⁽⁵⁾	A port	V _{CC} = 3.45 V,	$V_I = 0$ to V_{CC}	500			μΑ
I _{BHHO} ⁽⁶⁾	A port	V _{CC} = 3.45 V,	$V_I = 0$ to V_{CC}	-500			μΑ
		V _{CC} = 3.45 V, I _O = 0,	Outputs high			45	
I_{CC}	A or B port	V_{I} (A-port or control input) = V_{CC} or GND,	Outputs low			45	mA
		V_I (B port) = V_{TT} or GND	Outputs disabled			45	
$\Delta I_{CC}^{(7)}$		V_{CC} = 3.45 V, One A-port or control input at Other A-port or control inputs at V_{CC} or GND				1.5	mA
C _i	Control inputs	V _I = 3.15 V or 0			4	5.5	pF
C	A port	V _O = 3.15 V or 0			6.5	8	nE.
C _{io}	B port or CLKOUT	V _O = 1.5 V or 0			9.5	11.5	pF
C _o	CLKIN	V _O = 3.15 V or 0			4.5	5.5	pF

- All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current. The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
- The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
- An external driver must source at least I_{BHLO} to switch this node from low to high.
- An external driver must sink at least I_{BHHO} to switch this node from high to low.
- This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			
l _{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0$ to 5.5 V	10	μΑ
l _{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V},$	$V_0 = 0.5 \text{ V to 3 V},$	OE = 0	±30	μΑ
I _{OZPD}	$V_{CC} = 1.5 \text{ V to } 0,$	$V_0 = 0.5 \text{ V to 3 V},$	OE = 0	±30	μΑ



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Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I _{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0$ to 1.5 V		10	μΑ
I _{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V},$	BIAS $V_{CC} = 0$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}, \overline{OE} = 0$		±30	μΑ
I _{OZPD}	$V_{CC} = 1.5 \text{ V to } 0,$	BIAS $V_{CC} = 0$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}, \overline{OE} = 0$		±30	μΑ
I (DIAC \/)	$V_{CC} = 0 \text{ to } 3.15 \text{ V}$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	V (P. port) = 0 to 1.5 V		5	mA
I _{CC} (BIAS V _{CC})	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	V_O (B port) = 0 to 1.5 V		10	μΑ
Vo	$V_{CC} = 0$,	BIAS $V_{CC} = 3.3 \text{ V}$,	I _O = 0	0.95	1.05	V
Io	V _{CC} = 0,	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	V _O (B port) = 0.6 V	-1		μΑ

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (unless otherwise noted)

			MIN	MAX	UNIT
f _{clock}	Clock frequency			175	MHz
	Pulse duration	LEAB or LEBA high	3		20
t _w	Pulse duration	CLKAB or CLKBA high or low	3		ns
		A before CLKAB↑	2.2		
		B before CLKBA↑	2.4		
	Cabus times	A before LEAB↓, CLK = Don't care	1.8		
t _{su} Setup time	Setup time	B before LEBA↓, CLK = Don't care	2.1		ns
		CEAB before CLKAB↑	1.5		
		CEBA before CLKBA↑	1.5		
		A after CLKAB↑	0.7		
		B after CLKBA↑	0.5		
		A after LEAB↓, CLK = Don't care	1.2		
t _h Hold time	Hold time	B after LEBA↓, CLK = Don't care	0.9		ns
		CEAB after CLKAB↑	1.5		
		CEBA after CLKBA↑	1.5		

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Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,

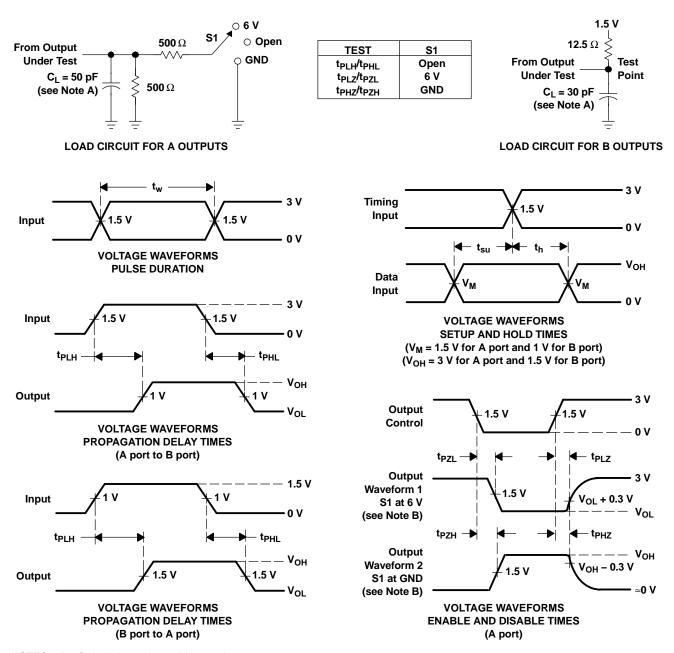
 $V_{TT} = 1.5 \text{ V}$ and $V_{REF} = 1 \text{ V}$ for GTLP (normal mode) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	MIN	TYP ⁽²⁾	MAX	UNIT	
f _{max}				175			MHz	
t _{PLH}	Α	В	Slow	4.3	5.6	7.1	ns	
t _{PHL}	Α	В	SiOW	3.2	4.6	6.4		
t _{PLH}	А	В	Fast	3.2	4.3	5.6	ns	
t _{PHL}	Α	В	rast	2.7	3.9	5.3		
t _{PLH}	LEAB	В	Slow	4.8	6.2	7.8	ns	
t _{PHL}	LLAD	В	Siow	3.5	4.9	6.7	113	
t _{PLH}	LEAB	В	Fast	3.5	4.8	6.2	ns	
t _{PHL}	LLAD	В	rast	3.1	4.3	5.8	115	
t _{PLH}	CLKAB	В	Slow	4.8	6.1	7.6	20	
t _{PHL}	CLNAD	Б	Siow	3.5	4.8	6.6	ns	
t _{PLH}	CLKAB	В	Fast	3.6	4.9	6.2	ns	
t _{PHL}	CLNAD	Б	Fasi	3.1	4.3	5.7		
t _{PLH}	CLKAB	CLKOLIT	Clave	5.5	6.9	8.5	ns	
t _{PHL}	CLKAB	CLKOUT	Slow	5.5	7	9.3		
t _{PLH}	CLKAB	CLKOUT	Fast	4	5.3	6.7	ns	
t _{PHL}	CLNAD	CLKOUT	Fast	4.4	5.8	7.6		
t _{en}	OEAB	D or OLKOLIT	Slow	4.8	6.2	7.8	ns	
t _{dis}	OEAB	B or CLKOUT	SIOW	3.4	5.2	7.8		
t _{en}	OFAD	D OLKOUT	Fact	3.6	4.8	6.2	ns	
t _{dis}	OEAB	B or CLKOUT	Fast	3	4.4	6.1		
	Diag time D aut	(200/ to 000/)	Slow		2.5		200	
t _r	Rise time, B out	puts (20% to 80%)	Fast	1.4		ns		
	E 11.0 D .	. (000/ 1 000/)	Slow 3.3					
t _f	Fall time, B out	outs (80% to 20%)	Fast		2.4	ns		
t _{PLH}	D			1.1	2.8	4.3	ns	
t _{PHL}	В	A	_	1.9	3.1	4.1		
t _{PLH}	LEDA			1.3	3.1	4.6		
t _{PHL}	LEBA	Α	_	1.4	2.6	3.8	ns	
t _{PLH}	011/04			1.3	3.3	4.8	ns	
t _{PHL}	CLKBA	A	_	1.8	2.9	4.1		
t _{PLH}	CLKOUT	OLIVIN		2.2	3.7	5.3		
t _{PHL}	CLKOUT	CLKIN	_	2.7	3.9	5.1	ne	
t _{en}		A 0117111		1.2	2.9	4.8		
t _{dis}	OEBA	A or CLKIN	_	2.3	4	5.5	ns	

⁽¹⁾ Slow (\overline{ERC} = GND) and Fast (\overline{ERC} = V_{CC}) (2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50~\Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 - D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (see Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be closely approximated to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

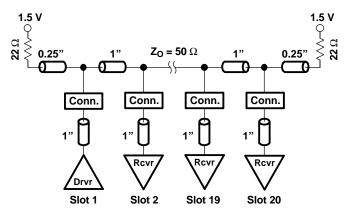


Figure 2. High-Drive Test Backplane

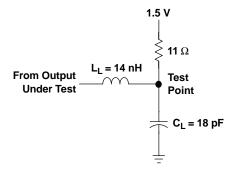


Figure 3. High-Drive RLC Network



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Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5 \text{ V}$ and $V_{REF} = 1 \text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	TYP ⁽²⁾	UNIT	
t _{PLH}	A	В	Slow	5.3	ns	
t _{PHL}	Α	В	Slow	5.3	110	
t _{PLH}	А	В	Fast	4	ns	
t _{PHL}	Α	В	i asi	4	113	
t _{PLH}	LEAB	В	Slow	5.2	ns	
t _{PHL}	LLAD	Б	Slow	5.2	113	
t _{PLH}	LEAB	В	Fast	3.9	ns	
t _{PHL}	LLAD	В	i asi	3.9	115	
t _{PLH}	CLK	В	Slow	5.5	ns	
t _{PHL}	OLIX	Б	Slow	5.5	113	
t _{PLH}	CLK	В	Fast	4.3	ns	
t _{PHL}	OLIK	5	1 431	4.3	113	
t _{PLH}	CLKAB	CLKOUT	Slow	5.9	ns	
t _{PHL}	CLIVID	OLINOOT	Clow	5.9	110	
t _{PLH}	CLKAB	CLKOUT	Fast	4.8	ns	
t _{PHL}	OLIVAD	OLKOOT	1 431	4.8	113	
t _{en}	OEAB	B or CLKOUT	Slow	5.7	ns	
t _{dis}	OLAD	D OF OLIVOOT	Olow	4.3	113	
t _{en}	OEAB	B or CLKOUT	Fast	4.3	ns	
t _{dis}	OLAD	D OF OLICOT	1 431	3.8	113	
t _r	Risa tima Routr	outs (20% to 80%)	Slow	2	ns	
ч	Nise time, b out	7410 (2070 10 0070)	Fast	1.2	113	
t _f	Fall time R outo	uts (80% to 20%)	Slow	2.5	ns	
Ч	i ali time, b outp	uis (00/0 to 20/0)	Fast	1.8	113	

⁽¹⁾ Slow (\overline{ERC} = GND) and Fast (\overline{ERC} = V_{CC}) (2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.





27-Sep-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins I	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74GTLPH1616DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74GTLPH1616DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLPH1616DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

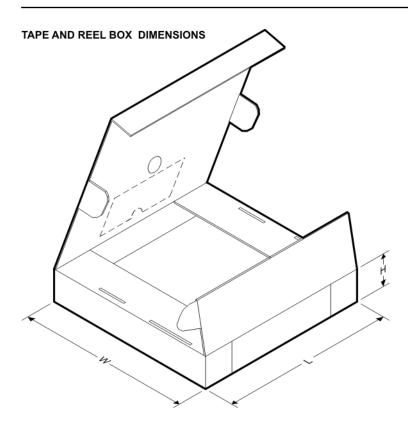
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH1616DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH1616DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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